

PIL testing of the Optical On-board Image Processing Solution for EO-ALERT

OBDP 2021

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Presented by Francisco Membibre



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EO-ALERT: Next generation satellite processing chain for rapid civil alerts

- H2020 project: DEIMOS SPACE, DLR, OHB, Politecnico di Torino, TU-GRAZ, DMS IMAGING
- **Objective:** On-board low latency processing of EO products
- DEIMOS SPACE is project coordinator and responsible of optical observables for Ship Detection and Extreme Weather products
- The tendency is towards product latency of 15 to 30 min
- Our latency is < 1 minute
- Idea: Move key EO data processing elements from GS to FS (using ML and AI onboard)
- Real image databases: from **DEIMOS-2 VHR optical** satellite and **MSG SEVIRI**
- Processing is done on a Multi-board scheme based on COTS to decrease processing time or cover more area
- Allowing to process 8400px x 12000px images (100 km² per board)

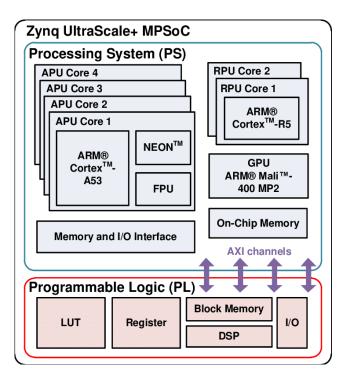




Architecture

COTS - Zynq® UltraScale+™ MPSoC





Shen, Zhuoxuan & Dinavahi, Venkata. (2018). Real-Time MPSoC-Based Electrothermal Transient Simulation of Fault Tolerant MMC Topology. IEEE Transactions on Power Delivery. PP. 1-1. 10.1109/TPWRD.2018.2866562.





Single Event Effect (SEE) Protections

Introduction of elements against radiation in COTS

- Single Event Upset (SEU)
 - User Memory
 - Error Detection and Correction (EDAC)
 - Configuration Memory
 - Memory Scrubbing (Soft Error Mitigation (SEM) IP)
- Single Event Latch-up (SEL)
 - Watch Dog

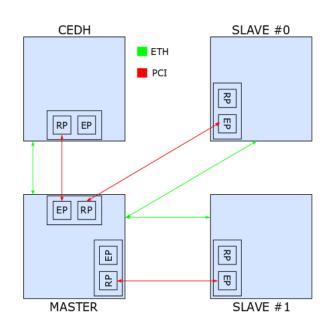
The system is protected by hardware redundancy (Spare Boards)





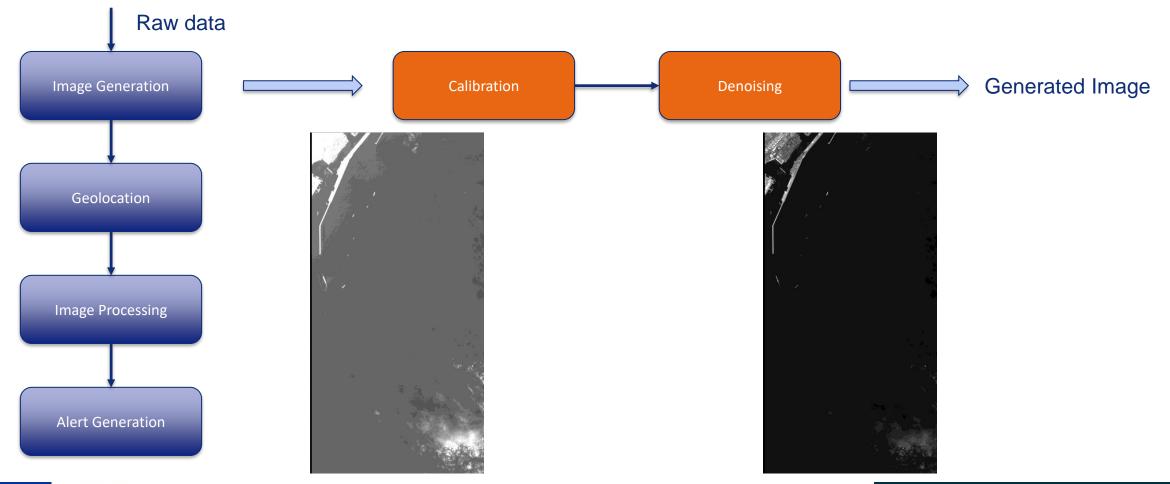
Multi-board Scheme – Test Bench Validation

- Data Storage & Transfer
- Interfaces
 - PCIe Data transfers
 - Ethernet Manage Data Transfers (Telecommands)
 - ➢ Will be replaced by CAN bus





Algorithms: Ship Detection

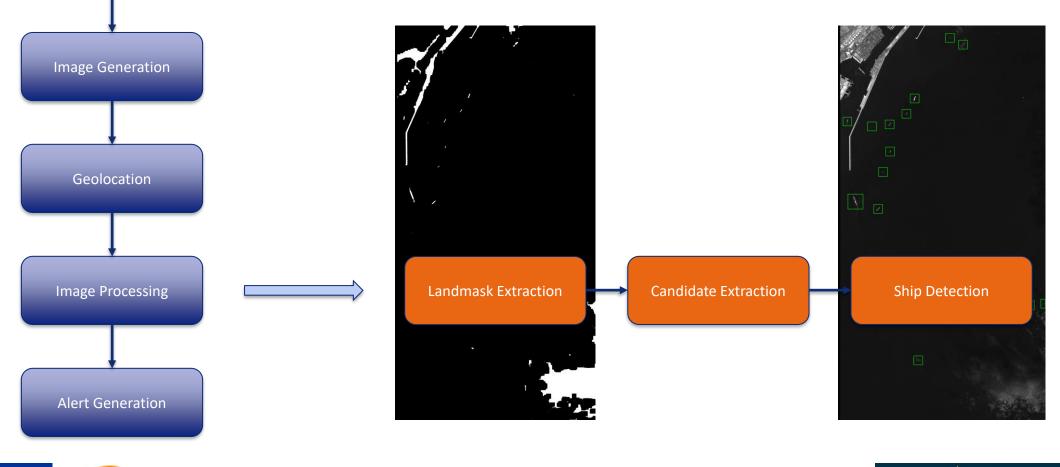




EOALERT



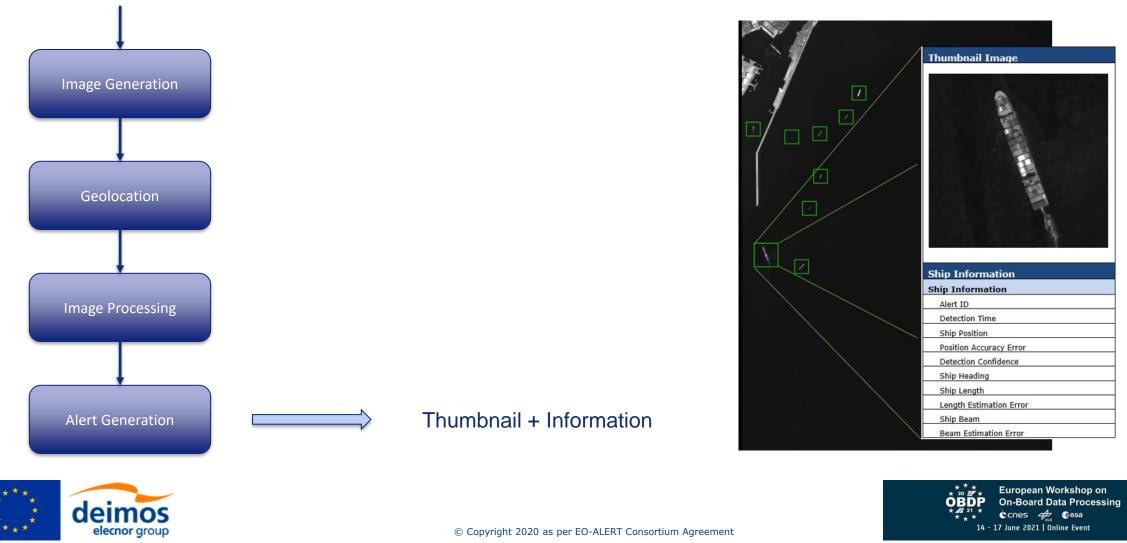
Algorithms: Ship Detection







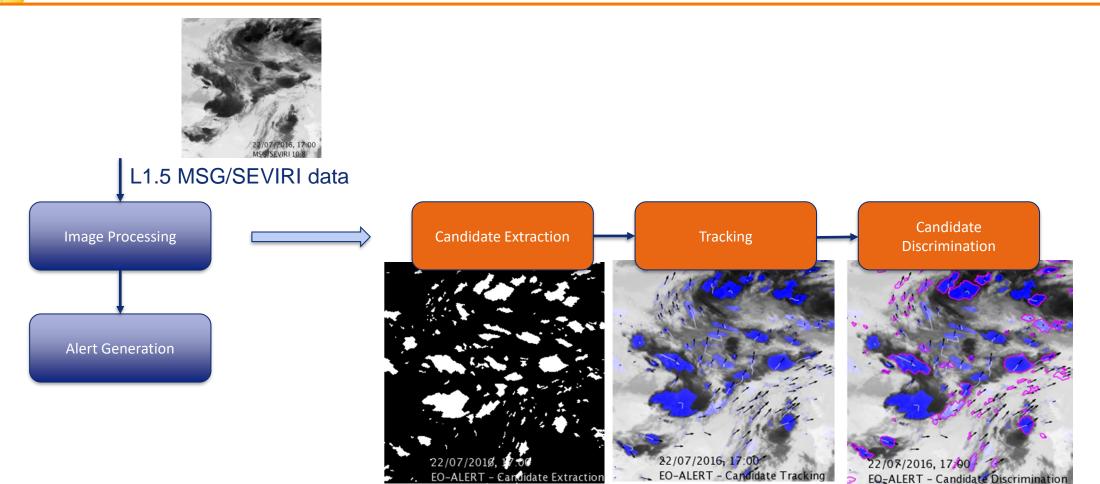
Algorithms: Ship Detection



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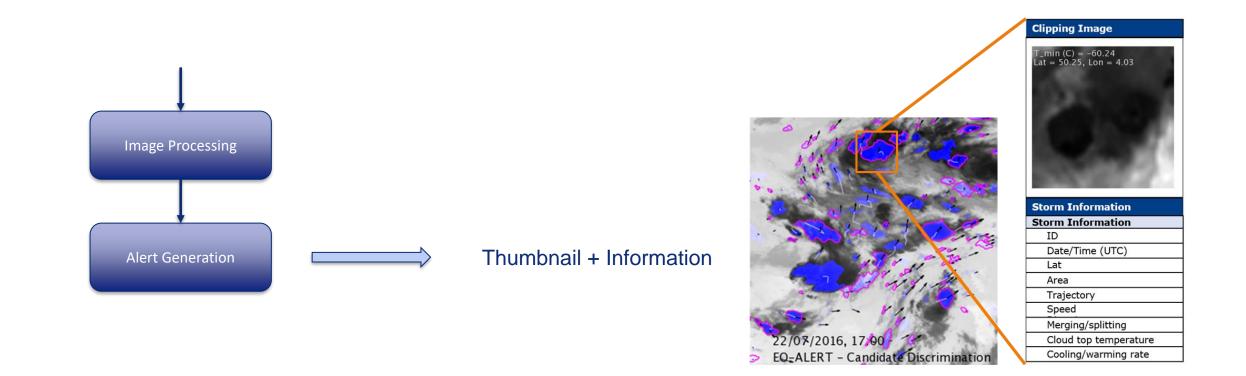
Algorithms: Extreme Weather







Algorithms: Extreme Weather



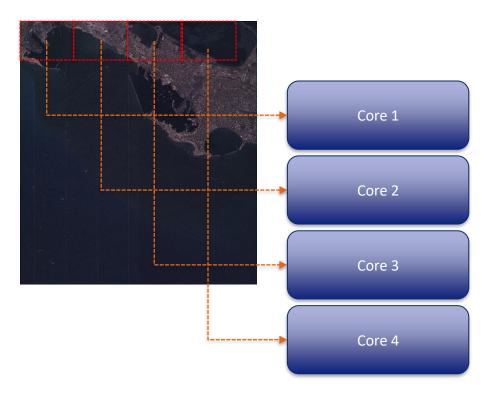




Implementation

HW/SW Processing Codesign

- Multi-core
 - Flexibility
 - Rapid development
- FPGA
 - Parallelism
 - Computing Power
 - Fixed Point Models MATLAB®
 - > Overflows
 - Unaligned
 - HW libraries SDSoC[™]/Vitis[™]
 - > OpenCV
 - Xilinx® IP COREs
 - Avoid HW-SW dependencies



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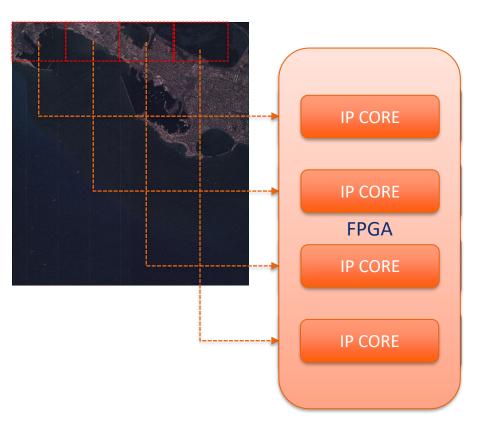




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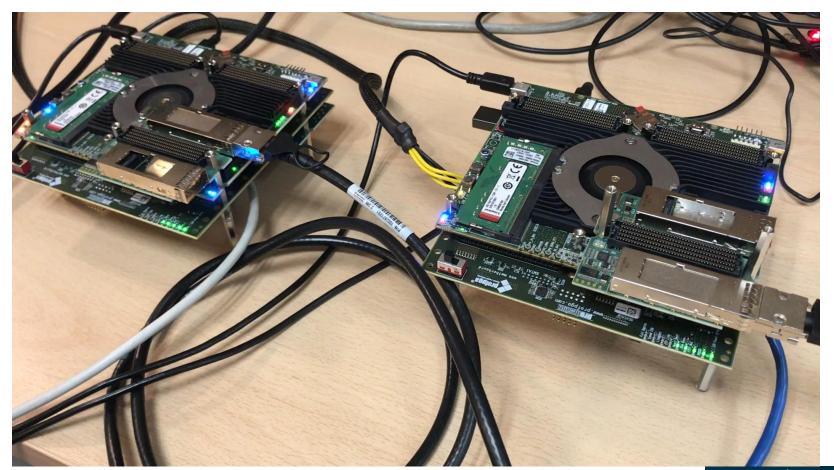
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Tests: Dual-board Scheme (Video)







Conclusions

- Next generation satellite processing chain for rapid civil alerts is the correct tendency to decrease product latency.
- These kinds of devices are increasingly used in space projects and contribute to put more computation power than ever before.
- Rapid prototyping allows developing from a global perspective.
- The time requirements have been validated on the TB:
 - 38 sec. (100 km²) One processing board. -> (8400 x 12000 px)
 - 115 sec. (900 km²) and 154 sec. (1200 km²) Three processing boards -> (3x3x8400x12000)px and (4x3x8400x12000)px
- There are several points that can be improved such as additional functions to the FPGA.
- This project is focus on Ship Detection and Extreme Weather but can be used for many other applications which use ML and Al.
- With these techniques (AI and ML), normally used on ground, it is possible to send results to the end user using near real time links with global coverture.







Thank you



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http://www.eo-alert-h2020.eu/





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