Enhanced Reliability of Fully Differential Difference Amplifier Through On-chip Digital Calibration

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Abstract—This paper presents a novel on-chip digital method of calibration for a fully differential difference amplifier (FDDA), which is aimed at improved performance and reliability through enhanced robustness against variations of process parameters, voltage, temperature, and ageing drift. The proposed method was designed and verified within 130 nm CMOS technology design kit in Cadence environment. Calibration hardware is built-in with the calibrated FDDA circuit, and the whole integrated system is able to operate with only 0.4 V power supply. The effectiveness of the proposed calibration method was examined mainly by evaluation of the FDDA input offset voltage using Monte Carlo, and process corners and ageing analyses performed for the temperature range from -20°C to 85°C . The work established metrics for comparison of different calibration methods (i.e. digital calibration, chopper stabilization, analog calibration and autozero), which significantly differ in fundamentals of their operation. The proposed digital calibration outperforms its alternatives, while the precision of calibration, area and power consumption overhead are considered. The less advanced topology of digital calibration was previously implemented for variable-gain amplifier with considerable success (residual offset of the calibrated amplifier reaches fair levels of $13\ \mu\text{V}$ to $167\ \mu\text{V}$). The concept proposed in this work utilizes advanced high precision calibration algorithm.

Index Terms—digital calibration, PVT variations, high reliability, high precision compensation, input offset voltage, ultra-low voltage design

I. INTRODUCTION

Integrated circuits (ICs) subject to a trend of constantly increasing density of integration of electronic components. Following the Moore's Law, the number of transistors packed on a single chip has grown from about 5 million to nearly 50 billion over the last 20 years [?]. Thanks to the enormous progress of fabrication processes of ICs, it is possible to implement smaller and smaller electronic components. Reducing the dimensions of these elements brings new possibilities for reducing the energy consumption of ICs. On the other hand, the manufacturing process of integrated circuits is not ideal. During the production of every chip, the imperfection of

process technology cause variations in parameters of sensitive analog ICs, which can significantly affect its overall functionality and reliability. Pure digital circuits (without analog parts) are not significantly sensitive to parameter fluctuations caused by manufacturing technology due to their discrete nature. These circuits can work very reliably also with ultra-low values of the supply voltage, since the tolerance of values of electrical voltage or current can be relatively large with respect to the defined value of the logic level.

II. MOTIVATION

On the contrary, analog and also mixed-signal ICs are extremely sensitive to fluctuations in their parameters due to their continuous nature. Therefore, analog designers are recently facing the challenge of robustness of IC design against these fluctuations. Without addressing this issue in the design phase, with continuous transistor size as well as the supply voltage scaling, analog ICs may lose their performance or/and reliability.

An effective solution to this problem is to design a type of subcircuit, so-called *calibration circuit* that will be as resistant as possible to imperfections of the production process and will not affect the overall power consumption significantly. The main task of the calibration circuitry is to compensate deficiencies of the key circuit parameters caused by the production process and other effects.

One of the most used analog integrated circuits is an operational amplifier (OPAMP). Ideally, its input common-mode level is set to half of the supply voltage value and its input offset voltage is suppressed to zero. However, in the real case, the influence of imperfections in the circuit's manufacturing process can cause the input offset voltage rise to the order of millivolts. Consequently, this might cause that the main differential pair transistors are realized with different channel lengths, which in turn creates different currents flowing through the differential pair.

In this work, the design of a calibration circuit, which can very effectively compensate the operational amplifier input offset voltage, is presented. The bulk-driven fully differential difference amplifier for ultra-low voltage applications - FDDA [?] is used as the calibrated device. In order to achieve the lowest possible sensitivity to the variations of manufacturing process and at the same time to achieve the lowest possible energy consumption, a digital calibration algorithm is employed. It was designed as a complex system used as a calibration circuit for an FDDA. Section III presents the design of the calibration circuit and principle of its operation. Part IV brings results of circuit verification in the Cadence environment through Monte Carlo analysis, Corner analysis and Reliability analysis. Section V presents the conclusion of this work.

III. OPERATION PRINCIPLE AND IMPLEMENTATION OF CALIBRATION CIRCUIT

Calibration circuit consists of five blocks: a control circuit, two counters and two digital-to-analog converters (DAC). From higher level of abstraction view, it is divided into three main parts: the control block, the main calibration part and the correction part, as shown in block diagram in Fig. 1. The whole circuit works as voltage-current converter, since the input of the calibration circuit is represented by the FDDA differential output voltage and the output of the calibration circuit creates the pair of compensation currents for the FDDA.

The basic principle of calibration circuit operation is that before the FDDA is initiated into the proper operation (function mode), the variations in currents flowing through the input differential pair of the FDDA are compensated in two cycles. In the first cycle, the main calibration block is in action. It injects currents I_{COMP+} and I_{COMP-} with a greater step to the input differential pair of the FDDA. The result of this cycle is a lower absolute value of the difference between the DC voltages $OUT+$ and $OUT-$. However, after this current compensation, the compensation of FDDA offset voltage is still not accurate enough. Therefore, in the second cycle, a correction calibration block injects compensation currents with a lower and more accurate step to the input differential pair of the FDDA. After its completion, the calibration circuit is switched off and the FDDA is ready for its use in application.

Fig. 1: Block diagram of the calibration system.

Control block provides three main tasks: sensing the FDDA output differential voltage, evaluating the difference between these voltages and finally, generating the control clock signals CLK_{MAIN} and CLK_{AUX} for the main and correction parts of the calibration system.

Fig. 2 shows that the input comparator senses the FDDA output voltage offset through the voltage signals $OUT+$ and $OUT-$. At the beginning of the first cycle, the comparator sets its output to the value of logic 0 by comparison condition. The Q outputs of DFF_1 and DFF_2 are set to the value of logic 1 by initial RST signal. Then, the Q output of DFF_2 is redundantly set (for this time) to the value of logic 1 by delayed NXOR gate. Finally, when the main calibration cycle is finished, the Q output of DFF_2 is flipped to the value of logic 0 by rising edge of the signal from the inverter and grounded D input. Clock signal CLK_{MAIN} controls the main part of calibration circuit and CLK_{AUX} is static during this cycle.

Secondly, correction cycle starts at the moment when the main cycle is finished and comparator flips its output to logic 1. The rising edge of this change sets the Q output of DFF_1 to the value of logic 0 by grounded D input. In this moment, clock signal CLK_{MAIN} is gated and it remains in the state of logic 1. Again, the Q output of DFF_2 is set to the value of logic 1 by delayed NXOR gate and clock signal CLK_{AUX} starts to control the correction part of the calibration circuit.

When the comparator flips its output to the value of logic 0 again, Q output of DFF_2 flips to the logic 0, the CLK_{AUX} is also gated and the second, correction calibration cycle is finished. The overall process of calibration is completed in this way.

Fig. 2: Schematic diagram of the control block.

Counters and **DACs** cooperate on injecting the correct current values into branches of the FDDA input difference pair. The most important parameter of these circuits is the resolution. Resolution can be ideally expressed as follows [?]:

$$Resolution = \frac{FullScale}{1.LSB} \leq \frac{V_{IN_offset_uncomp}}{V_{IN_offset_comp}} \quad (1)$$

Fig. 3: DAC in the correction part of the calibration circuit.

where $V_{IN_offset_uncomp}$ and $V_{IN_offset_comp}$ are the input offset voltage of the FDDA before and after the calibration process takes, respectively. In this work, the resolution of the counter and DAC used in the main part of the calibration circuit is 10 bits, and the correction part contains 7-bit circuits. DACs comprises of the M2M transistor network and transmission gates (or so-called T-gates). Fig. 3 shows the DAC implemented in the correction part. The active loads that set the value of individual current branches are formed by PMOS transistors of the same dimensions. The output currents from the DAC I_{COMP+} and I_{COMP-} are the result of the sums of the currently closed T-gates, which are controlled by the output bus of the counters (7-bit or 10-bit).

Connection of the DAC to the FDDA is shown in Fig. 4. Current mirrors based on PMOS transistors connected by bulk-driven (BD) technique are used to mirror the output current from the DAC to the FDDA input difference pair.

Fig. 4: Compensation configuration of DAC output and FDDA.

Fig. 5 shows the topography of the proposed digital calibration system. The area of calibration circuitry itself is marked there (by yellow).

Fig. 5: Topography of the proposed digital calibration system.

IV. VERIFICATION

The proposed method of digital calibration was implemented in selected process and the calibrated system is currently under fabrication. The designed system was verified through extensive simulations considering the industrial range of temperatures from -20°C to $+85^{\circ}\text{C}$. Simulation verification included Monte Carlo (MC) analysis, Process corner analysis and Reliability analysis, which investigates drift of IC parameters during its lifetime [?].

Figure 6 shows boundary cases of process corners analysis for residual voltage offset at the output V_{OUT_offset} . One can observe the FDDA output voltage in the sequential calibration process. After the calibration cycle is finished, the FDDA is initiated for the proper operation (function mode). Its input is fed with differential harmonic signal with a peak-to-peak amplitude of $200\text{ }\mu\text{V}$. The output signal amplitude goes up

to 290 mV. This reveals a voltage gain of 63 dB, which is in correspondence with FDDA's nominal design. The residual offset output voltage of the FDDA after calibration reaches 10 mV at highest, which represents the input offset voltage V_{IN_offset} approximately of 10 μV . These results prove that the target of calibration was successfully met.

Fig. 6: The process of digital calibration in boundary cases of fabrication technology and temperature variations.

Figure 7 displays results of reliability analysis of calibration process applied to the FDDA output voltage. For this purpose, RelXpert engine of Cadence environment was used. This analysis calculates a drift of IC parameters over 10 years of operation mainly due to ageing of material structures, and electrical stress (Hot carrier injection [?], and Bias temperature instability [?], [?]). One can easily observe shortening in duration of aged IC calibration cycle. This in turn, deteriorates resolution that the offset voltage is compensated with. Therefore, the V_{IN_offset} is supposed to rise from 2.4 μV to 10 μV . When the calibrated FDDA is initiated to the proper function, the drift of V_{IN_offset} is obviously negligible according to differential output signals (see Figure 7).

Fig. 7: Reliability analysis of drift in process of calibration cycle over 10 years of operation.

The plot in Figure 8 displays voltage gain of the digitally calibrated FDDA in best, typical and worst cases obtained through Corner analysis, considering industrial range of temperatures. The tight variations in FDDA's frequency spectrum key characteristics proves fair efficiency of the proposed calibration method.

Fig. 8: Voltage gain of digitally calibrated FDDA in corners of process and temperature variations.

Figure 9 displays the statistical results of Monte Carlo analysis aimed at FDDA's V_{IN_offset} . The two histograms compare the FDDA input offset voltage with and without the use of digital calibration. It is rather observable that the implemented calibration significantly improves the distribution of samples. The mean value is reduced by more than 2500 times and standard deviation is reduced by tremendous 13500 times.

Table I compares key parameters of digitally calibrated FDDA, designed and implemented in our work, to other works, where different calibration techniques are used. They include digital and analog methods of calibration and Chopper stabilization. The presented statistical results were obtained from 100 samples of Monte Carlo simulation considering temperature of 27 $^{\circ}C$, process variations and device mismatch.

The main principle of operation significantly differs between calibration methods such as Chopper stabilization and digital method. In order to maintain the relevance of comparison, it is important to establish a condition that is common for compared methods. For this purpose, we restricted the total harmonic distortion (THD) of calibrated amplifier's output signal to 1%. Likewise, it is mandatory to take more key parameters of the system into account as compared calibration methods substantially differ in principle of operation. Therefore, we established so-called figure of merit (FOM), which is based on the following equation:

$$FOM = k_A(V_{IN_OFF_R} \cdot A_C \cdot P_C)^{-1}, \quad (2)$$

where $V_{IN_OFF_R}$ is residual input offset voltage of the calibrated amplifier, A_C and P_C are die area and power consumption of calibration circuits, respectively. The whole

TABLE I: Comparison of key parameters of the proposed calibration method to other works.

		This work		[?]	[?]	[?]	[?]	[?]	[?]	[?]
		μ	σ							
Year		2021		2015	2008	2008	2010	2010	2013	2008
Technology	[nm]	130		130	350	180	130	130	130	700
V_{DD}	[V]	0.4 - 0.6		1.2	1	1.8	1.2	1.2	2.8	5
A_A ¹⁾	[.10 ³ μm ²]	115		12.3	224	36	243	34	630	3325
A_C ²⁾	[.10 ³ μm ²]	43		12.3	17.4	30	95	33.2	261	475
P_A ¹⁾	[μW]	13.3	2.7	14000 ³⁾	8000 ³⁾	11000 ³⁾	52800	2000	160000 ³⁾	2800
P_C ²⁾	[μW]	6	1.2				3600	2400		
V_{IN_OFF}	[μV]	4.3	11.1	5	538	126	-	75	0,097	μ=1,81 σ=0,67
FOM	[—]	2254		120[†]	1.4	2.4	-	17[†]	25[†]	12[†]
Source of results		Sim.		Meas.	Sim.	Meas.	Meas.	Meas.	Meas.	Meas.
Calibration method		Dig.		Analog.	Analog.	Dig.	Dig.	Analog.	Dig.	Chop.

¹ The die area (A) and power consumption (P) of FDDA.

² The die area (A) and power consumption (P) of calibration circuits.

³ These works mention only overall chip area, they do not separate amplifier and calibration circuits.

[†] These works does not mention THD. The comparison of FOM is therefore not fully relevant.

Fig. 9: Monte Carlo analysis of V_{IN_offset} in non-calibrated FDDA and digitally calibrated FDDA.

index is inverted in order to tie it proportionally to the performance of calibration method and it is scaled by k_A .

It can be observed from Table I that the die area of the proposed calibration solution belongs into lower range among

the compared works. The presented digital calibration exhibits the lowest power consumption of less than 10 μW with gaping difference to other works. Also the V_{IN_offset} of the digitally calibrated FDDA reaches fairly good values. The high and robust performance, proved by presented results, is emphasized with FOM parameter (according to 2). The presented digital calibration reaches, in terms of this index, value over 2200 in comparison to the other works reporting value of tens to hundreds. While the works [?] and [?] provide better compensation of V_{IN_offset} , it comes at the cost of enormous die area or power consumption of calibration circuits.

V. SUMMARY AND CONCLUSION

In this work, the design of the calibration circuit for the FDDA was realized in 130 nm CMOS technology. Its primary task is to suppress the effect of fluctuations of FDDA parameters caused by the variations in manufacturing process parameters, temperature and time-dependent drift over IC lifetime. To ensure the lowest possible power consumption and sensitivity of calibration hardware to imperfections of the manufacturing process, a digital algorithm has been implemented. The algorithm works in two cycles - the main calibration cycle and the correction calibration cycle. Therefore, the proposed circuit consists of three main parts: control block, the main calibration part and the correction calibration part. For efficient application of the calibration circuit to the ultra-low voltage FDDA, its outputs have been designed as bulk-driven current mirrors.

The presented results were acquired through process corners analysis, Monte Carlo analysis and reliability analysis. Based

on obtained results, it can be stated that the digital calibration has high potential. Firstly, after the completion of both FDDA calibration cycles, it was observed that the differential harmonic signal with a peak-to-peak amplitude of $200\ \mu V$ was amplified to a pure signal with an amplitude of $290\ mV$ at $63\ dB$ gain - the nominal value of FDDA gain. In this case, the output offset voltage was at most $10\ mV$, which means that the input offset voltage reached approximately $100\ \mu V$. Secondly, the calibration circuit is also highly resistant to ageing - after simulated 10 years of voltage stress and ageing, the FDDA was calibrated accurately, which proves the reliability of calibration circuit. Thirdly, after the calibration process, FDDA DC gain acquired through Corner analysis reaches $58\ dB$ in worst case and $65\ dB$ in best case. Finally, the great benefit of this circuit lies not only in its reliability and accuracy but also in ability to work under ultra-low supply voltage: in the range of $0.4 - 0.6\ V$, and it occupies small die area on chip: $43.10^{-3}\ \mu m^2$, and exhibits low power consumption: $6\ \mu W$ (μ) and $1.2\ \mu W$ (δ).

All the results, presented in this work were acquired from simulations, while the designed system is currently under fabrication. The experimental measurements will take place in near future in order to validate presented results. The proposed method will be experimentally evaluated by measurements of the prototyped chips within next few months.

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REFERENCES

- [1] R. R. Tummala, "Moore's law for packaging to replace moore's law for ics," in *2019 Pan Pacific Microelectronics Symposium (Pan Pacific)*, 2019, pp. 1–6.
- [2] D. Arbet, M. Kováč, V. Stopjaková, and M. Potočný, "Bulk-driven fully differential difference amplifier for ultra-low voltage applications," in *2018 41st International Convention on Information and Communication Technology, Electronics and Microelectronics (MIPRO)*, 2018, pp. 0093–0098.
- [3] D. Arbet, G. Nagy, V. Stopjaková, and M. Kováč, "Digital offset calibration of an opamp towards improving static parameters of $90\ nm$ cmos dac," *Radioengineering*, vol. 23, pp. 931–938, 2014.
- [4] T. McConaghy, K. Breen, J. Dyck, and A. Gupta, *Variation-aware design of custom integrated circuits: a hands-on field guide*. Springer Science & Business Media, 2012.
- [5] A. Gupta, C. Gupta, H. S. Jatana, and A. Dixit, "Investigation of hot-carrier degradation in $0.18\text{-}\mu m$ mosfets for the evaluation of device lifetime and digital circuit performance," *IEEE Transactions on Device and Materials Reliability*, vol. 19, no. 4, pp. 609–614, Dec 2019.
- [6] B. Ullmann, M. Jech, K. Puscharsky, G. A. Rott, M. Walzl, Y. Illarionov, H. Reisinger, and T. Grasser, "Impact of mixed negative bias temperature instability and hot carrier stress on mosfet characteristics—part i: Experimental," *IEEE Transactions on Electron Devices*, vol. 66, no. 1, pp. 232–240, 2019.
- [7] D. K. Schroder, "Negative bias temperature instability: What do we understand?" *Microelectronics Reliability*, vol. 47, no. 6, pp. 841 – 852, 2007, modelling the Negative Bias Temperature Instability. [Online]. Available: <http://www.sciencedirect.com/science/article/pii/S002627140600374X>
- [8] Y. Zhang, Y. Fei, Z. Peng, and F. Huang, "A $250\ mhz$ $60\ db$ gain control range $1db$ gain step programmable gain amplifier with dc-offset calibration," in *2015 International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS)*, Nov 2015, pp. 227–230.
- [9] P. Mak, S. U., and R. P. Martins, "On the design of a programmable-gain amplifier with built-in compact dc-offset cancellers for very low-voltage wlan systems," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 2, pp. 496–509, March 2008.
- [10] Z. Cheng and J. Bor, "A cmos variable gain amplifier with dc offset calibration loop for wireless communications," in *2006 International Symposium on VLSI Design, Automation and Test*, 2006, pp. 1–4.
- [11] H. Shih, C. Kuo, W. Chen, T. Yang, and K. Juang, "A $250\ mhz$ $14\ db-nf$ $73\ db$ -gain $82\ db$ -dr analog baseband chain with digital-assisted dc-offset calibration for ultra-wideband," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 2, pp. 338–350, Feb 2010.
- [12] Xiaojie Chu, Min Lin, Zheng Gong, Yin Shi, and Fa Foster Dai, "A cmos programmable gain amplifier with a novel dc-offset cancellation technique," in *IEEE Custom Integrated Circuits Conference 2010*, 2010, pp. 1–4.
- [13] S. Li, J. Li, X. Gu, H. Wang, M. Tang, and Z. Zhuang, "A continuously and widely tunable $5\ db$ -nf $89.5\ db$ -gain $85.5\ db$ -dr cmos tv receiver with digitally-assisted calibration for multi-standard dbs applications," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 11, pp. 2762–2774, Nov 2013.
- [14] J. F. Witte, K. A. A. Makinwa, and J. H. Huijsing, "A cmos chopper offset-stabilized opamp," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 7, pp. 1529–1535, 2007.