



Satellite Instrument Control Unit with Artificial Intelligence engine on a Single Chip

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Current GPUs Application Scenarios





High parallelism application (AI, Sensor fusion, computer Vision, gaming, etc...)



High Performance Computing (Data Centre, mining)



Ad-hoc software for high level complex developments (e.g., CUDA, ROCm)



https://www.mordorintelligence.com/industry-reports/graphic-processors-market













Edge Hardware Accelerators





Movidius Myriad X, VPU (Intel)



Jetson Nano, GPU (NVIDIA)



In the latest years several companies have developed **dedicated COTS HW accelerators** for AI/ML algorithms. These solutions allow an easy development via their dedicated framework, but they lack of modularity and reconfigurability.

PROs	CONs
Good performance	No radiation tollerant
Dedicated Framework	No reconfigurable
Fast developing time	



What if an GPU would run on FPGAs?



Large and growing technology availability:

- Long lifespan: up to 20 years industrial grade*
- Radiation hardening
- Full European devices
- Low Power devices (Design dependent)

Low effort for new technologies: once a new FPGA is out, only bitstream generation required!

Integrability on a System on Chip with CPUs, Communication modules, etc...

Integrable in existing FPGA-Based board

Dynamic reconfiguration

* https://www.xilinx.com/support/quality/reliability.html#reliabilityEstimator





ICU4SAT



ICU4SAT aims at changing the rules of image handling & processing on-board satellites.

- Innovative fully programmable data handling & data processing SoC.
- Analyse and process on-board data acquired through AI and computer vision algorithms.
- Automatically discharge unwanted data and transmit only the meaningful ones.
- Re-configurable, to allow for the repurposing of earth observation missions with no need to launch new satellites as monitoring need change, even temporarily.

<u>3 Open-source/hardware innovative Components</u>

- **RISC-V** (Command & control platform)
- soft-GPU (HW accelerator for computer vision & AI)
- **SpaceFibre Interface** (High speed interface for satellite OBDH)







RISC-V is a free and open ISA enabling a new era of processor innovation through open standard collaboration, experiencing rapid uptake in both industry and academia. It is based on the fifth generation of RISC design from UC Berkeley.

ICU4SAT will mount the CVA6 (Ariane) RISC-V processor:

- 64-bit RISC-V ISA, Open Source.
- Provided by OpenHW group
- 6-stage, single issue, in-order CPU
- It fully implements I, M, A and C extensions
- Three privilege levels M, S, U to fully support a Unix-like operating system (Linux capable).

https://github.com/openhwgroup/cva6





nnnn



soft-GPU is a soft GPU-like architecture for FPGAs. It can be programmed using OpenCL and TensorFlow kernels. Its HW configuration can be customized according to application needs.

- Portable, scalable and flexible. Dynamically HW Reconfigurable
- Multiple-Thread (SIMT) processor developed in VHDL
- Power savings between 3.2x and 4.5x, with respect to NEON ARM extension
- Speedups between 10.6x and 48.5x, with respect to NEON ARM extension
- Area overhead between 3.0x and 17.7x.









Candidate as Next-gen Satellite OBDH high speed protocol

- Open Protocol developed under supervision of ESA
- Standardisation process ended in May 2019
- Meant to be used for Very high speed (up to 100Gbps) satellite On-Board Data-handling
- Full HDL implementation, with AXI Slave I/F
- Built-in Quality of Service, Fault Detection Isolation & Recovery.
- Overcome limitations, e.g., Bandwidth, Flexibility, etc., of State-of-the-art solutions



Space



ICU4SAT – Software Architecture





ICU4SAT SoC ←

ICU4SAT software is composed by a compiler (based on LLVM), dedicated to the generation of the soft-GPU executable kernels, and a development tool, offered to end-users for deploying new applications

- FrontEnd, dedicated to parse the high-level programming languages code
- **Optimiser**, dedicated to improve the code and simplify the operations
- **BackEnd**, dedicated to translate and adapt the optimized code for the target hardware
- **Skeleton code**, dedicated to reduce the effort required to develop a new application on the ICU4SAT







ICU4SAT HW design is **totally described in HDL**.

This allows the HW developer to **customize**, add, and **improve**, the HDL in case some operations are missing or should be optimized.

This high flexible solution makes ICU4SAT very interesting both for those who want to **use it as it is** and for those who are interested in strongly customizing it.



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Innovation of ICU4SAT system



Modularity



FPGAs allow to **partially re-configure** the soft-GPU, by adding or removing dynamically different IP cores.

For example, in case the users will not need SpaceFibre/SpaceWire as communication module, they shall remove and/or include their IP communication modules.

Furthermore, the possibility of **commercializing** the single IP core allows interesting collaboration with big space system integrators, which can be interested only in the soft-GPU accelerator.





Customizability



Opposite to the dedicated HW accelerators developed on top of FPGA, the **soft-GPU** has its own **developer workflow**.

High-level framework for AI applications have simplified the developing of these algorithms, making the developers life very simple.

Basic preliminary framework, which will be improved and maintained to be compatible with the standard frameworks already available, is provided to **port** and **run computer vision** and **AI algorithms** directly on the ICU4SAT system.



Innovation of ICU4SAT system



On-board design



The new satellites era is characterized by a **strong use of AI algorithms** for the post-processing of data on ground.

This process requires to download the data acquired by on-board sensors before processing it, even when it is not relevant for the mission or not usable.

Thanks to the **soft-GPU of ICU4SAT**, part of the **processing** can be **shifted** from ground **to edge**, relaxing bandwidth, and storage pre-requisites. The soft-GPU can execute computer vision kernels, leading to **improvements in the standard algorithms run on-board satellite**, i.e., optical flow, re-binning, etc.



Preliminary results





soft-GPU speedup over ARM Cortex-A9 Dual Core processor when 8 CUs are synthesized.

Maximum, minimum, and the average speedup for different problem sizes ranging from **256** to **256K** are reported

For some kernels, a minimum problem size is required to achieve a positive speedup for the soft-GPU.

soft-GPU speedup over the MicroBlaze according to the number of CUs synthesized. The reported speedup is the **average speedup** over different problem sizes ranging from 256 to 256K. **Higher the number of CUs, the better**.









THANK YOU FOR LISTENING



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