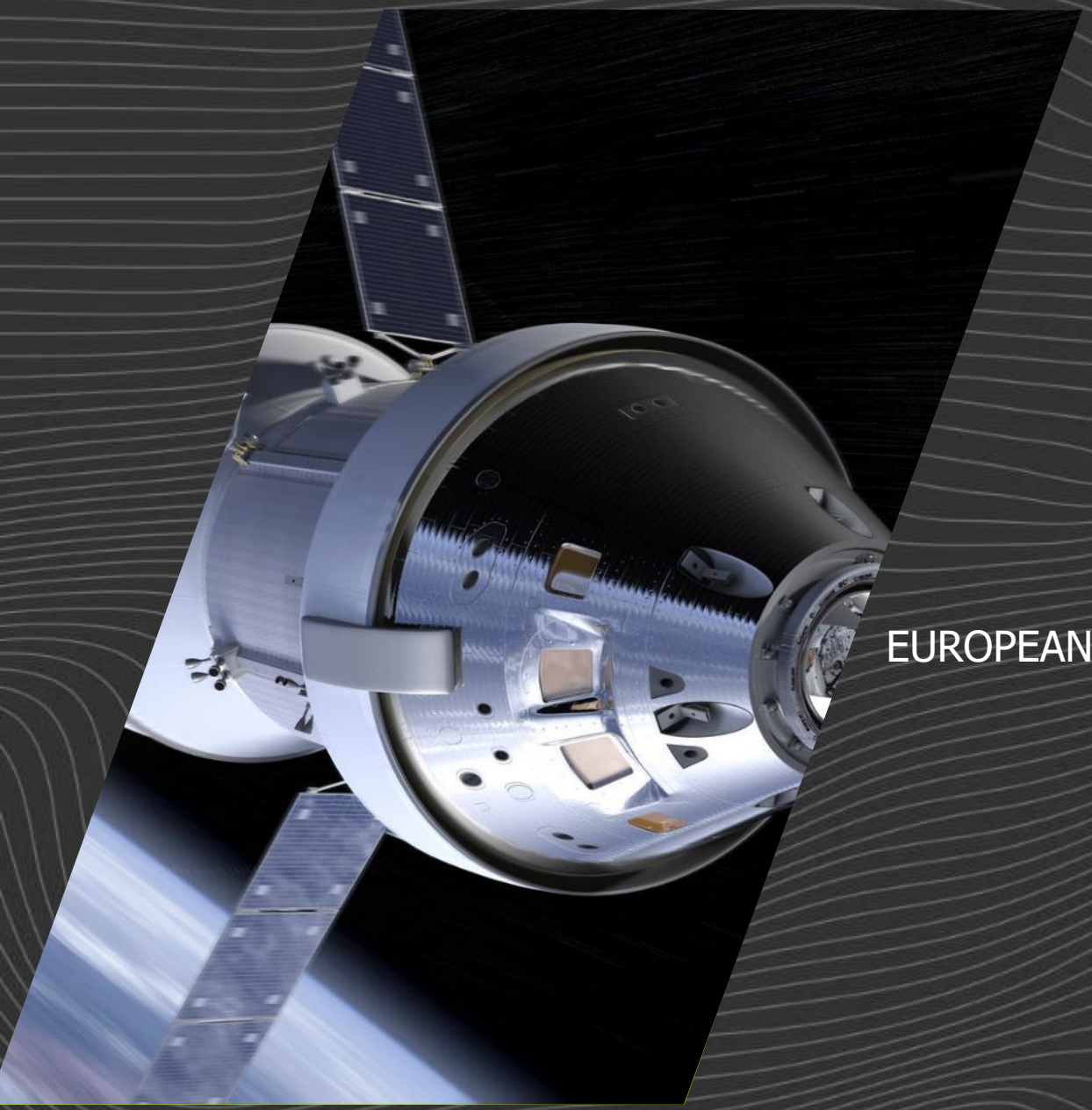


CAES PIONEERING ADVANCED ELECTRONICS

GR740 SINGLE BOARD COMPUTER

EUROPEAN WORKSHOP ON ON-BOARD DATA PROCESING (OBDP2021)

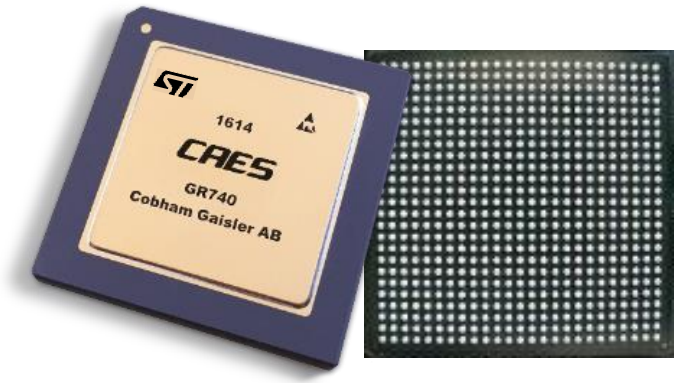
16 JUNE 2021

Agenda

- Development introduction
- HW overview
- Compact PCI Serial Space
- HW design description
- SW description
- Summary

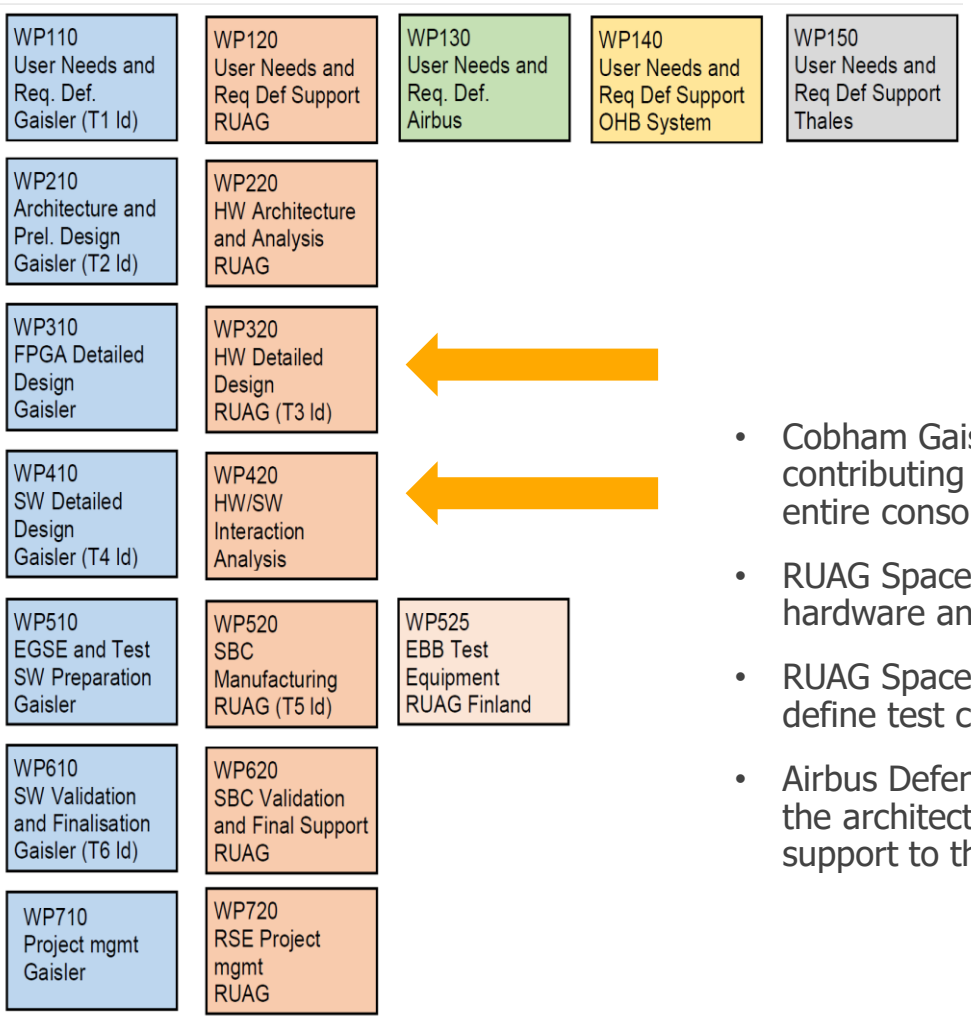
GR740 SBC activity

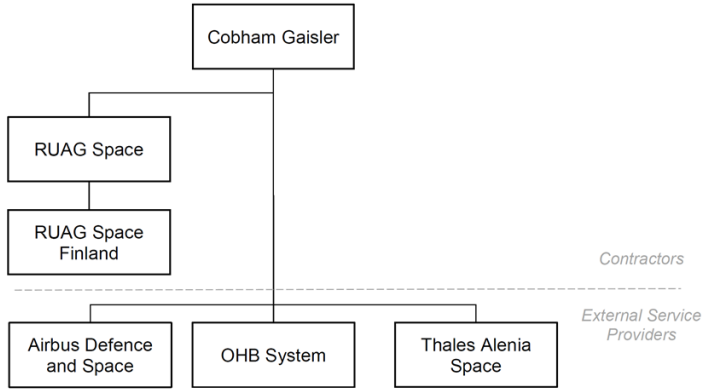
- ESA activity “Reference Design and Basic Software for a Single Board Computer based on GR740”
- Main objectives
  - To create a reference design, available to all European space users, a single board computer using the GR740
  - Reference design data package
  - Development of Elegant Breadboard
  - Verified at functional and performance level (TRL 4)
  - Supported by a Qualification Test Plan
  - Supported by boot software, device drivers and test application software



Overview of the GR740 SBC activity

Work to be carried out





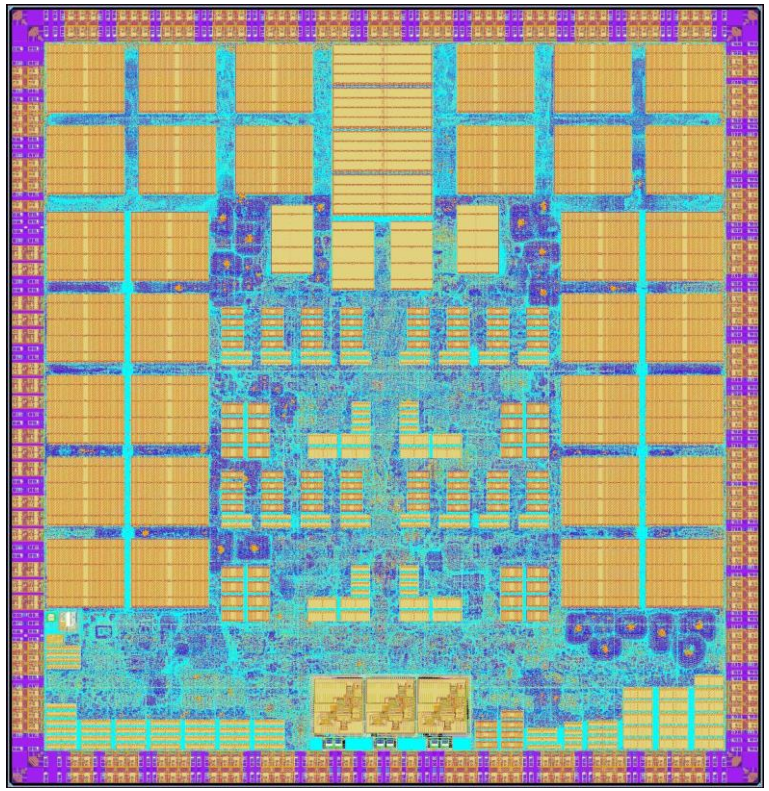
- Cobham Gaisler - responsible for the overall activity, the software design and the FPGA design, as well as contributing to the system architecture and hardware design and analyses; project management of the entire consortium.
- RUAG Space in Sweden - responsible for the hardware design and validation, and for significant parts of the hardware analyses.
- RUAG Space in Finland - responsible for defining and specifying the in-house EBB Test Equipment and to define test cases and supervise the manufacturing of the Test Equipment.
- Airbus Defence and Space, OHB System and Thales Alenia Space - input provided to the requirements and the architecture of the GR740 SBC: general features, form factors and hardware and software aspects; support to the overall plans focusing on interfaces and risk assessments, and participation in the SRR.

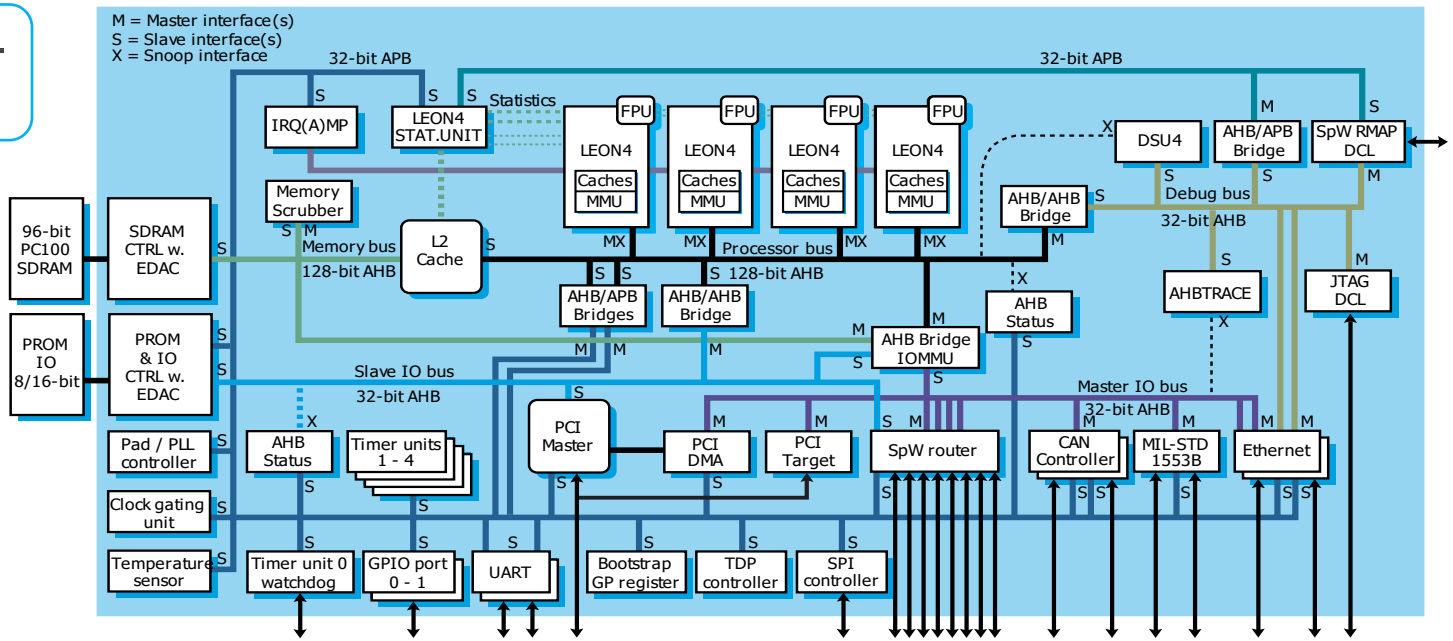
Agenda

- Development introduction
- HW overview
- Compact PCI Serial Space
- HW design description
- SW description
- Summary

Introduction to GR740

Rad-hard system-on-chip quad-core fault-tolerant LEON4FT SPARC V8 processor





Cobham Gaisler digital IP: LEON4FT and IO peripherals

STMicroelectronics C65SPACE technology platform

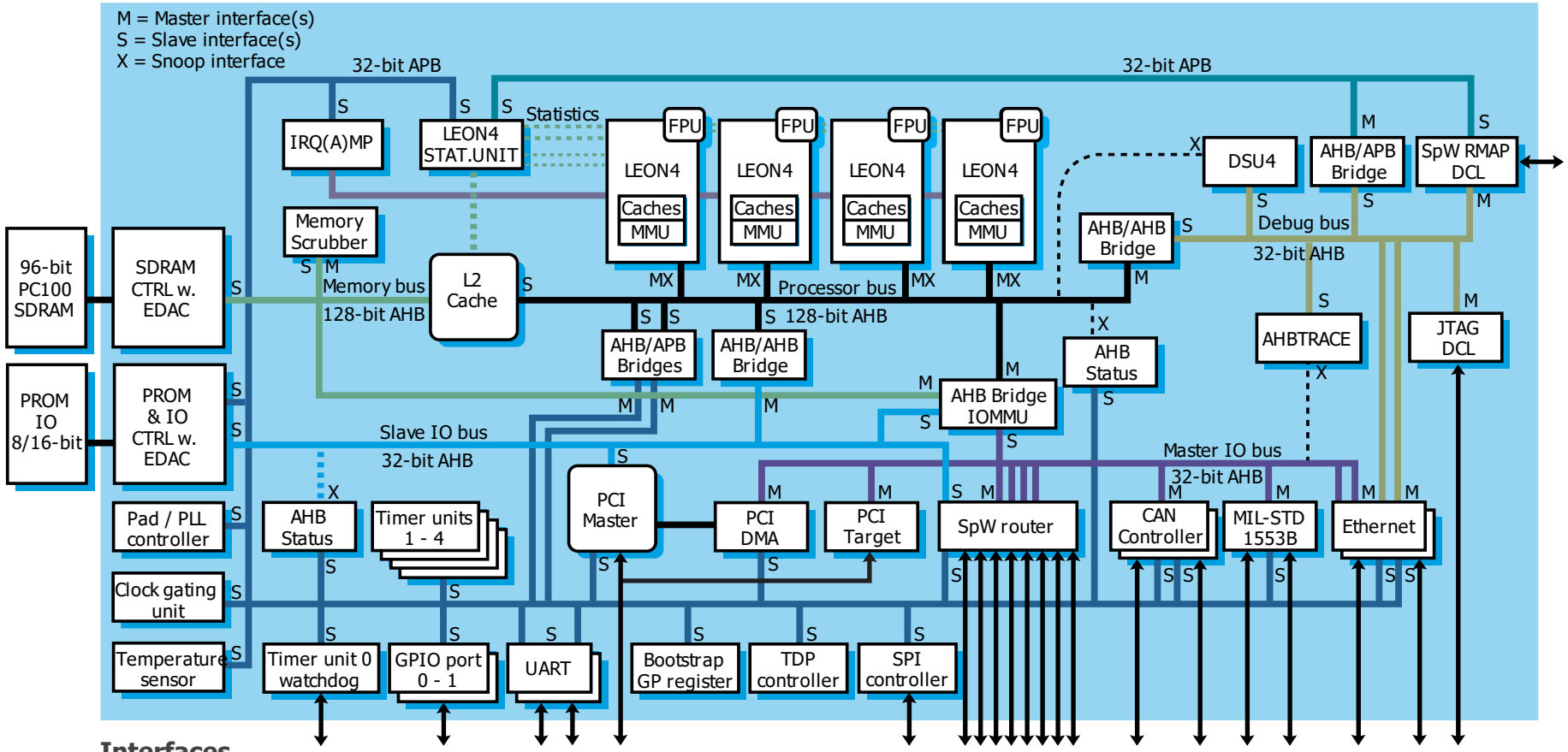
Complete software toolchain and debuggers are available

http://www.gaisler.com/GR740

GR740

Features

- Fault-tolerant quad-processor SPARC V8 integer unit with 7-stage pipeline, 8 register windows, 4x4 KiB instruction and 4x4 KiB data caches
- Double-precision IEEE-754 FPU (1 FPU/Core)
- 2 MiB Level-2 cache
- 64-bit PC100 SDRAM memory interface with Reed-Solomon EDAC
- 8/16-bit PROM/IO interface with EDAC
- CPU and I/O memory management units
- Multi-processor interrupt controller with support for asymmetric and symmetric multiprocessing
- SpaceWire TDP controller and support for time synchronisation

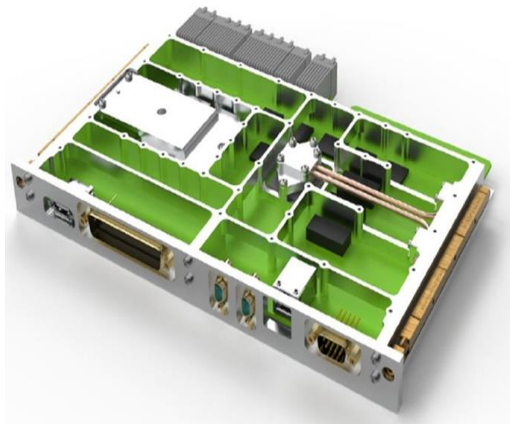


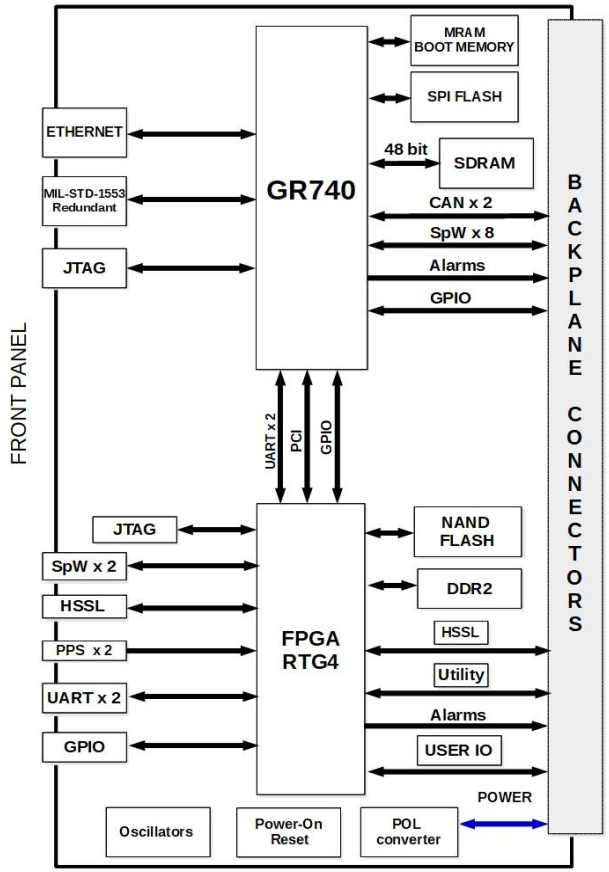
Interfaces

- SpaceWire router with 8 SpaceWire links (200 MHz)
- 2x 10/100/1000 Mbit Ethernet interfaces
- 2x MIL-STD-1553B interface
- 2x CAN 2.0 controller interface
- 2x UART, SPI, Timers and watchdog, 16+22 pin GPIO
- PCI Initiator/Target interface
- JTAG

GR740 Single Board Computer
HW Overview – expected final platform features

- A high-performance Single-Board Computer based on Cobham Gaisler GR740 quad-core 32-bit LEON4FT SPARC V8 processor and Microsemi RTG4 radiation tolerant FPGA.
- The SBC provides an extensive set of memories and redundant interfaces to support the needs of current and future OBC and Data Handling platforms.
- Features
  - Implemented following the Compact PCI Serial Space backplane standard (CPCI-S.1 R1.0)
    - Dual star, eight SpaceWire interfaces from GR740
    - Multi drop bus, redundant CAN from GR740
    - Full mesh, HSSL (SpFI) from RTG4
    - Multi drop bus, I2C from RTG4
    - Alarms and other utility signals
  - On-board memory
    - SDRAM interfaced with GR740, 512 MIB of accessible data RAM plus ECC check bits
    - Parallel Boot MRAM, 64 KiB interfaced with GR740
    - SPI Flash memory, 32 MiB interfaced with GR740
    - 3D-PLUS NAND FLASH, 8 GiB interfaced with RTG4
    - 3D-PLUS DDR2, 512 MiB of accessible data RAM plus ECC check bits interfaced with RTG4
  - PCI, UART and GPIO interface between GR740 and RTG4
  - Interfaces at front edge of board:
    - Redundant MIL-STD-1553B
    - 2 x SpaceWire
    - Gigabit Ethernet
    - General purpose I/O's
    - PPS (Pulse Per Second) input for synchronization (SMB)
    - UART/JTAG debug interfaces
  - Form factor
    - 6U (233.5 mm x 160 mm), 5 HP. Mass 1.2 kg (estimate)
  - Power consumption: ~30 W (estimate)
- SBC included with DDR2, NAND FLASH and HSSL as extensions





Agenda

- Development introduction
- HW overview
- Compact PCI Serial Space
- HW design description
- SW description
- Summary

Compact PCI Serial Space

CPCI-S.1 R1.0

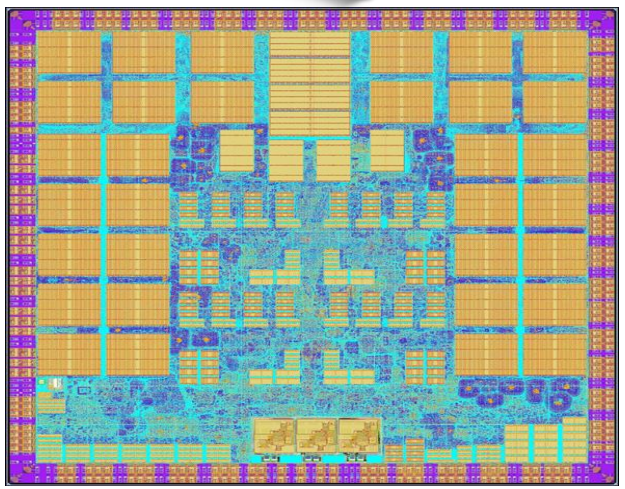
- The GR740 SBC is implemented following the Compact PCI Serial Space backplane standard (CPCI-S.1 R1.0)
  - The form factor of the board is 6U (233.5 mm x 160 mm)
  - Slot width of 5 HP and an estimated mass of 1.2 kg
  - The SBC can be tailored to fit into the system or payload slot as in the CPCI-S.1 standard
- The SpaceVPX and CPCI Serial Space (CPCI-S.1) both the standards provide necessary features like
  - modular redundancy
  - redundant interfaces
  - support the needs of current and future platforms
- The selection of backplane should follow an agreed standard developed for space applications and that is widely adopted by the European space industry.
  - The GR740 SBC will follow the conclusion of ADHA/backplane workshop results which has support from all the major European space industry
- To list the features of the CPCI-S.1
  - Simple with features necessary for space industry
  - Derived from a successful non-space backplane standard
  - Backplane solution with possibility for interoperability between different vendors
  - Support for SpaceWire
  - European Industry support

Agenda

- Development introduction
- HW overview
- Compact PCI Serial Space
- HW design description
- SW description
- Summary

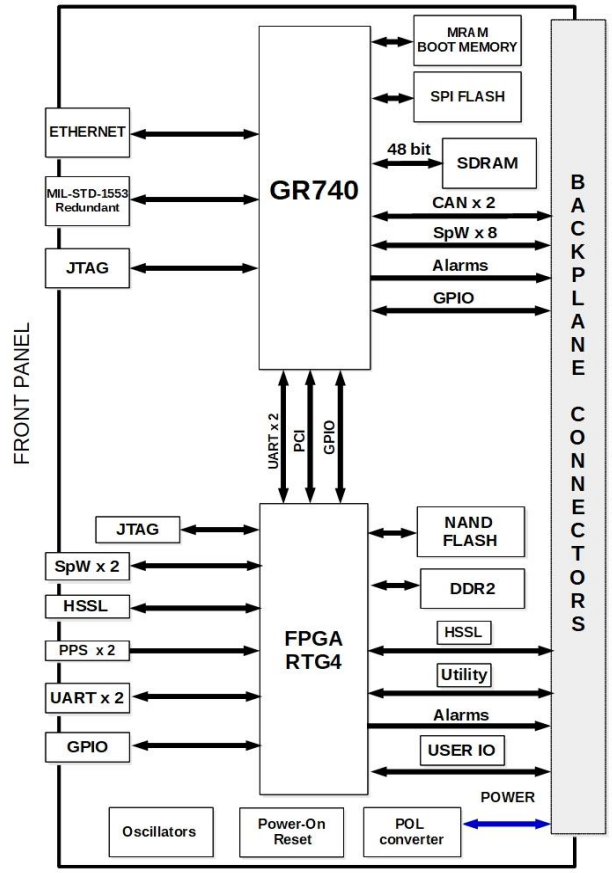
GR740 Single Board Computer
Processing capability

- A high-performance Single-Board Computer based on Cobham Gaisler GR740 quad-core 32-bit LEON4FT SPARC V8 processor and Microsemi RTG4 radiation tolerant FPGA.
- **Processing capability**
  - **GR740 radiation-hard system-on-chip**
    - Fault-tolerant quad-processor SPARC V8 integer unit with 7-stage pipeline, 8 register windows, 4x4 KiB instruction and 4x4 KiB data caches
    - Double-precision IEEE-754 floating point units
    - 2 MiB Level-2 cache
    - System frequency: 250 MHz
    - The GR740 processors run at 250 MHz nominal frequency and each processor provides 459 Dhrystone MIPS (or DMIPS) per core, which gives 1.84 DMIPS/MHz
  - **Microsemi RTG4 radiation tolerant FPGA**
    - To create a versatile and competent SBC design, the high-end Microsemi RTG4 FPGA has been chosen
      - To implement glue logic and additional required interfaces
      - Application specific developments and implementation of accelerator functions
    - The RTG4 brings the DDR2 memory and high-speed serial link (HSSL) capability to the SBC
    - The glue-logic required to be compatible with the CPCI-S.1 R1.0 standard are also implemented in the FPGA
    - Maximum logic elements (LUT4 + TMR flip-flop) 151,824
    - Total SRAM 5.2 Mbits
      - More than 70 % of the FPGA resources are available for user defined functic
    - Mathblocks (18-bit × 18-bit) 462
    - uPROM 374 Kbits
      - All FPGA resources are available for user defined functions



GR740 Single Board Computer
On-board Memory

- Memory interfaced with GR740
  - Parallel Boot MRAM
    - 64 KiB interfaced with GR740 (possible to increase MRAM size to 128 KiB)
    - Considering pin sharing between MIL-STD-1553B, CAN, UART and the PROM interface in GR740
  - Application storage
    - SPI Flash memory, 32 MiB interfaced with GR740
  - Volatile (working memory) SDRAM to execute application software and operating system software
    - 512 MIB of accessible data RAM plus ECC check bits
    - The PCI interface on GR740 is pin shared with SDRAM memory interface.
    - Since PCI is used to interface with FPGA only half 48 bits of the available 96 SDRAM data bits are used for memory interface
- Memory interfaced with RTG4
  - Platform Data Storage for non-volatile storage of data
    - 3D-PLUS NAND FLASH, 8 GiB interfaced with RTG4
  - Volatile (working memory) for the user defined FPGA based functions
    - 3D-PLUS DDR2, 512 MiB data RAM plus ECC check bits interfaced with RTG4



GR740 Single Board Computer
Interfaces

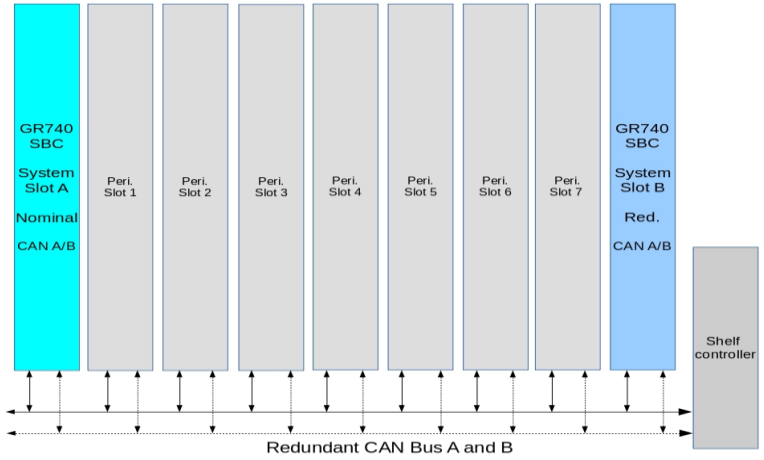
- Redundant MIL-STD-1553 Bus Controllers for communication with spacecraft platform and payload equipment
- 10 x SpaceWire interfaces for communication with spacecraft platform and payload equipment
- CAN Bus Controllers for communication with spacecraft platform and payload equipment
- 2x UARTs for communication with platform legacy sensors and actuators
- 8 x HSSL (SpFi) Controllers for communication with spacecraft platform and payload equipment
- GPIO for low speed signaling with spacecraft functions
- Ethernet/UART Debug Support Unit control I/F for test purposes
- JTAG for test and debug purposes
- Reserved user IO and utility interfaces
- PPS (Pulse Per Second) input for synchronization

GR740SBC Interface	Type	Redundancy offered	Possible use
SpaceWire (Backplane)	Point to Point	Eight interfaces from the backplane.	To realize dual star command and control interface through the backplane module. Useful to communicate within a unit.
SpaceWire (Front panel)	Point to Point	Two interfaces from the front panel.	1.) As cross strapped interfaces between redundant units. 2.) To communicate with external instruments, possible to cross strap since two interfaces are provided.
CAN	BUS	Redundant bus from the backplane.	1.) To realize command and control interface bus through the backplane module. Useful to communicate within a unit.
MIL-STD-1553	BUS	Redundant bus from the front panel.	1.) As communication interface between redundant units. 2.) To communicate with external instruments.
UART	Point to Point	Two interfaces from the front panel.	1.) As cross strapped interfaces between redundant units. 2.) To communicate with external instruments, possible to cross strap since two interfaces are provided.
HSSL (supported by RTG4, SpFi)	Point to Point	Eight interfaces from the backplane possible.	To realize a full mesh data communication between every modules on the backplane.

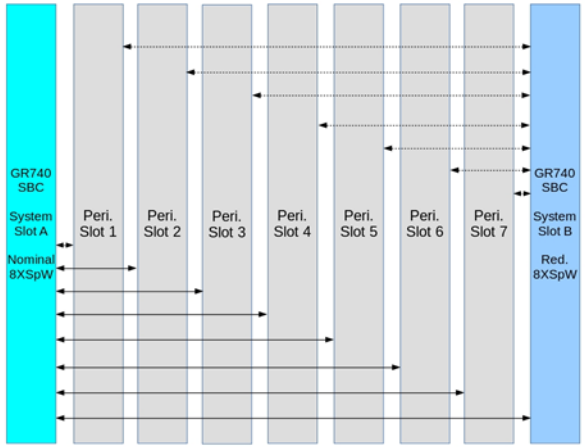
GR740 Single Board Computer
Backplane electrical interconnects

BP interface routing topology	GR740SBC Interface	Comments
Dual star	SpaceWire	Point to Point, eight interfaces from GR740
Multi drop bus	CAN	BUS, Redundant CAN from GR740
Full mesh	HSSL	Supported by RTG4 (SpFI)
Multi drop bus	I2C	BUS, I2C from RTG4

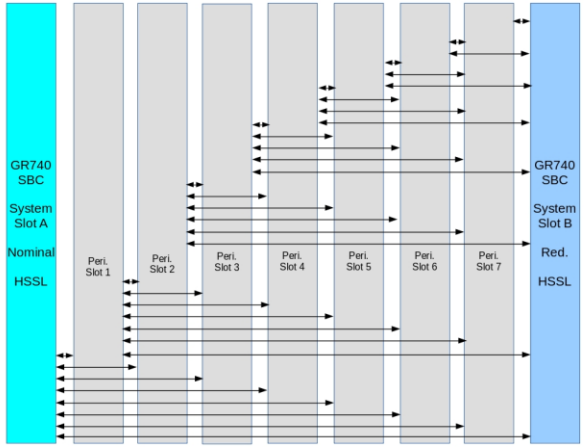
- Multi drop CAN bus

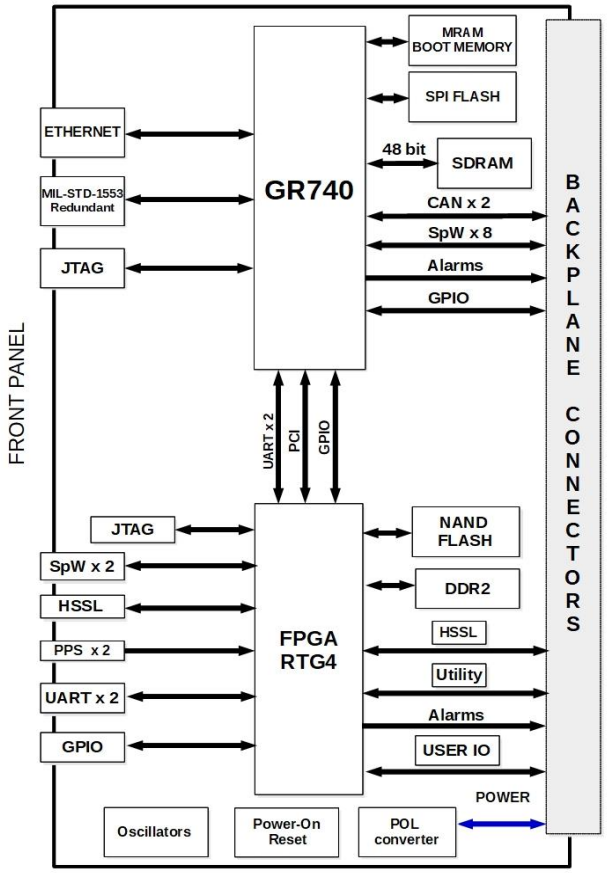


- SpW Dual Star



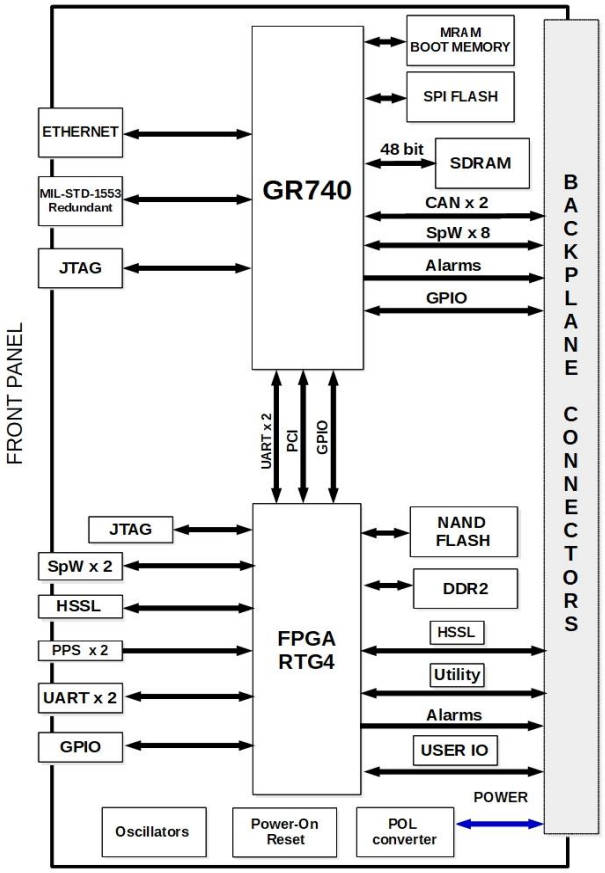
- Full mesh - HSSL





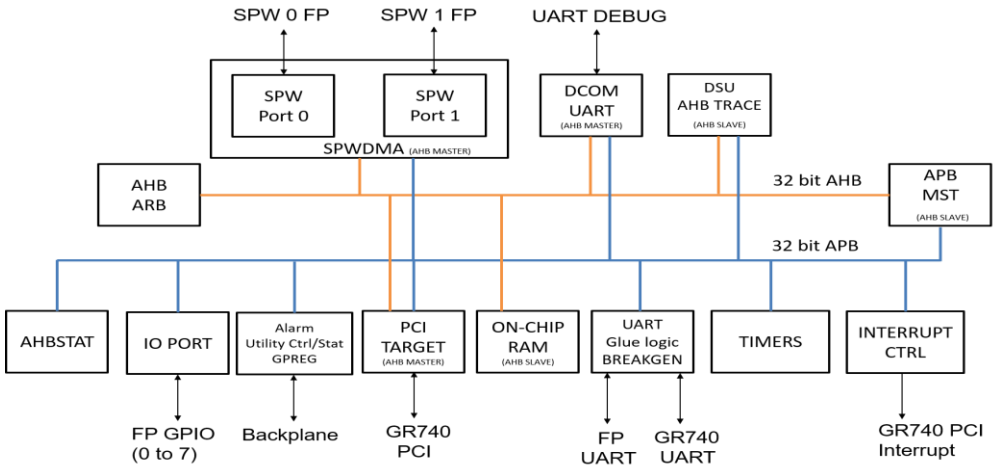
GR740 Single Board Computer
Interfaces between GR740 and RTG4

- The communication interface between the GR740 and the FPGA
  - Must utilize least amount of FPGA resources
  - GR740 must be able to control, configure (register access) and stream data into the memory connected with the FPGA
- A trade-off has been performed comparing PCI, SpaceWire and Ethernet MAC-to-MAC interfaces.
- PCI has been chosen since it provides following advantages compared to other interfaces:
  - PCI memory mapped solution can offer register access with less software overhead compared to using SpaceWire RMAP
  - PCI also provides streaming of data using dedicated DMA available in the GR740
  - Well known and established bus with VHDL IP cores available for FPGA implementation
  - Visibility to the performed accesses compared to other interfaces
  - Easy to analyse the PCI in a bread board setup since standard connectors/backplane solutions and prototype boards are available which helps early SW development
  - SW product development:
    - There are several developments with GR740 and FPGA interfaced using PCI
    - The SW output from this activity can be used by several users of the GR740 if the SBC SW development targets PCI implementation
  - The CPCI Serial Space specification (CPCI-S.1)
    - Standard requires eight SpW interfaces from a system slot controller to communicate with all its peripheral slot devices
    - If PCI is used, then all the eight SpW interfaces available from the GR740 SpW router can be utilized for the backplane SpW routing needs



GR740 Single Board Computer
FPGA VHDL design

- FPGA VHDL design
  - Interface for communication with GR740, PCI target implementation
  - AMBA 2.0 bus fabric for integration of different IP's with AMBA support
  - Reset handling
  - On chip clock generation
  - On chip memory
  - UART Glue logic, to provide additional features to support the SAVOUIR UART spec
  - General purpose IO ports to FP
  - Status, interrupt interface between FPGA and the GR740
  - Utility and Alarm signal handling
  - PPS distribution



- Having standards like PCI and AMBA helps to develop and integrate different IP's (accelerator's) with a standard communication medium.
- Having AMBA bus gives the possibility to easily add additional IP cores for future design.
- Several IP cores are required to realize the defined FPGA design.
- The following IP cores are identified, procured and used in the implementation.

IP	Functionality
SPWDMA	SPW with DMA supporting four SpW interfaces and an AMBA interface
AHBARB	AHB arbiter and decoder
APBMST	AHB/APB bridge
AHBRAM	On-chip RAM with AHB slave interface
TIMERS	Two general purpose timers
DCOM	UART for debug support unit
DSU	To utilize the AHB Trace from this IP
AHBSTAT	AHB status register. Latches the address and bus parameters when an error is signaled on the AHB bus
IOPORT	General purpose IO
IRQCTRL2	Interrupt Controller
PCI TARGET	PCI target interface with AMBA
BREAKGEN	To generate BREAK as per the "SAVOIR UART protocol and interface specification". The IP has programmable baud rate capability.
GPREG	An IP to act as general-purpose register. The registers can be used to store and drive necessary signals in the design. The IP provides the capability to read and write the registers using AMBA APB bus.

Type	Used	Total	Percentage
4LUT	10925	151824	7.20
DFF	7301	151824	4.81
User I/O	113	720	15.69
RAM64x18	64	210	30.48
RAM1K18	8	209	3.83
H-Chip Globals	24	48	50.00
RCOSC_50MHZ	0	1	0.00
CCC	3	8	37.50
SYSRESET	1	1	100.00
GRESET	1	1	100
RGRESET	15	206	7.28

- Clock generation
  - The design make use of the RTG4 Clock Conditioning Circuit (CCC) blocks available in the FPGA fabric to generate the clocks necessary for the FPGA design and for the clocks needed for the GR740SBC board.
  - FPGA design clocks,
    - System clock (40 MHz) *
    - SpaceWire transmit clock (80 MHz) *
    - SpaceWire 10 MHz clock
    - SERDES clock, 125 or 156.25 MHz
    - SpaceFibre Codec clock
  - GR740SBC board required clocks,
    - MIL_CLK for GR740 20 MHz
    - Ethernet PHY clocks, 25 and 125 MHz
    - SDRAM clocks (memory interfaced with GR740), as needed by the design, currently estimated to be (45 MHz) *

(*) Note these clocks can be modified according to the user needs or needs of the board design. The current values are listed above but in future other frequencies can be generated.

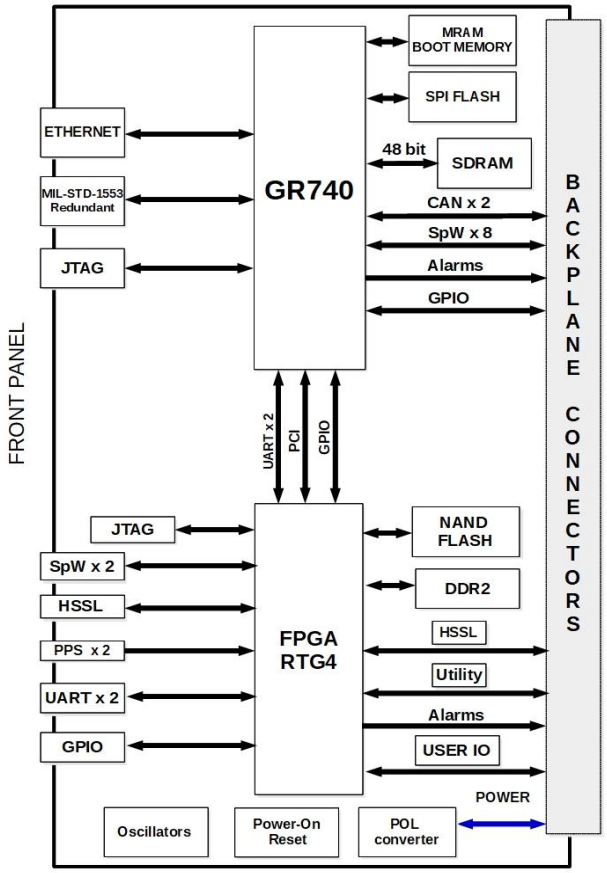
Module	Clock source (MHz)	GL0 (MHz)	GL1 (MHz)	GL2 (MHz)	GL3 (MHz)
Clkgen_1	External 50 MHz	40 system clock	80 SpW transmit clock	20 MIL1553 clock to GR740	50 Second clk50
Clkgen_2_eth	Second clk50	25	125 Gigabit Ethernet clock 125 MHz, needed for GR740	125 Gigabit Ethernet PHY clock 125 MHz clock	10 SpW start up clock needed for SPWDMA
Clkgen_3_speedgrade_1	Second clk50 EPCS_0_TX_CLK, output from the SERDES	45 SDRAM memory clock, to GR740 device	45 SDRAM memory clock, to SDRAM device	156.25 SERDES clock	78.125 SPFI codec clock

- A separate FPGA design is developed based on GRLIB
  - To implement the extended IP cores required for HSSL, NAND FLASH and DDR2 memory controller
- This design is implemented to sanity check the pins used for implementing the extended interfaces are proper
  - The implementation so far resulted in the design passing the Synthesis and PR
- This design use the same clock generation scheme as utilized for the ESA design
- The design synthesis, place and root performed using the Microsemi Libero Software Release v12.5.

Type	Used	Total	Percentage
4LUT	45904	151824	30.24
DFF	31283	151824	20.60
I/O Register	8	2154	0.37
User I/O	357	718	49.72
-- Single-ended I/O	333	718	46.38
-- Differential I/O Pairs	12	358	3.35
RAM64x18	0	210	0.00
RAM1K18	45	209	21.53
MACC	0	462	0.00
H-Chip Globals	20	48	41.67
CCC	3	8	37.50
RCOSC_50MHZ	0	1	0.00
SYSRESET	1	1	100.00
UJTAG	1	1	100.00
SERDESIF Blocks	1	6	16.67
FDDR	2	2	100.00
GRESET	1	1	100.00
RGRESET	3	206	1.46

GR740 Single Board Computer
Misc. details

- Bootstrap and configuration settings resistors
- Power
  - VIN power input +12V via backplane
  - On-board regulators converting from VIN to 3.3V, 2.5V, 1.8V & 1.2V
  - Power consumption: ~30 W (estimate)
- Form factor
  - 6U (233.5 mm x 160 mm),
  - Slot width of 5 HP,
  - Mass 1.2 kg (estimate)



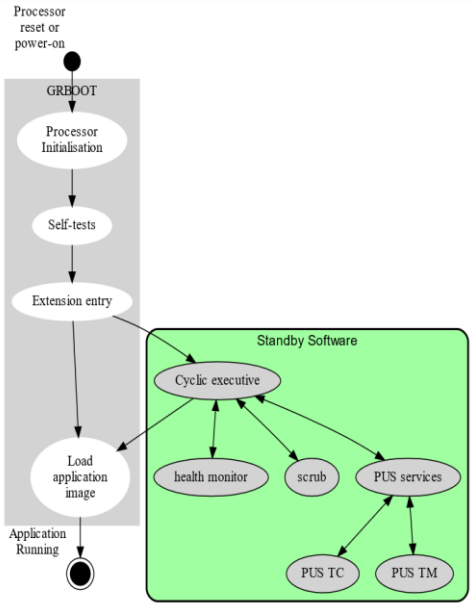
Together ahead. RUAG

Agenda

- Development introduction
- HW overview
- Compact PCI Serial Space
- HW design description
- SW description
- Summary

GR740 Single Board Computer
SBC software description

- The SBC is supported by boot software (GRBOOT), device drivers and test application software
- GRBOOT Boot Software
  - The GRBOOT Boot Software is responsible for taking the GR740 from system reset state to the execution of multi-processor mission application software
- Peripheral drivers
  - The purpose of the peripheral driver development is to provide the GR740SBC application developer with a high-quality implementation of drivers for:
    - GR740 CAN controller (GRCAN)
    - GR740 PCI host controller (GRPCI2)
    - GR740 SPI controller (SPICTRL)
  - These drivers will complement the software environment output from ESA activity "Qualification of RTEMS-SMP" to create better RTEMS-5 SMP support for the GR740 SBC
- Test application
  - The focus for the Test Application (TA) and EGSE SW is to verify the board interfaces and functions on a functional level
  - The TA and EGSE SW developed in this activity can be reused and extended for a specific implementation of the GR740 SBC platform simplifying an efficient functional verification of the hardware platform



GR740 Software Ecosystem

Operating Systems

OS	Real Time	SMP	AMP	MMU	Toolchain	License
BCC bare-metal	Y	N	*	N	GCC/LLVM	BSD
RTEMS-5 **	Y	Y	Y	N	GCC/LLVM	BSD/GPL
Linux 4.9	N	Y	*	Y	GCC	GPL
VxWorks 7	Y	Y	Y	Y & N	GCC/LLVM	COM
Zephyr RTOS 2.5	Y	N	*	N	GCC	APACHE

*) single-core and/SMP support, no dedicated AMP mode

**) ESA RTEMS SMP qualification package released 2021/2022

Hypervisor and memory protection support via Partners

- Para-virtualization or processes interface for mixed criticality, protection using MMU
- WindRiver VxWorks 7 Real-Time Processes (RTP) w/wo Time Partition Scheduler
- FENTISS Xtratum Next Generation (XNG)
- SysGo PikeOS

Software ecosystem support from Cobham Gaisler

- Software Life-cycle webpage
- Software Overview webpage
- Updated continuously as part of LEON device support and LEON5

  Upcoming releases Q2 and Q3: Linux 5.10 LTS and Zephyr 2.6 LTS

GR740 Software Ecosystem

Toolchain support

- GCC-7 and GCC-10 (GPL)
- LLVM Clang-8 (MIT)
- C/C++11 or later depending on environment

Boot loaders

- MKPROM2 (GPL)
- GRBOOT (COM)
  - ECSS quality development flow, Criticallity B
  - Flight Computer Initialisation Sequence (SAVOIR-GS-002)
  - Unit/validation test-suite
  - Optional STANDBY SpW/PUS remote terminal

GRMON-3 hardware debugger

- Assembly and C/C++ via GDB
- JTAG and Ethernet debug-link
- GR740/LEON4 drivers, AMP and SMP system support
- Instruction trace, AHB bus traces, I/O register inspection, etc.

Simulator (GR740 specific support)

- TSIM3 multi-core simulator
- Wind River Simics simulator (partner)

Agenda

- Development introduction
- HW overview
- Compact PCI Serial Space
- HW design description
- SW description
- Summary

- With the available processing capability, memory and redundant interfaces, the following applications are examples of potential use cases for the SBC:
  - Centralized payload control and data handling for multiple instruments
  - Image processing and selection of valuable data for earth observation or similar missions
  - Visual navigation for critical docking and lander missions, e.g., debris removal, satellite life-extension and lunar and mars missions
  - Object identification tracking for surveillance missions
- The activity consists of five major work phases (requirements definition, preliminary design, detailed design, manufacturing and validation).
- Currently the activity is at detailed design phase. The activity is expected to complete in Q4 2021.

EBB GR-CPCIS-GR740 availability: Q4 2021

Thank you for listening!

Together ahead. RUAG

CAES

PIONEERING ADVANCED ELECTRONICS