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Systematic Evaluation of the European NG-LARGE FPGA & EDA Tools for On-Board Processing

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1. Introduction

2. Evaluation Methodology

**3.** Evaluation Results

4. Conclusion and Future Work

# INTRODUCTION

# On-Board Data Processing

 $\odot$  applications  $\rightarrow$  increased computational & I/O demands, multiple algorithms, ...

 $\odot$  platforms  $\rightarrow$  reliability, re-programmability, low-power, fast I/O, ...

# Embedded Platforms

 $\odot$  space-grade CPUs  $\rightarrow$  never reach "very high-performance"

 $\odot$  space-grade FPGAs  $\rightarrow$  limited pool, even smaller for European high-density chips

○ high-density EU space-grade FPGAs → NanoXplore BRAVE FPGAs

# NG-LARGE FPGA

 $\odot$  2<sup>nd</sup> European high-density FPGA  $\rightarrow$  successor of NG-MEDIUM

 $\odot$  to be used in ESA missions ightarrow Navigation, Exploration, ...

 $\odot$  <u>competitive</u>  $\rightarrow$  radiation-hardness, resources, reconfiguration

# INTRODUCTION

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## **NG-LARGE** Features

- SRAM-based, 65nm, rad-hard by design
- $\odot$  logic/arithmetic  $\rightarrow$  137K LUTs, 32K CYs, 384 DSPs
- $\odot$  memory/register  $\rightarrow$  129K DFFs, 192 RAMBs
- $\bigcirc$  <u>I/O</u>  $\rightarrow$  SpaceWire @400Mbps (also for configuration)

# "QUEENS2" ESA Activity

- "QUality Evaluation of European New SW for BRAVE II"
  - assessment of the <u>SW programming tool</u> (NXmap)

LUT6

10099

10108

10093

intensive DSP benchmarking on the <u>HW chip</u> (NG-LARGE)

DFF

7386

7388

7411

irtex-50V xar5vfx130) with SIFT Descr benchmark

DSP25x18

32

32

32

RAM

Kbits 612

1116

2304

4320

NG-Large (BRAVE)

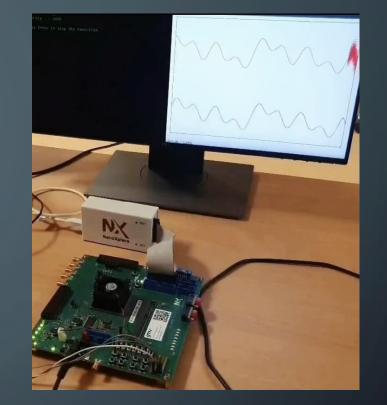
RAMB36

17

31

64

120



#### based on our evaluation methodology!

	c4	10248	7416	32	
			•		
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Config.

c1

c2

c3

OBDP2021

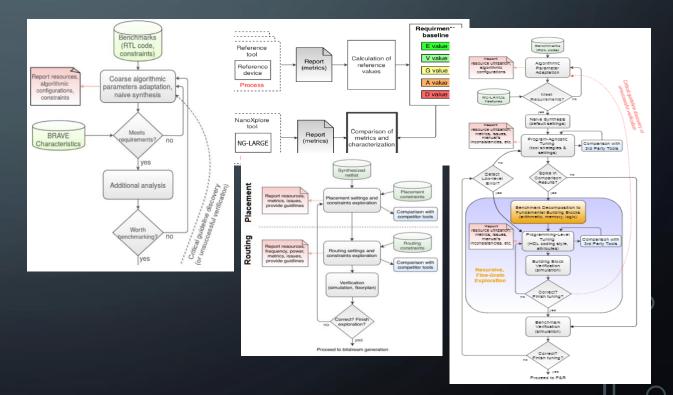
# **PROPOSED EVALUATION METHODOLOGY**

### Systematic Assessment Approach

- enhanced vs QUEENS1 activity (NG-MEDIUM evaluation)
- involves feedback loops
- $\odot$  performs comparisons vs. state-of-the-art tools/devices  $\rightarrow$  COTS & space-grade FPGAs

# Methodology Steps

- 1. selection of benchmarks
- 2. definition of rating method
- 3. assessment of synthesis
- 4. assessment of placement & routing
- 5. assessment of bitstream generation



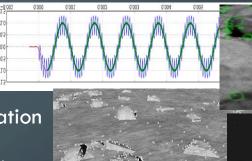
# STEPS 1-2: BENCHMARKS AND RATING METHOD

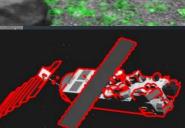
### Benchmark Selection

 $\odot$  goal  $\rightarrow$  stress the tool/device with diverse algorithms (computations, I/O, resources, etc.)

#### ○ <u>categories</u>:

- DC1: low-complexity  $\rightarrow$  FSM, RAM, MULT, ADD
- DC2: medium-complexity  $\rightarrow$  LEON3, VGA controller
- DC3: high-performance DSP  $\rightarrow$  image processing, navigation
- $\odot$  <u>selection criteria</u>  $\rightarrow$  scalability, diversity, throughput, etc.





# Rating Method

- $\odot$  <u>goal</u>  $\rightarrow$  define the evaluation process and comparison to 3<sup>rd</sup> party tools
- $\odot$  metrics  $\rightarrow$  resource utilization, frequency, power, tool runtime, etc.
- $\odot$  <u>reference value</u>  $\rightarrow$  average of all the 3<sup>rd</sup> party results

# STEP 3: ASSESSMENT OF SYNTHESIS

## Assessment Targets

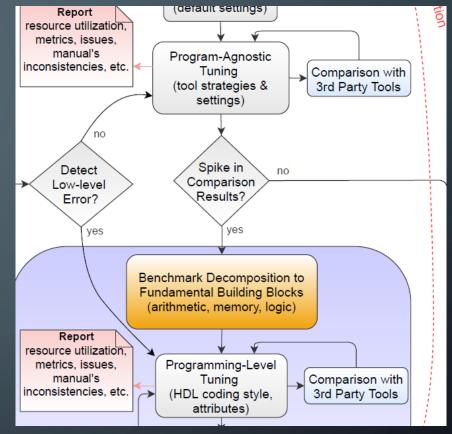
- NXmap settings (strategies and synthesis options)
- mapping efficiency
- quality of results (resources, correctness)
- quality of NXmap reports

### Testing in 2 Stages

- 1. program-agnostic tuning  $\rightarrow$  tool settings
- 2. <u>programming-level tuning</u>  $\rightarrow$  HDL coding

### Assessment Mechanisms

- $\odot$  <u>report records</u>  $\rightarrow$  systematic comparison with 3<sup>rd</sup> party tools
- $\odot$  <u>functional verification</u>  $\rightarrow$  post-synthesis netlist <u>simulation</u>
- $_{\odot}$  issues resolving ightarrow benchmark decomposition to small blocks + feedback loop



# STEPS 4-5: ASSESSMENT OF P&R AND BITSTREAM

### Placement & Routing

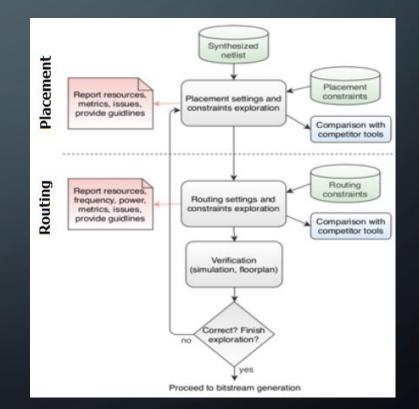
- exploration of physical constraints & place/route settings
- assessment of STA, power consumption, reports
- $\odot$  <u>functional & timing verification</u>  $\rightarrow$  post-P&R netlist simulation

# Bitstream Generation

- $\odot$  configuration interfaces & speed
- reconfiguration tests
- bitstream validation

# HW Verification

○ comparison to ground-truth data



# EVALUATION RESULTS (1/2)

## Implementation of High-Performance Benchmarks

- <u>benchmarks</u> → FIR, Harris, Canny, Disparity, SpaceSweep
- <u>SW tool</u> → NXmap3 v.2020.3 (also tested v.2.9.6, v.2.9.7, v.3.0.9, v.2020.1)

# Resource Utilization

- competitive vs 3<sup>rd</sup> party tools (compare absolute numbers)

  - LUT  $\rightarrow$  good (-6% for Harris, -57% for Disparity, +48% for Canny)
  - DFF  $\rightarrow$  good (-2% for Harris, -5% for SpaceSweep, +46% for Canny)
- significant improvement vs QUEENS1
  - NXmap3  $\rightarrow$  more mature vs earlier versions (NXmap2)

FIR

Harris

Canny

Disparity

80

101 60

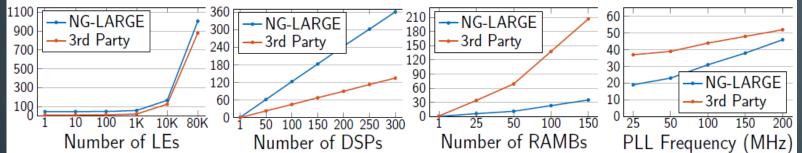
1751

2.669

1563

# Evaluation Results (2/2)

## Power Consumption



worse w.r.t. LE/DSP (5x-1.5x)
better w.r.t. RAMB/PLL (up to 6x)
similar static power (diff. 0.08W)

# **Performance**

	Frequency (MHz)	Runtime (s)	Throughput (*)
FIR	214	continuous	214 MSPS
Harris	40	0.19 / frame	5.3 FPS
Canny	38	0.10 / frame	10 FPS
Disparity	50	6.7 / frame	18 MPDS
SpaceSweep	52	10.8 / frame	29 MPDS

- O Disparity/SpaceSweep (1024x1024)
  - improve depth extraction by 1 order
- Harris/Canny (1024x1024)
  - sufficient: VBN  $\rightarrow$  1-10 FPS
- O Frequency Improvement vs Nxmap2

# SYSTEM-LEVEL EVALUATION: "SPARTAN VBN2"

Implementation of Entire VBN System (I/O + Processing, past ESA activity)

- algorithms on HW → Harris Corner Detector + SIFT Descriptor/Matching
- $\odot$  <u>architecture</u>  $\rightarrow$  GR740 (processor) + NG-LARGE (accelerator)
- $\bigcirc$  <u>I/O</u>  $\rightarrow$  SpaceWire @100Mbps for 512x512 stereo pair + HW output

### Comparative Evaluation

	LE	LUT	DFF	DSP	RAMB	MHz	
NG-LARGE			56296		113	22	
	(76%)	(71%)	(44%)	(65%)	(58%)		
3rd Party	14894	50427	39008	129	228	30	
	(73%)	(62%)	(48%)	(40%)	(77%)	30	

				<b>Total System</b>		
	$\mathbf{Time}^1$	$\mathbf{Time}^1$	$\mathbf{Time}^1$	<b>Time</b> <sup>2</sup>	<b>Throughput</b> <sup>2</sup>	
NG-LARGE	208ms	395ms	28ms	1251ms	0.8 FPS	
<b>3rd Party</b>	104ms	196ms	28ms	624ms	1.6 FPS	
$\frac{1}{2}$ refers to one 512×512 image.						

<sup>2</sup> refers to a localization step with one  $512 \times 512$  stereo pair.

#### ○ results vs competitor

- LE, LUT, DFF  $\rightarrow$  6.5x, 2x, 1.4x more (due to LE & LUT architecture)
- DSP  $\rightarrow$  2x more (due to design choices)
- RAMB  $\rightarrow$  2x less (due to bigger RAMB size)
- Max MHz  $\rightarrow$  > 2x less (improving among Nxmap versions)
- system throughput  $\rightarrow$  2x less FPS

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#### o fully functional, correct execution!

# CONCLUSION AND FUTURE WORK

# $\Box$ NG-LARGE $\rightarrow$ Promising Space-Grade Solution

- O <u>successful</u> HW execution of high-performance benchmarks
- O <u>competitive</u> resource utilization and power consumption
- <u>sufficient</u> SW tool capabilities
- <u>improving</u> throughput (already good for space applications)

# **Evaluation of NG-ULTRA ("QUEENS3")**

- assessment of SoC's embedded processor
- implementation of new benchmarks (e.g., telecom)

### Implementation of New VBN Pipelines & Al Algorithms

- custom designs on BRAVE FPGAs
- $\odot$  I/O via SpaceWire

# Thank you! Questions?

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"QUEENS2"

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