A Low Power Dynamic Circuit Topology towards a-IGZO Thin-Film Ultrasonic Transducer Driving Circuit

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***Abstract*—A 4bit counter with dynamic logic is demonstrated running up to 3.5MHz at 8.4V using amorphous indium-gallium-zinc-oxide thin-film transistors (a-IGZO TFT). Dynamic logic is selected to achieve the required speed for digital circuits driving ultrasonic transducers enabling large-area ultrasonic applications. In addition a back-gate switching technique is introduced in order to further reduce logic area and increase speed of the dynamic gate, illustrating to our knowledge the best in class EDP product for a small footprint meeting the requirements for ultrasonic transducer driving.**

***Index Terms*—IGZO, thin-film, ultrasonic driving, dynamic circuit, back-gate switching**

I. Introduction

In recent years a growing number of applications have been making use of ultrasonic transducer arrays, ranging from ultrasonic fingerprint-readers [1] to ultrasonic haptic feedback systems [2]. These applications either implement large bulk piezo transducers in conjunction with PCB-driving circuitry or smaller MEMS transducer arrays driven by a silicon integrated circuit. This inhibits to either increase the size of the array, or to increase the resolution beyond the possibilities that a PCB solution could offer.

Integrating both driving circuits and transducers into a single thin-film technology would enable to create high density systems at a low cost. In addition, these flexible transducer-driving systems would enable new possibilities in physical design and integration, such as seamless integration into a car dashboard. Thin-film transducers already show some promise but lack thin-film driving circuits for full integration [3]. Passive driving of transducers bring certain challenges to the system operation. Firstly the phase shift over the passive lines towards the transducers is difficult to compensate for. Secondly driving the transducers requires a large amount of power. As a consequence, supplying this power to transducers dissipates large amounts of resistive losses over the long driving lines. Increasing the line width's is neither the solution as the large amount of wide wires would lead to routing congestion. An approach to circumvent this issue is to connect columns and rows together. This set-up eliminates individual driving and thus limits the performance of the whole array. These problems can be solved by placing a TFT driving circuit underneath the transducer as illustrated in Figure 1.

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Thin-film transistors as an emerging research field have shown a lot of potential for applications with recent innovations in low-cost NFC tags [4], gate drivers for displays [11], and sensor arrays for bio-potential measurements [10]. In order to expand to ultrasonic arrays some key issues need to be addressed. Firstly, in these applications power consumption is a major concern. Lower power consumption could enable the system to be mobile by using battery power. However a big concern is the limited thermal budget of TFT circuits on flexible substrates. Secondly the footprint of the circuit is another limitation, as it can not exceed the surface area of the transducer and must match the pixel pitch. As a consequence, a reduction of area is also needed compared to conventional topologies in TFT. The current high-power consumption is due to the lack of complementary thin-film devices and thus of a good pull-up device for n-type only IGZO. Conventional topologies such as diode-load logic (DLL), zero-V_{gs} logic (ZVL) and Pseudo-CMOS do not solve this pull-up problem. Recently crossover logic has been presented [5]. Although it solves the static current path and thus the linked high-power consumption, it lacks speed performance. Since ultrasonic application requirements are demanding in operational frequency, we propose dynamic logic.

This paper discusses the thin-film circuit requirements for ultrasonic transducer driving and demonstrates a 4bit dynamic counter as benchmark circuit. Such a counter is a crucial element for beamsteering in our proposal to drive an US transducer array. The 4bit counter is designed with a novel dynamic topology illustrating a working dynamic circuit in IGZO technology. Dynamic back-gate switching is proposed to further improve upon the conventional dynamic topology. Finally the last section shows measurement results of the dynamic counter compared to a static DLL counter.

II. Design

In order to create beam-steering capability in the transducer array, each transducer in the array has to be driven by a particular phase. To generate these phase shifts locally in the circuit below the transducer an analog or a digital approach is possible. As TFT technologies suffer from large mismatch and process variations an analog implementation would result

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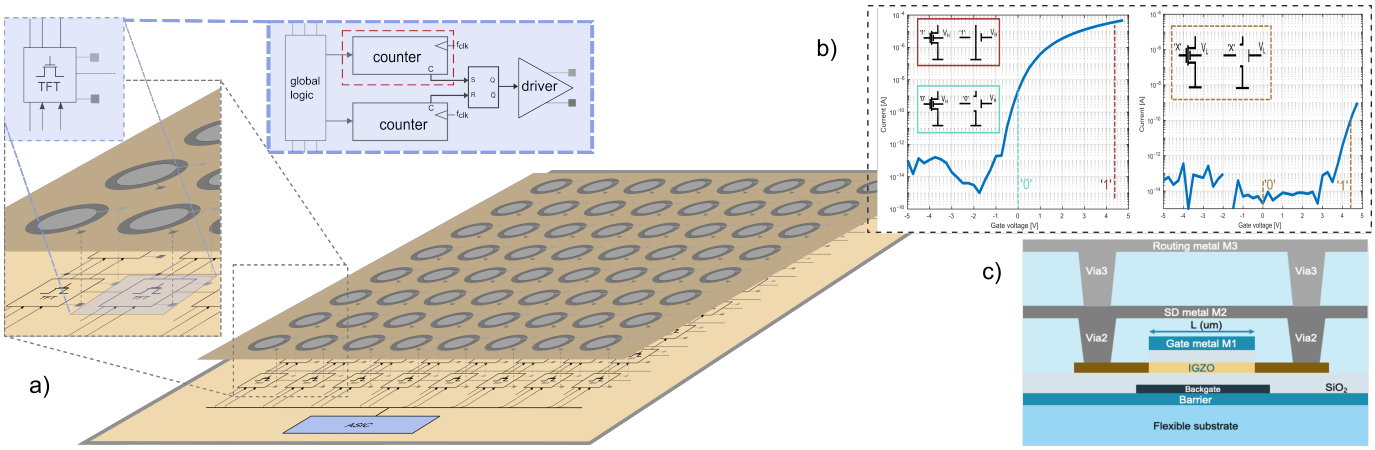

Fig. 1. a) A thin-film system concept for ultrasonic transducer applications with a closer look into the thin-film transistor driving circuitry. b)The states of the dual-gate transistor with corresponding measurements of a TFT (W=400μm L=2μm, different wafer from measurement samples). c) Cross section of a dual gate self-aligned IGZO thin-film transistor and metal stack of the used technology [5].

in a low yield. A synchronous digital approach has a larger robustness to process variations. In order to generate a synchronous phase shift in a digital manner, a high speed digital synchronous counter is needed as illustrated in Figure 1. This counter should operate at a clock frequency $f_{clk} = 2^n.f_{osc}$ with f_{osc} the oscillating frequency of the transducer to achieve a phase accuracy of n bits. In order to achieve this high speed with low power consumption, static current should be eliminated. Dynamic gates already have been employed to solve this problem [6] and have shown some improved characteristics on electrical stability compared to DLL and differential logic [7].

A. Back-gate switching

The potential at the back-gate influences the threshold voltage V_T and can be used to compensate process variations [8], however another option is to inhibit charge carrier accumulation in the channel for normal operation voltages at the gate. Driving the back-gate at a large negative voltage pushes the electrons away from the gate, inhibiting the gate to accumulate electrons and create a channel. By using this negative voltage the transistor has a third possible state as shown in Figure 1b. The measurements confirm that the gate potential does not increase the current in a significant manner and the TFT remains switched off.

In a dynamic circuit topology implementation [9], as depicted in Figure 2, by switching the back-gate from the normal compensating voltage from the normal compensating voltage for process variation (V_H) to a large negative voltage (V_L), it turns off the pull-down structure, eliminating the need for a footer transistor. This allows to reduce the size of the remaining pull-down transistors as the series resistance is lowered when the footer transistor is removed. Table I shows the simulated speed and area gains for basic gates by implementing the proposed back-gate switching. The total power given in the table also takes into account the amount of power needed to drive the clock signals for the logic gate, while T_{fall} and T_{rise} are the corresponding propagation delay of the rising and falling edge. Due to the added clock

TABLE I
PERFORMANCE COMPARISON

		NOR type I	NOR proposed	NAND Type I	NAND proposed	NAND DLL
P $[\mu W]$	Mean	**12.5**	**10.9**	13.2	13.7	**129.7**
	σ	2	1.8	1.5	1.8	18.1
T_{fall} $[ns]$	Mean	**15.1**	**10.8**	15.6	14.9	6.5
	σ	1.1	1.2	1.5	1.4	0.77
T_{rise} $[ns]$	Mean	12.9	9.4	20.9	12.3	12.9
	σ	4.1	3.0	8	4.8	4.92
A*$(\mu m)^2$	Mean	130	50	190	**90**	**300**

* Area determined by the summation of channel area.

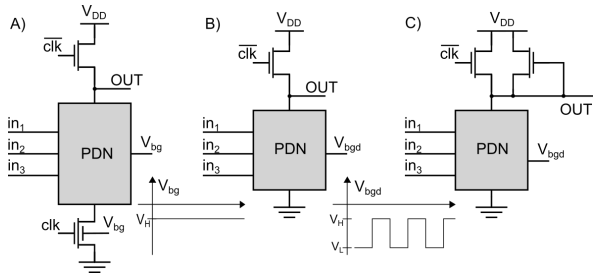

Fig. 2. A) The standard dynamic logic topology (Type I). B) The dynamic topology with backgate switching (proposed). C) B with a bleeder transistor.

signal and the reduced size of the pull-down network, the power consumption changes slightly, but is significantly lower compared to the static DLL implementation.

The voltage swing of the back-gate is determined by V_H and V_L. The V_H is brought to a slight negative voltage in order to shift V_T of the transistor just above zero. By shifting it slightly positive, the transistor is turned off if the logic state at the gate is low. By keeping the V_T low, the gates also reach maximal operating speed. For V_L the potential should be sufficiently low to switch off the transistor even when the gate is at logic level 'high', while keeping the swing between V_L and V_H as small as possible to minimize the feed-trough charge injection into the output stage.

To enhance robustness, a bleeder transistor is added to the dynamic gate. This results in the implemented topology as shown in Figure 2c.

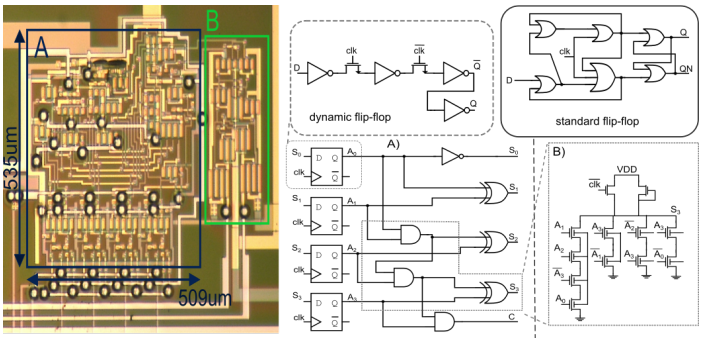

Fig. 3. a) Micrograph picture of the design with: A) The 4bit counter with the dynamic flip-flop B) The output buffer. The standard flip-flop is also illustrated.

B. Dynamic FF

Not only combinational logic draws a significant amount of power, also the flipflops are power hungry. To reduce the size and power consumption of the flipflops, a dynamic flipflop is proposed in Figure 3. It uses a passgate latch with simple DLL inverters. This latch relies on the parasitic capacitance of the inverter to store the input state. This reduces the size of the flipflop by reducing the number of transistors from the conventional 19 transistors to 14. In addition, it also improves the power consumption and the operational frequency of the flipflop significantly. The disadvantage of our approach is a reduced noise margin and therefore robustness of the flipflop.

C. Dynamic 4bit counter

In Figure 3 the full 4bit counter is shown. Here multiple logic gates are duplicated and integrated in a single dynamic gate compared to a conventional 4bit synchronous counter. This eliminates the issue of cascading dynamic logic gates which are well-known in conventional CMOS. The restructured counter has only a single stage of dynamic logic. An example of such a restructured gate is given in Figure 3.

TABLE II
MEASUREMENT RESULTS & COMPARISON

	Simulation DLL 4bit counter	Simulation Proposed 4bit counter	Measured Proposed 4bit counter
Power $[mW]$ @V_T=-0.96 @2MHz	12.42	3.87	/
Power $[mW]$ @V_T=0.63 @2MHz	7.86	4.12	5.11
Max. operating freq. [Hz]	2.3M	5.2M	3.5M
Area* $(\mu m)^2$	7316	3216	3216
standard logic compatible	yes	no	no

* Area determined by the summation of channel area.

III. Measurements and Results

In Figure 3 a picture of the fabricated 4bit synchronous counter (denoted A) on flexible polyimide foil is shown. The total footprint of the counter is $535\mu m$ by $509\mu m$. In order to drive a 4pF load for measurement of the output signal, a three stage output buffer is added (denoted B). All circuits are designed with a channel length of L=2um.

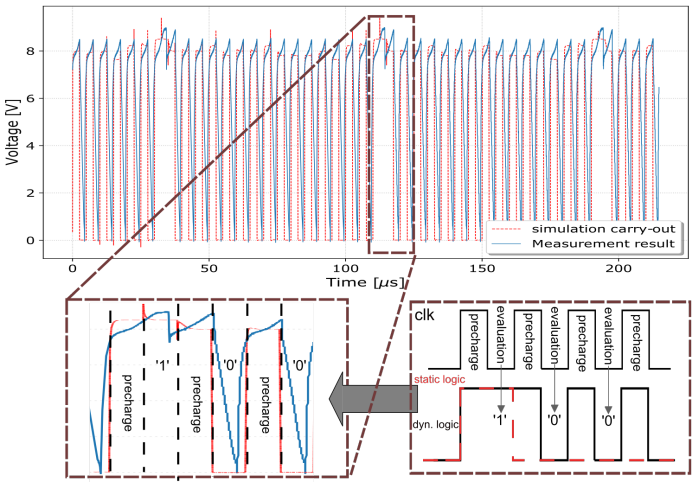

Fig. 4. Measurement of the 4bit counter and corresponding simulation with annotation of corresponding state.

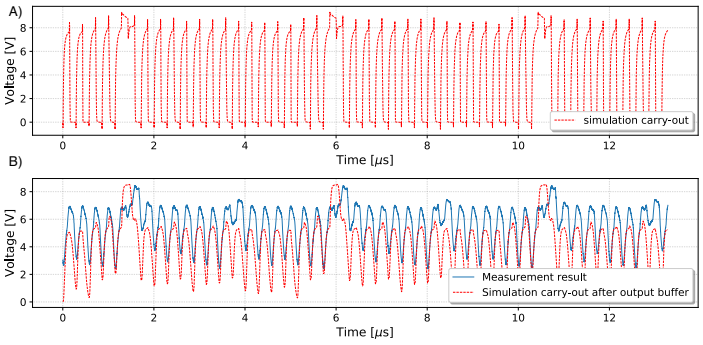

Fig. 5. A) Simulated waveform B) measured waveform comparison at maximal operating speed 3.5MHz.

Figure 4 shows the simulated waveform from the ripple carry of the dynamic counter. Each clock cycle, the signal evaluates from a pre-charged state to the evaluated logic state. For every 16 clock cycles the signal remains high as the logic state of the carry corresponds to '1'. Table II compares the demonstrated dynamic counter directly with a static implementation with DLL. The proposed counter has a significantly lower area and larger speed, but the power advantage is reduced due to the DLL inverters in the flipflop and the expected V_T from -0.92V to 0.63V. Good correspondence is observed between measured and simulated results, with the measurement result shown in Figure 5 for the maximum operating frequency.

IV. Conclusion

This work demonstrates a dynamic logic style which is a viable topology in TFT technology for ultrasonic transducer applications. This logic style includes a novel back-switching technique to reduce the footprint of the circuit and further enhances the speed further. A 4bit counter has been realised. It operates at 3.5MHz consuming 5.11 mW power. This illustrates that ultrasonic transducer driving applications are possible with TFT technology. Future work will focus on integrating this dynamic circuitry in a fully integrated pixel-architecture to drive a transducer array.

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