Principles, Fundamentals and Applications of Programmable Integrated Photonics

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Abstract: Programmable Integrated Photonics is an emerging new paradigm, which aims at designing common integrated optical hardware resource configurations, capable of implementing an unconstrained variety of functionalities by suitable programming following a parallel but not identical path to that of integrated electronics in the last two decades of the last century. Programmable Integrated Photonics is raising a considerable interest as it is driven by the surge of a considerable number of new applications in the fields of telecommunications, quantum information processing, sensing and neurophotonics calling for flexible, reconfigurable, low-cost, compact and low-power-consuming devices that can cooperate with integrated electronic devices to overcome the limitation expected by the demise of Moore's Law. Integrated photonic devices exploiting full programmability are expected to scale from application specific photonic chips (featuring a relatively low number of functionalities) up to very complex application-agnostic complex subsystems much in the same way as Field Programmable Gate Arrays and microprocessors operate in electronics. Two main differences need to be considered. First, as opposed to integrated electronics, programmable integrated photonics will carry analog operations over the signals to be processed. In second place, the scale of integration density will be several orders of magnitude smaller due to the physical limitations imposed by the wavelength ratio of electrons and lightwave photons. Success of Programmable Integrated Photonics will depend on leveraging on the properties of integrated photonic devices and, in particular, on research into suitable interconnection hardware architectures that can offer a very high spatial regularity as well as the possibility of independently setting (with a very low power consumption) the interconnection state of each connecting element. Integrated multiport interferometers and waveguide meshes provide regular and periodic geometries, formed by replicating unit elements and cells respectively. In the case of waveguide meshes, the cells can take the form of a square, hexagon or triangle, among other configurations. Each side of the cell is formed by two integrated waveguides connected by means of a Mach-Zehnder Interferometer or a tunable directional coupler that can be operated by means of an output control signal as a crossbar switch or as a variable coupler with independent power division ratio and phase shift. In this paper, we provide the basic foundations and principles behind the construction of these complex programmable circuits. We also review some practical aspects that limit the programming and scalability of Programmable Integrated Photonics and provide an overview of some of the most salient applications demonstrated so far.

1. Introduction

1.1 Definition and general features of reconfigurable systems

Reconfigurable (or programmable) systems are configurations with soft-definable features that can be tuned, reshaped, or otherwise altered by digital logic to suit the purposes of their users [1]. These systems are usually referred to as "soft hardware", [1, 2]. Reconfigurability is now

commonplace in electronics components and circuits with the Field Programmable Gate Array (FPGA) device being the real paradigm of electronic reconfigurable systems.

FPGAs were initially conceived to compete with Application Specific Integrated circuits (ASICs). But nowadays, after almost 30 years since their inception, they have practically replaced them in most applications [3]. The increased complexity that can be achieved, fueled by the benefits of Moore's law and reduced non-recurring engineering costs, have propelled FPGAs to a leading position that is further sustained by the trend in fusing practical engineering and design principles. Thanks to FPGAs, one can effectively manage the flexibility required in the so-called software-x approaches, which include among others software-defined radios [4], software-defined networks [5], cloud computing [6] and data center concepts [7]. All in all, the FPGA concept has shown the potential of reconfigurability to become a disruptive technology in information and communication systems according to the requirements described by Christensen [8].

But, going beyond the all-digital FPGA concept, electronic programmable systems are being now developed that encompass as well new subsystems [3], including small sets of resident reconfigurable analog processing blocks as well as digital-to-analog and analog-to-digital conversion stages.

Going even further one may ask if it makes sense to consider the extension of programmable systems to other application scenarios such as reconfigurable circuitry at radio frequencies, antenna structures and, of course, photonics. None of these fields have yet reached the degree of integration maturity of electronics in general and FPGAs in particular.

Broadly speaking, the design of reconfigurable systems needs to consider two important aspects. The first one, known as *designing for reconfigurability*, refers to the set of ideas for embedding flexibility within systems through the methodical incorporation of exploitable switch and configuration mechanisms. The second aspect, known as *designing with reconfigurability*, refers to the processes by which user designs are embedded in reconfigurable fabrics, often through design automation.

Reconfigurable systems are sometimes criticized because they require overhead, which may lower performance and add complexity, possibly reducing reliability. These considerations must be traded-off against their advantages when considering their use for a particular application or field. Nevertheless, they bring a considerable number of benefits, which can be summarized as follows:

1. *Flexible reshaping of finite resources*: A reconfigurable system can be considered as a finite collection of resources that can be reshaped at will, leading to advantages in mass extreme customization, reduction of nonrecurring engineering expenses, economic savings through inventory collapse, design rectification and functional update and iterative refinement to accommodate evolution.

2. *Robustness and resilience*: Reconfigurability results in systems that are tolerant to faults and manufacturing defects by exploiting unused configurable resources. Redundancy can be implemented provided that enough spatial resources are available. Furthermore, by software programming it is possible to create self-healing and/or cooperative multitasking.

3. *Achieving "x on demand"*: Reconfigurability brings the advantage of creating systems quickly. Prebuilt parts can be personalized rapidly overcoming the long fabrication cycles of dedicated systems or chips. This is especially important in electronic microfabrication.

4. *Infinite resources through timesharing*: Reconfigurable systems can be thought as a set of infinitely re-purposeable components leading to temporal reuse.

The interested reader can find a very detailed description of these and other concepts pertaining to the general properties of reconfigurable systems in [1].

1.2 Programmable integrated photonics

Programmable Integrated Photonics (PIP) [9]-[24] is a new paradigm that aims at designing common integrated optical hardware configurations, which by suitable programming can implement a variety of functionalities that, in turn, can be exploited as basic operations in many application fields. Programmability enables by means of external control signals both chip reconfiguration for multifunction operation as well as chip optimization against non-ideal operation due to fluctuations in environmental conditions and fabrication errors. Programming also allows activating parts of the chip, which are not essential for the implementation of a given functionality but can be of help in reducing noise levels through the diversion of undesired reflections.

PIP comprises three main families that range from simple reconfigurable Application Specific Integrated Photonics Circuits (ASPICs) to multiport interferometers and, ultimately, integrated waveguide meshes. Figure 1 illustrates the classifications and connection between the different PIP families as well as some of the salient features of each one.

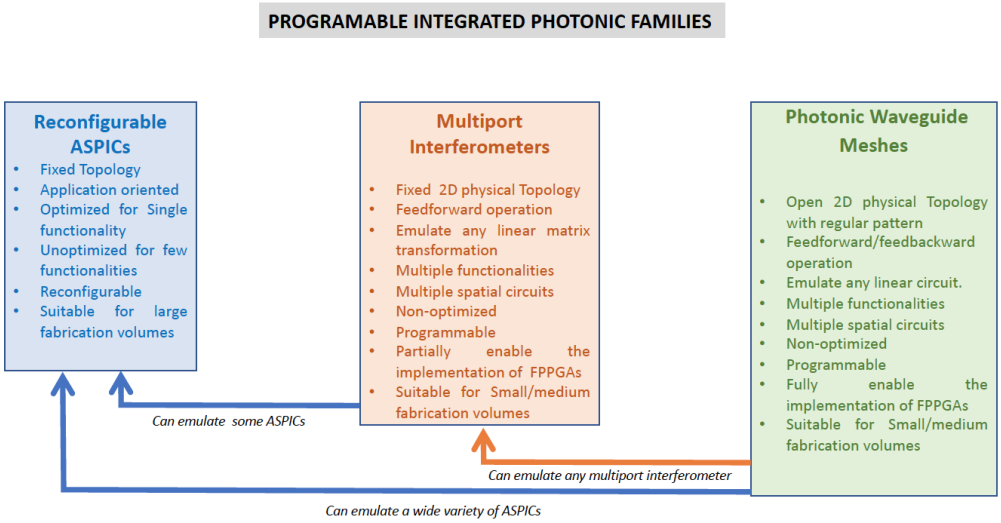

Fig. 1. Classification and features of the main Programmable Integrated Photonic families. (Authors elaboration)

The most basic configuration for PIPs is the reconfigurable ASPIC, which retains most of the main features of fixed designs but bring some degree of reconfigurability whereby the operation and bias points governing the circuit response can be programmed but the overall functionality of the chip is not changed. A second family is formed by multipoint interferometers. These are based on two-dimensional (2D) fixed topologies built from tunable interferometers and can be programmed to emulate any linear feedforward arbitrary unitary matrix transformation. Finally, photonic waveguide meshes, based on open 2D topologies following regular geometric patterns are capable of emulating any reconfigurable ASPIC and multiport interferometer while in addition can implement any feedforward and feedbackward transformation.

PIP aims to provide a complementary approach to that based on fixed ASPICs, which has been dominant during the last years with an ultimate objective of seeking similar advantages as FPGAs bring over ASICs in electronics, including fast time to market, low non-recurring

engineering costs, high flexibility and simple design flow. Of the above families, both multiport interferometers and waveguide meshes can support this *optical* FPGA concept and, therefore, will be the subject of this paper.

PIP has recently raised the interest of many research groups worldwide, justified by the surge of a number of emerging applications that are and will be calling for true flexibility, reconfigurability as well as low-cost, compact and low-power-consuming devices. One area in which considerable seminal work has been produced is quantum information, where PIP can open avenues to large-scale quantum gates and boson sampling circuits based on unitary matrix transformations [9], [10], [13], [15].

In the field of telecommunications, PIP can be instrumental in a series of signal processing functionalities, such as arbitrary mode converters [25], [26], fiber-wireless interfacing devices [27] and broadband switches [28], which can also form the basis for computer interconnections [29]. In the field of sensing, PIP can lead to a generic class of programmable measuring devices [30], which might be successfully integrated as a building block in the future Internet of Things.

The success of PIP relies on several factors. The first one is the disposal of a suitable material platform that enables the fabrication of complex photonic circuitry. In section 2.1 we review the salient features of the main alternatives that are currently available. As we will see, the most popular platforms feature somehow complementary properties in terms of losses, footprint and capability of incorporating active devices. Therefore, it makes sense to consider hybrid or heterogeneous approaches that leverage on the best of each of them. These approaches will be also briefly covered.

A second key aspect is the possibility of designing suitable basic building blocks able to carry elementary signal processing operations and interconnection architectures that can offer a very high spatial regularity and the possibility of independently setting (with a very low power consumption) the interconnection state of each connecting element. The most attractive and versatile option for the implementation of basic building blocks proposed so far is based on elementary 2x2 arbitrary unitary transformers also known as *rotation matrices*. From these transformers, one can construct 2x2 *reversible gates*. The principles behind these unitary 2x2 reversible gates are provided in section 2.2. An additional advantage of rotation matrix transformers is that they can be readily implemented by combining a set of fairly simple and standard integrated optic components reviewed in sections 2.3 and 2.4, such as beamsplitters, Mach Zehnder Interferometers, directional couplers and phase shifters. Section 2.5 illustrates how 2x2 reversible gates can be built from these components while section 2.6 introduces two basic processing subsystems: *mode converters* and *universal couplers* that can be built by suitable combination of reversible gates and find a considerable room for practical applications.

Complex circuit architectures for the implementation of PIP circuits make use of interconnection architectures for the basic building blocks, which fall broadly into two categories. The first, which is covered in section 3, includes the so-called multiport interferometers and has been historically the first to be developed, in particular to enable unitary linear optical transformations that are at the heart of quantum circuits, reconfigurable neurophotonic systems and Fourier-based optical signal processors [24]. The most popular multiport interferometer designs are the triangular multiport interferometer concept proposed by Reck et al. [21] and subsequently developed for integrated optics by Miller [11], [12]. The more recent rectangular multiport interferometer was proposed by Clements and co-workers [22], [23]. In sections 3.1 and 3.2, we provide a full description of these designs respectively while in section 3.3 we cover the more advanced topic of 3D fast interferometers. Multiport interferometers can enable any kind of linear optics transformations as long as feed-forward-only propagation is assumed. While this covers a wide range of applications, it does not enable the programming of resonant structures where simultaneous feed-forward and feed-backward propagation is required.

Integrated waveguide meshes [17]-[20], covered in section 4, are the second category of interconnection architectures and overcome this limitation. They provide regular and periodic

geometries, formed by replicating a unit cell, which can take the form of a square, hexagon or triangle, among other configurations. Each side of the cell is formed by two integrated waveguides connected by means of a beamsplitter/tunable coupler that can be operated by means of an output control signal as a crossbar switch or as a variable coupler with independent power division ratio and phase shift. A mesh formed by a suitable amount of unit cells can be programmed to implement a wide variety of functionalities much in the same way as a FPGA operates in electronics [17], [20]. In this section we cover the salient features and define the main figures of merit to benchmark the performance of different waveguide mesh designs and provide a comparative analysis.

Once we have discussed the possible implementation options for complex photonic architectures, the next logical step is to consider their use as the optical core of a much more flexible and versatile programmable system, the Field Programmable Photonics Gate Array (FPPGA), which is called to play a similar role to that of FPGAs in electronics. In a FPPGA, a common photonics hardware is designed to provide several resources that can be employed to implement different functionalities by means of programming. However, the FPPGA is different from the FPGA in the sense that it does not carry digital logic operations, rather it exploits optical interference to perform very-high-speed analog operations acting over the phase and amplitude of optical signals. We discuss the main features of FPPGAs in section 5, including the basic hardware design principles as well as design flow and technology mapping concepts.

The design, programming and operation of complex programmable integrated photonic circuits and FPPGAs entails addressing a considerable number of challenges and limitations. Some of these reside in the pure physical characteristics of the material platforms employed in their construction and mainly affect their insertion losses through signal coupling efficiency and propagation and scattering losses. Others are connected to the inherent fabrication errors and fluctuations in the operating values of the building blocks parameters and call for active control and monitoring of the waveguide meshes. A third class of challenge is connected to the design and programming of scalable structures containing ever increasing unit cells. These challenges are addressed in detail in section 6, where we also cover some of the most interesting experimental solutions reported so far.

Present and future envisaged applications of PIP are covered in section 7 where we address some applications in emerging quantum systems, including quantum computing and quantum transport simulation, as well as in classical applications such as telecommunications and switching, RF and analog photonics, neurophotonics and artificial intelligence.

2. Basic principles, building blocks and technologies

2.1 Fundamental material platforms for programmable integrated photonics.

PIP circuits rely principally on optical waveguides and, therefore, the same material platforms and approaches that are employed in the implementation of ASPICs are applicable here. In addition to the low cost implicit in the economies of scale resulting from replicating the same architecture, further cost savings can be ripped by aligning the fabrication processes with current state-of-the-art Generic Integration (GIM) and Generic Foundry (GFM) Models [31]. In the GIM, a small set of standardised basic building blocks are provided to control the basic properties of light and more complex circuits or Compound Building Blocks are then built by connecting several basic building blocks. In the GFM, the foundry provides a shared open access to its generic integration process through multi project wafers, where different designs are combined on the same wafer providing cost sharing and additional advantages such as on-wafer testing. Since GIM and GFM allow a broad range of functionalities to be synthesized from a small set of basic building blocks, they have been identified as the only path leading to mass production of photonic integrated circuits (PICs), where figures in the order of 10 €/mm^2 can already be reached at volumes of 1000 chips for InP technology [31].

To date, three material platforms: 1) Indium Phosphide (InP), 2) Silicon on Insulator (SOI) and 3) Silicon Nitride (Si_3N_4-SiO_2), have reached the required degree of maturity to be considered as viable options for programmable integrated photonics, either monolithic or hybrid. These operate mainly in the 1.3- and 1.55-μm wavelength regions. We briefly review the salient features of these and refer to the interested reader to the abundant literature in the field.

2.1.1 Indium Phosphide PIC technology

Indium Phosphide is a III-V compound semiconductor material and the only technology capable of the monolithic integration of active (i.e. featuring optical amplification) and passive photonic components [31]-[34]. A variety of techniques, including butt-joint regrowth, selective area growth, offset and dual quantum well placing and quantum well intermixing, can be employed to integrate regions with different absorption/gain properties along a single waveguide. Waveguide types include shallow (low loss and long bending radius) and deeply etched (higher losses and lower bending radius) designs (see upper row in Figure 2).

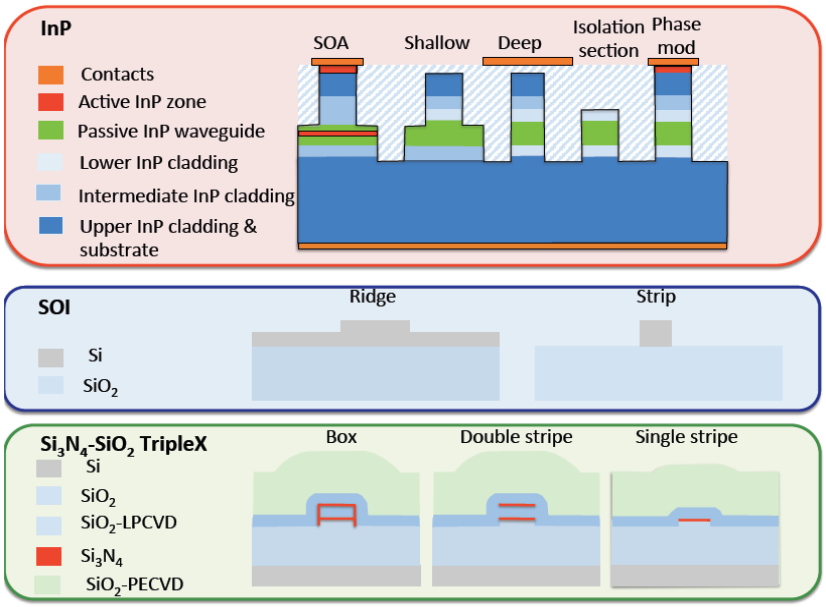

Fig. 2. Waveguide structures for the InP (upper row) SOI (intermediate row) and Si_3N_4-SiO_2 (lower row) platforms. (Authors elaboration)

Shallow waveguides have typical widths of 2 μm and this figure is approximately 1.5 μm for deeply etched designs. Typical losses are around 1.5 and 3 dB/cm for shallow and deeply etched waveguides, respectively, and this is usually quoted as one of the disadvantages of this technology. These losses can be reduced however to figures below 1 dB/cm by removing the p-type top layer in the non-active parts of the chip. Minimum bending radii are in between 10 and 500 μm for deeply etched and shallow etched waveguides, respectively. Another quoted limitation of the InP platform is related to the difficulty of its integration with electronics into the same chip. However, highly promising work is under way towards the integration of the full photonic functionality in a single InP Membrane on Silicon that could be implemented both in a CMOS or an InP fab, merging InP photonics with silicon electronics.

InP provides the most complete list of available components for integration [32] including: Passives, optical filters, arrayed waveguide gratings, semiconductor optical amplifiers, saturable absorbers, optical sources (Fabry-Perot, distributed Bragg reflector, distributed

feedback and mode-locked lasers), detectors (pin single and balanced configurations), amplitude and phase modulators and polarization handling devices. Moreover, it has shown record performance in integrated component count on the same chip with figures exceeding 450 and now targeting 1000 [33].

2.1.2 Silicon Photonics PIC technology

Also known as Silicon on Insulator [35]-[38], Silicon Photonics is a semiconductor technology where components are etched/patterned/fabricated in a 180-220 nm Silicon layer placed on top of a 1-3 μm insulator layer. Silicon passives are formed by initial few mask layers through partial and/or full Silicon etching steps after which multiple ion implantations are conducted for "active" devices such as Ge photodetectors and Silicon modulators. Coupling into and outside the chip can be performed via edge couplers (with typical losses of 1 dB/facet) or vertically, via Silicon surface gratings (3.5-6 dB/coupler with 40-70 nm 3-dB bandwidth). The main advantage of SOI technology resides in its potential compatibility with CMOS fabrication processes and the infrastructure used in microelectronics and thus in the potential for monolithic integration of the electronic and photonic parts of the chip. Refractive index contrast is over 100% (n = 3.4 for Silicon and n = 1.45 for SiO_2), leading to small footprint circuits.

Two main types of waveguides are available (see intermediate row in Figure 2): Ridge or shallow (1-8 μm width), which exhibit relatively low losses down to 0.1-0.5 dB/cm, but are limited in bending radius to around 100 μm, and Strip waveguides (500 nm width) that exhibit much higher losses (1-3 dB/cm) but support lower values for minimum bending radius (5-20 μm). Integration density on a chip is currently below 100 components [39], but the component count integration trend is exceeding the rate given by Moore's law indeed. Several basic photonic components are available in monolithic SOI, including passives, such as arrayed waveguide gratings and optical filters, Ge photodetectors, ring and travelling-wave electro-refractive modulators (up to 50 GHz). The main disadvantage of monolithic SOI technology is that it does not support optical sources and other active components such as optical amplifiers. To overcome this limitation, III-V functionalities have to be integrated into the SOI platform by means of either molecular [39] or adhesive [40] wafer bonding. This approach, known as hybrid silicon or hybrid integration technology has succeeded in incorporating amplifiers, saturable absorbers, optical sources (Fabry-Perot, distributed Bragg reflector, distributed feedback and mode-locked lasers, optical amplifiers, electroabsorption (>70 GHz), and Mach-Zehnder (>25 GHz) modulators, photodetectors (>35 GHz) and polarization handling components into SOI chips. However, GFM and GIM have not yet been developed for hybrid integration technology.

2.1.3 Silicon Nitride Si_3N_4-SiO_2 PIC technology

This waveguide technology is based on a combination of stoichiometric silicon nitride (Si_3N_4) as waveguide layers, filled by and encapsulated with silica (SiO_2) as cladding layers grown on a silicon wafer [41], [42]. SiO_2 and Si_3N_4 layers are fabricated with CMOS-compatible industrial standard low-pressure chemical vapour deposition equipment that enables cost-effective volume production. A special technology known as TriPleX™ [34], [41], developed by the Dutch company LioniX International, allows the fabrication of waveguides with minimized surface roughness allowing high refractive index contrast (20-30%) and low scattering losses.

The TriPleX™ platform offers seven waveguide cross-sectional geometries [41], some of which are shown in the lower part of Figure 2. Their salient characteristics at 1550 nm are: low index contrast box-shaped (1μm x1μm) that features reduced birefringence, ≤ 0.2 dB/cm losses and minimum bending radius (R_{min}) around 500 μm and Mode Field Area (MFA) of 3.6 x 3.6 μm^2; high-index contrast featuring R_{min} of 150 μm and MFA of 1.4 x 1.4 μm^2; single-stripe (R_{min} of 2000 μm, <0.03 dB/cm losses and MFA of 4.7 x 2.9 μm^2); double-stripe (1μmx1μm, R_{min} of 100 μm and MFA of 1.6 x 1.7 μm^2) obtained by removing the sidewalls of the box

configuration, which leads to significant reduction of the waveguide losses that are now in the <0.1 dB/cm range. In/out coupling is achieved by means of adiabatically tapered spot-size converters to low index contrast double-stripe cross-sections with <1 dB coupling loss. Several fundamental building blocks are available including the optical waveguide, tuning elements, directional and multimode interference couplers. From these, more complex subsystems have been demonstrated. For the double-stripe geometry, a library of standard optical components with predictable characteristics is available. The main disadvantage of this technology is that no optical sources, detectors, amplifiers and modulators are available. The integration of these components requires a hybrid approach with separately fabricated InP platform chips [42]. The recent development of InP device stamping techniques [43] and InP membranes on Silicon [44] opens the path for the compact and versatile implementation of this required hybrid integration approach.

2.2 Integrated waveguides and phase shifters

Integrated optical waveguides can have, as pointed out in the previous subsection, different geometries and refractive index profiles [45]-[49]. Their main role is to propagate stable electromagnetic field patterns known as guided modes. Although in general we will consider throughout this paper the term "mode" in a very general way as a solution to the Maxwell equations, we will not consider here other alternatives to guided modes such as radiation and leaky modes.

The solution of Maxwell equations for an integrated waveguide at a given frequency ω can be expressed as a superposition of guided modes, each characterized by a stable transversal field profile and a propagation constant [45], [46], [49]. In practice, a good approximation is to consider only transversal electric (TE) and transversal magnetic (TM) modes. Figure 3 (a) shows the top view of an integrated optical waveguide including the axes convention 1, TE modes are characterized by having only one non-zero electric field component E_x, H_y being proportional to E_x and $|H_z|<<|H_y|$. TM modes are characterized by having only one non-zero magnetic field component H_x and by E_y being proportional to H_x and $|E_z|<<|E_y|$.

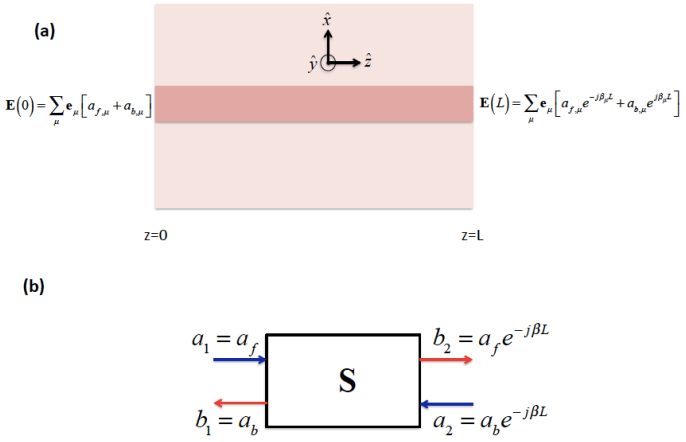

Fig. 3. (a) Top-view representation of a photonic integrated waveguide of length L with input and output fields corresponding to the different propagated modes. (b) Black-box representation of the integrated waveguide action over the fundamental TE_{01} mode (Adapted from [49]).

In general, we can write for TE modes the field in the waveguide as [49]:

$$\mathbf{E} = \sum_m \mathbf{e}_m \left[a_{fm} e^{-jb_m z} + a_{bm} e^{jb_m z} \right],$$
$$\mathbf{H} = \sum_m \mathbf{h}_m \left[a_{fm} e^{-jb_m z} - a_{bm} e^{jb_m z} \right], \quad (1)$$

where μ is the index representing the mode number, $a_{f\mu}$ $a_{b\mu}$ the mode amplitudes of the forward and backward propagation components respectively, β_μ is the propagation constant of mode μ and $\mathbf{e}_\mu$, $\mathbf{h}_\mu$ the field patters of mode μ, which can be expressed as:

$$\mathbf{e}_\mu = E(x,y)\hat{e}_\mu,$$
$$\mathbf{h}_\mu = H(x,y)\hat{h}_\mu, \quad (2)$$

where $E_\mu(x,y)$, $H_\mu(x,y)$ represent the field stable transversal profiles of the mode and $\hat{e}_\mu$ and $\hat{h}_\mu$ are the polarization vectors of the electric and magnetic fields, respectively. The actual shape of $E_\mu(x,y)$, $H_\mu(x,y)$ usually requires a numerical calculation using 2D and/or 3D solvers.

In the case of a singlemode (i.e., TE_{01}) propagation waveguide of length d and referring to Figure 3 (b) we have (μ = 1, but we drop the subscript in this case):

$$b_2 = a_f e^{-j\beta d} = a_1 e^{-j\beta d}, \quad (3)$$
$$b_1 = a_b e^{-j\beta d} = a_2 e^{-j\beta d}.$$

Hence, the scattering matrix for describing the waveguide action over this mode reads:

$$\mathbf{S} = \begin{pmatrix} 0 & e^{-j\beta d} \\ e^{-j\beta d} & 0 \end{pmatrix}. \quad (4)$$

The matrix can be extended as well to consider N propagating modes if needed, although, in the rest of the paper we will be mainly concerned with singlemode waveguides. From (4), we observe that the main action of the propagation along a waveguide consists in a phase shift of the propagated mode. Actually, the phase shift depends on the waveguide length and the mode propagation constant [45]-[49]. More generally, the propagation constant for the TE fundamental mode can be expressed in terms of an effective refractive mode index as:

$$\beta_{TE} = \frac{2\pi n_{TE} d}{\lambda}. \quad (5)$$

Any change in the value of n_{TE} for a fixed waveguide length will result in a corresponding change in the phase shift (a similar expression holds for the fundamental TM mode). n_{TE} depends, upon other factors on the waveguide geometry as well as core and cladding material refractive index n and this in turn can be changed through different mechanisms that include temperature, current injection, electro-optic effect, mechanical stress, and non-volatile phase actuation based on phase-change materials etc. For each one, detailed expressions of these dependences can be found in the literature for the main materials employed in integrated photonics [46]-[49]. Hence, through the application of an external control signal s over a suitable actuating device of length d grown on top of an integrated waveguide as shown in Figure 4(a), one can change the material refractive index in that localized region and therefore the propagation constant of any guided mode in general and the fundamental TE mode in particular. This means that the control signal s can change the phase shift experienced by the propagating signal. This embodiment of an actuator close to the integrated waveguide is known

as a *tunable phase shifter*, and it is a fundamental block of programmable circuits, as we shall see.

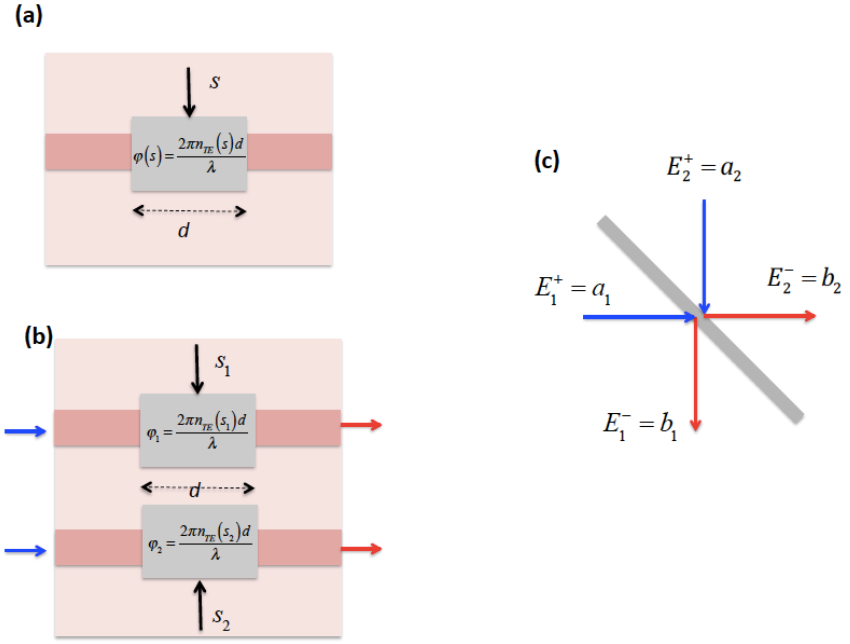

Fig. 4. (a) Schematic layout of an integrated phase shifter where an actuator placed on top of the waveguide generates a change in its refractive index $n_{TE}(s)$ and a subsequent phase shift by means of a control signal *s*. (b) a two waveguide tunable phase shifter. (c) Representation of bulk beamsplitter including input and output fields corresponding to its two surfaces. (Adapted from [49]).

Referring to (4), (5) and our previous discussion, the scattering matrix of a tunable phase shifter is given by:

$$\mathbf{S}=e^{-jq(s)}\begin{pmatrix}0 & 1\\ 1 & 0\end{pmatrix},\quad q(s)=\frac{2\pi n_{TE}(s)d}{\lambda}. \tag{6}$$

In practice, phase shifters are also implemented over two parallel waveguides in the so-called *differential push-pull* phase shifter scheme, with independent control signals s_1 and s_2 as shown in Figure 4(b). In this case and considering the propagation from left to right in each waveguide one can define the following scattering matrix:

$$\mathbf{S}_{DPP}\left(f_1,f_2\right)=\begin{pmatrix} e^{-j\frac{2\pi n_{TE}\left(s_1\right)d}{\lambda}} & 0 \\ 0 & e^{-j\frac{2\pi n_{TE}\left(s_2\right)d}{\lambda}} \end{pmatrix}=e^{-j\frac{\left(f_1+f_2\right)}{2}}\begin{pmatrix} e^{-j\frac{\Delta f}{2}} & 0 \\ 0 & e^{j\frac{\Delta f}{2}} \end{pmatrix}, \quad (7)$$

$$\begin{cases} f_1=\dfrac{2\pi n_{TE}\left(s_1\right)d}{\lambda} \\ f_2=\dfrac{2\pi n_{TE}\left(s_2\right)d}{\lambda} \end{cases},$$

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2.3 Beam-splitters, tunable directional couplers and 3-dB Mach Zehnder interferometers.

Figure 4(c) illustrates the operation of a bulk beam splitter [49]-[51]. Given an incident optical signal, these devices reflect part of it and transmit the rest. In practice, beam splitters are not employed in integrated programmable photonic circuits, but they are commonly used in their functional description as they play a similar role to integrated waveguide couplers. Our interest here is in the derivation of its scattering matrix as this will be useful to understand the modelling of complex multiport interferometers, which are treated in section 3.

The action of the beam splitter can be described by means of its field reflection and transmission coefficients in each face (i.e., r_{11}, t_{21} and r_{22}, t_{12} respectively. Referring to Figure 4(c):

$$\begin{aligned} E_1^- &= r_{11}E_1^+ + t_{12}E_2^+, \\ E_2^- &= t_{21}E_1^+ + r_{22}E_2^+. \end{aligned} \quad (8)$$

Hence, the scattering matrix is:

$$\mathbf{S}=\begin{pmatrix} r_{11} & t_{12} \\ t_{21} & r_{22} \end{pmatrix}. \quad (9)$$

Reciprocity requires that **S** is symmetric and hence:

$$t_{21}=t_{12}=t. \quad (10)$$

Furthermore, if the beam splitter is assumed to be lossless, then:

$$\begin{aligned} &\left|r_{11}\right|^2+\left|t\right|^2=1, \\ &\left|r_{22}\right|^2+\left|t\right|^2=1, \\ &\left|r_{11}t\right|e^{j(\phi_{12}-\phi_{11})}+\left|r_{22}t\right|e^{j(\phi_{22}-\phi_{21})}=0. \end{aligned} \quad (11)$$

The first two expressions in (11) imply that:

$$\left|r_{11}\right|^2=\left|r_{22}\right|^2=\left|r\right|^2=1-\left|t\right|^2, \quad (12)$$

while the third, together with (12), imposes a phase shift condition to be fulfilled by the transmission and reflection coefficients:

$$f_{12} - f_{11} - f_{22} + f_{21} = \pm(2k+1)\pi, k \in N, \tag{13}$$

For the sake of simplicity, we take the arbitrary choice $\phi_{11} = \phi_{22} = 0$ and $k = 0$, with a positive sign. Hence, we have:

$$2\theta = \pi \Rightarrow \theta = \frac{\pi}{2} \tag{14}$$

Hence, the scattering matrix of the lossless bulk beam splitter is given by:

$$\mathbf{S} = \begin{pmatrix} r & jt \\ jt & r \end{pmatrix}; t = \sqrt{1 - r^2}, \tag{15}$$

Integrated couplers are essentially the waveguide equivalent of the beamsplitter and a fundamental building blocks in programmable circuits [12]-[24]. These devices are based on the coupling between field modes propagating within a specific localized region. There are two main types of couplers employed in integrated photonics: the directional coupler [45-51] and the multimode interference coupler (MMI) [52], [53]. Directional couplers are based on the coupling of the evanescent fields corresponding to the fundamental modes of two integrated waveguides in close proximity. This coupling provides a periodic coupling factor varying from zero to complete cross coupling along the direction of propagation. They are especially suitable for the implementation of 2x2 devices. MMI couplers are based on the interference between different modes propagating in a multimode region. The MMI coupler is based on the self-imaging principle, a property of multimode waveguides by which an input field profile is reproduced in single or multiple images at periodic intervals along the propagation direction of the guide. MMI devices are thus suitable for implementing *N*x*N* couplers. We briefly review the operating principles and main design equations of both types of couplers.

Directional couplers are based on the coupling between the evanescent fields of the co-propagating fundamental modes of two waveguides placed in close proximity as shown in Figures 5(a) and 5(b) [45], [49].

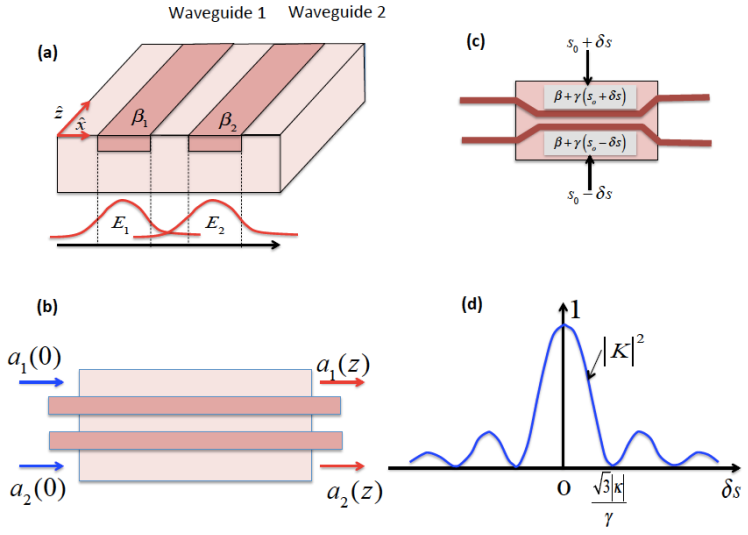

Fig. 5. Schematic (a) cross-section and lateral and (b) top view of a directional coupler. (c) Tunable dual drive directional coupler layout including common mode and differential control signals. (d) Tuning curve for the coupling constant value of a reconfigurable directional coupler versus the differential bias signal. (Adapted from [49])

Directional couplers can be designed so a wave launched in one guide can be partially or completely transferred to the other and vice-versa. In this sense, they behave as an integrated beam splitter. Furthermore, this transfer can be controlled by means of an external control signal enabling the so-called tunable directional couplers.

For the description of the directional coupler, we consider Figure 5(a) and two forward propagating modes a_1 and a_2 of waveguides 1 and 2 respectively (i.e., we only take the first member in (1)), which, in absence of coupling have propagating constants β_1 and β_2 and fulfil the equations [45]-[49]:

$$\begin{aligned} \frac{da_1}{dz} &= -jb_1a_1 + k_{12}a_2 \\ \frac{da_2}{dz} &= -jb_2a_2 + k_{21}a_1 \end{aligned} \quad . \tag{16}$$

where κ_{12} and κ_{21} are the coupling coefficients from waveguide 2 to waveguide 1 and from waveguide 1 to waveguide 2, respectively. The solution of (16) for a coupler with a coupling length region given by z can be found in several classical textbooks [45],[4],[50]: is given by:

$$\begin{aligned} &\begin{pmatrix} a_1(z) \\ a_2(z) \end{pmatrix} = \mathbf{S}_{TCD}\left(q = f\left(b_1, b_2, k\right)\right)\begin{pmatrix} a_1(0) \\ a_2(0) \end{pmatrix} \\ &\mathbf{S}_{TCD}\left(q = f\left(b_1, b_2, k\right)\right) = e^{-j\frac{(b_1+b_2)z}{2}}\begin{pmatrix} e^{j\jmath(\Delta b)}\cos(q/2) & j\sin(q/2) \\ j\sin(q/2) & e^{-j\jmath(\Delta b)}\cos(q/2) \end{pmatrix} \\ &K = \left(\frac{k\sin b_o z}{b_o}\right)^2 = \sin^2(q/2) \\ &\Delta b = b_2 - b_1 \\ &b_o = \sqrt{\left(\frac{\Delta b}{2}\right)^2 + k^2} \\ &\jmath(\Delta b) = \tan^{-1}\left[\frac{\Delta b}{2b_o}\tan b_o z\right] \end{aligned} \tag{17}$$

with $\kappa_{12} = \kappa_{21} = j\kappa$.

In many practical cases, directional couplers are made out by using identical waveguides and therefore $\Delta\beta = 0$, which simplifies (17) to the well-known relation:

$$\begin{aligned} &\mathbf{S}_{TDC}\left(b, q\right) = e^{-jbz}\begin{pmatrix} \cos(q/2) & j\sin(q/2) \\ j\sin(q/2) & \cos(q/2) \end{pmatrix} \\ &K = \sin^2 b_o z = \sin^2\left(\frac{q}{2}\right) \end{aligned} \tag{18}$$

Note however that tunable directional couplers are required for applications in programmable photonics and that tunability is achieved by means of inducing a refractive index asymmetry in the two optical waveguides. Therefore, the matrix form given by (17) needs to be employed. In this case, the coupling constant and overall phase shift of a directional coupler can be independently tuned by means of two control signals that will induce a propagation constant mismatch between the two waveguides in the coupler as illustrated in Figure 5(c). We assume that:

$$\begin{aligned} \beta_1 &= \beta + \gamma\left(s_o + \delta s\right), \\ \beta_2 &= \beta + \gamma\left(s_o - \delta s\right), \end{aligned} \tag{19}$$

where s_o is a common tunable bias signal and δs is the differential signal applied to the transducers. We further assume that under no applied control signals the coupler length is designed so the device is in cross-state, (i.e., $z = \pi/2|\kappa|$). Under these conditions, the differential signal change to achieve the transition to the bar state is [46], [50]:

$$\delta s = \frac{\sqrt{3}|\kappa|}{\gamma}. \tag{20}$$

Hence, the complete transition ($0<K<1$) is achieved for ($0<\delta s<\sqrt{3}|k|/g$) as shown in Figure 5(d). Moreover, the overall phase shift is given by:

$$\Delta = \left(\frac{\beta_1 + \beta_2}{2}\right) = \beta + \gamma s_o. \tag{21}$$

Note however that a residual phase shift is experienced by signals that does not change the propagation waveguide. This phase shift is given by:

$$\varphi\left(\delta s\right) = \tan^{-1}\left[\frac{1}{\sqrt{1+\left(\frac{|\kappa|}{\gamma\delta s}\right)^2}}\tan\left(\frac{\pi\gamma\delta s}{2|\kappa|}\sqrt{1+\left(\frac{|\kappa|}{\gamma\delta s}\right)^2}\right)\right]. \tag{22}$$

An alternative to tunable directional couplers that is the most widely option employed for the implementation of programmable integrated circuits is the tunable 3-dB balanced Mach-Zehnder interferometer. A layout of this device is shown in Figure 6(a) and it is composed of two 3-dB couplers that form a balanced Mach-Zehnder Interferometer (MZI) [54], where each arm incorporates a tunable phase shifter. The 3-dB splitters are usually implemented using multimode interference couplers (MMIs). The MMI is based on a step-index multimode waveguide shown in Figure 6(b) [52]-[54]. The structure displayed in the figure has a length L, a width W and a refractive index n, with input/output waveguide ports incorporated at the extreme surfaces. 3 dB MMIs splitters have the following 2x2 scattering matrix:

$$\mathbf{S} = \frac{je^{j\varphi_o}}{\sqrt{2}}\begin{pmatrix} 1 & j \\ j & 1 \end{pmatrix}, \tag{23}$$

where φ_o is a common phase factor.

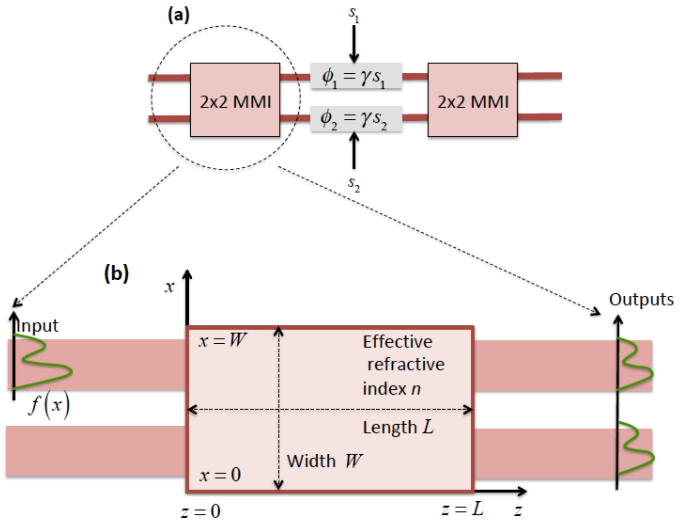

Fig. 6. (a) Tunable 3-dB MZI coupler, (b) layout of the 2x2 3-dB Multimode Interference (MMI) coupler used to embed the balanced interferometer (Adapted from [49]).

If we assume that the transduction mechanism leading to the phase shifting in each arm can be described by $\phi_i = \gamma s_i$, $i = 1, 2$, where γ is the transduction coefficient, then calling:

$$\begin{aligned} \Delta &= 2\varphi_o + \frac{\gamma\left(s_1 + s_2\right)}{2}, \\ \theta &= \gamma\left(s_2 - s_1\right) + \pi, \end{aligned} \tag{24}$$

which leads to:

$$\mathbf{S}_{MZI}\left(\Delta,\theta\right) = -\,je^{j\Delta}\begin{pmatrix} \cos\left(\theta/2\right) & \sin\left(\theta/2\right) \\ \sin\left(\theta/2\right) & -\cos\left(\theta/2\right) \end{pmatrix}. \tag{25}$$

Equation (25) represents a tunable coupler where the coupling constant $K=sin^2\theta$ and the overall phase shift Δ can be independently tuned **using the two control signals s_1 and s_2 according to the system of two equations** and two unknowns given by (30).

2.4 Reversible 2x2 Gates

Digital electronic FPGAs are composed of a set of interconnected configurable logic elements (CLEs), input/output devices and high-performance blocks (HPBs), as shown in Figure 7(a). It is customary to employ elementary *irreversible* gates [55], [56] for bit processing using Boolean logic as building blocks for CLEs [4], as shown. These gates are characterized by the fact that the number of input ports is 2 while the number of output ports is 1. Figures 7(b) and (c) show some basic examples of these gates, which are characterized by their so-called truth tables. The term irreversible reflects the fact that the input cannot be deduced from the output unambiguously. By cascading thousands of these gates one can build extremely complex combinatorial and sequential Boolean circuits.

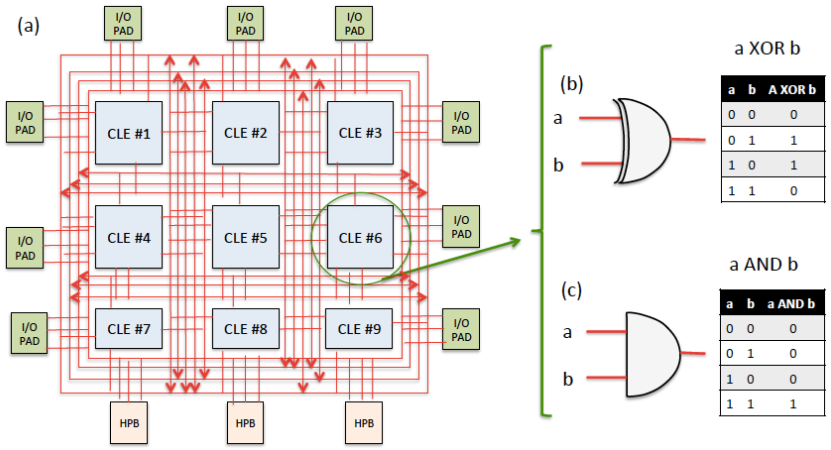

Fig. 7. (a) Schematic layout of an electronic FPGA containing a set of interconnected Configurable Logic Elements (CLEs), Input/output Pads and High-performance Blocks (HPBs) and Examples of irreversible logic Boolean gates employed in the design of CLEs (b) XOR gate, (c) AND gate. (Adapted from [55]).

Reversible gates [56], [57] feature the same number of input and output ports and are characterized as well by truth tables. In this case, the input state can be deduced from the gate output as the gate operation can also be described by a unitary matrix transformation U. If $\boldsymbol{I}$ and $\boldsymbol{O}$ denote respectively the input and output vectors, the $\boldsymbol{O} = \boldsymbol{UI}$, hence $\boldsymbol{I} = \boldsymbol{U^{-1}O}$, but since $\boldsymbol{U}$ is unitary its inverse is given by the Hermitian conjugate. Reversible gates can be employed to perform digital Boolean operations but this process is inefficient compared to the use of irreversible gates as it entails the use of fixed or *ancilla* bits and produces as well garbage bits, which are not useful to the rest of the computation [58]. As a consequence, reversible gates are not employed in digital electronics.

The situation in photonics is however quite different. First, reversible gates have found an application niche in the field of photonics quantum computation [13], [56]-[58]. The two main reasons are firstly that quantum computation does not rely on in Boolean logic but rather on the use of linear unitary transformations as a qubit $|\psi\rangle = \alpha|0\rangle + \beta|1\rangle$ resembles more an analog than a digital signal as the multiplying complex coefficients α and β states can be continuously changed. Indeed, the qubit processing by the logic gate is really carried altering its wave-like and not its particle-like properties. The second reason and equally important is that reversible gates can be engineered to exploit the garbage bits as heralding ports [56] to certify the correct operation of the gate. Since programmable integrated photonic circuits for classical signal processing applications handle, as we will see in the next section, analog signals as well it makes sense therefore to consider the use of reversible gates as a basic building block to implement complex circuit structures just much in the same way as they are employed for quantum photonics.

We now briefly consider the formalism for the implementation of complex programmable photonic circuits taking as basic building blocks a special family of 2x2 reversible gates known as rotation gates [56], [57]. We first illustrate how these gates isomorphically correspond to some of the photonic components addressed in the prior subsection, such as directional and 3-dB tunable couplers and push-pull phase shifters. We then show how these can be concatenated in two compact forms to implement tunable arbitrary 2x2 unitary transformers. These unitaries can be in turn, as we will see in section 5, assembled into two-dimensional configurations to feature FPPGAs.

We start by considering the basic 2x2 Pauli matrices given by [56]-[59]:

$$\sigma_o = I = \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix}; \sigma_1 = X = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix}$$
$$\sigma_2 = Y = \begin{pmatrix} 0 & -j \\ j & 0 \end{pmatrix}; \sigma_3 = Z = \begin{pmatrix} 1 & 0 \\ 0 & -1 \end{pmatrix} \quad (26)$$

Two-dimensional rotation matrices (by an angle θ) around axes x, y and z are defined by the following transformations:

$$R_x(\theta) = e^{-j\frac{\theta}{2}X};\ R_y(\theta) = e^{-j\frac{\theta}{2}Y};\ R_z(\theta) = e^{-j\frac{\theta}{2}Z}. \quad (27)$$

Using basic operator theory, it can be readily shown that:

$$R_x(q) = \begin{pmatrix} \cos(q/2) & j\sin(q/2) \\ j\sin(q/2) & \cos(q/2) \end{pmatrix}.$$
$$R_y(q) = \begin{pmatrix} \cos(q/2) & -\sin(q/2) \\ \sin(q/2) & \cos(q/2) \end{pmatrix} \quad (28)$$
$$R_z(q) = \begin{pmatrix} e^{-j(q/2)} & 0 \\ 0 & e^{j(q/2)} \end{pmatrix}$$

The reader can identify strong similarities between these and (25), (18) and (7) derived in the prior subsection, indicating that these rotations can be implemented in the photonics domain respectively by a directional coupler, a 3-dB Mach-Zehnder tunable coupler and two parallel waveguides including two phase shifters configured in push-pull mode, as shown in Figure 8. This is in fact the case although small modifications need to be introduced into these devices as shown in the figure and which we now outline.

It is immediate to verify that:

$$R_x(q) = \begin{pmatrix} \cos(q/2) & j\sin(q/2) \\ j\sin(q/2) & \cos(q/2) \end{pmatrix} = e^{-j\frac{(b_1+b_2)z}{2}} e^{j\frac{(b_1+b_2)z}{2}}$$
$$\begin{pmatrix} e^{jj(\Delta b)/2} & 0 \\ 0 & e^{-jj(\Delta b)/2} \end{pmatrix} \begin{pmatrix} e^{jj(\Delta b)}\cos(q/2) & j\sin(q/2) \\ j\sin(q/2) & e^{-jj(\Delta b)}\cos(q/2) \end{pmatrix} \begin{pmatrix} e^{jj(\Delta b)/2} & 0 \\ 0 & e^{-jj(\Delta b)/2} \end{pmatrix} = \quad (29)$$
$$= e^{j\frac{(b_1+b_2)z}{2}} e^{j2j_o} \mathbf{S}_{DPP}\left(j_o + j(\Delta b), j_o - j(\Delta b)\right) \mathbf{S}_{TDC}\left(q = f(b_1, b_2, k)\right) \mathbf{S}_{DPP}\left(j_o + \frac{j(\Delta b)}{2}, j_o - \frac{j(\Delta b)}{2}\right)$$

Note that since φ_o can be arbitrarily set, $2\varphi_o = -(\beta_1+\beta_2)z/2$, then:

$$R_x(q) = \mathbf{S}_{DPP}\left(j_o + j(\Delta b), j_o - j(\Delta b)\right) \mathbf{S}_{TDC}\left(q = f(b_1, b_2, k)\right) \mathbf{S}_{DPP}\left(j_o + j(\Delta b), j_o - j(\Delta b)\right). \quad (30)$$

Therefore, a rotation around the x axis can be implemented by a tunable directional coupler embedded by two identical push-pull waveguide phase shifters as shown in Figure 8(a). In a similar way:

$$R_y(q)=\begin{pmatrix}\cos(q/2) & -\sin(q/2)\\ \sin(q/2) & \cos(q/2)\end{pmatrix}=je^{-jD}\left(-je^{jD}\right)\begin{pmatrix}\cos(q/2) & \sin(q/2)\\ \sin(q/2) & -\cos(q/2)\end{pmatrix}\begin{pmatrix}1 & 0\\ 0 & -1\end{pmatrix}=$$
$$=je^{-jD}e^{jj_o}\mathbf{S}_{MZI}(D,q)\mathbf{S}_{DPP}(j_o+p,j_o-p) \tag{31}$$

Note now that since φ_o can be arbitrarily set so $\varphi_o = \Delta-\pi/2$ then:

$$R_y(q)=\mathbf{S}_{MZI}(D,q)\mathbf{S}_{DPP}(j_o+p,j_o-p) \tag{32}$$

In other words, a rotation around the y axis can be implemented by a 3-dB MZI tunable coupler preceded by a push-pull waveguide phase shifter as shown in Figure 8(b). Finally:

$$R_z(q)=\begin{pmatrix}e^{-j(q/2)} & 0\\ 0 & e^{j(q/2)}\end{pmatrix}=\mathbf{S}_{DPP}(q,-q). \tag{33}$$

Hence, a rotation around the z axis can be implemented by a push-pull waveguide phase shifter with zero common phase bias as shown in Figure 8(c).

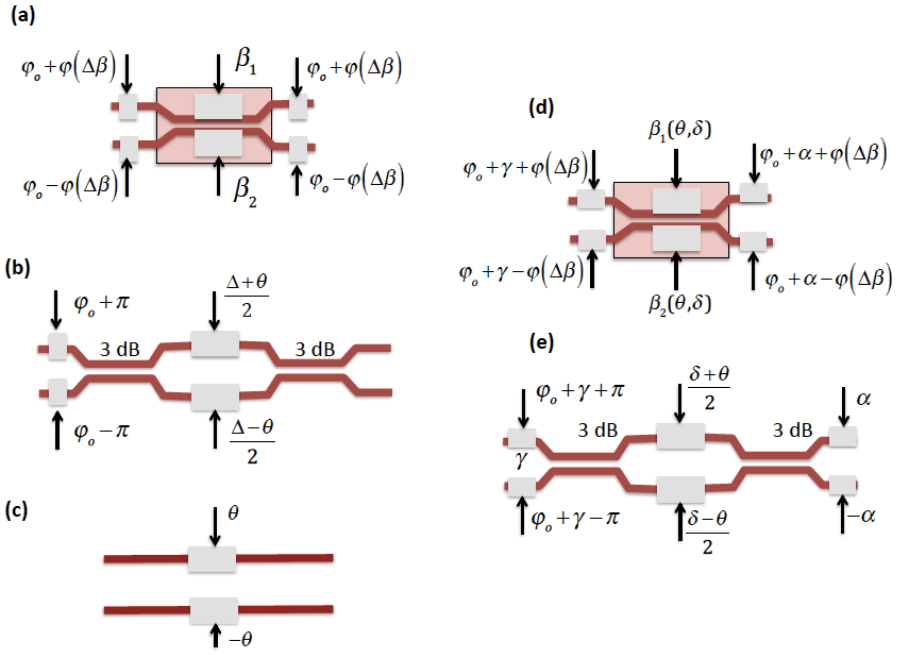

Fig. 8. (a) Schematic layout for the photonic implementation of $R_x(\theta)$ based on a tunable directional coupler. (b) Schematic layout for the photonic implementation of $R_y(\theta)$ based on a tunable 3-dB MZI coupler. (c) Schematic layout for the photonic implementation of $R_z(\theta)$ based on a differential push-pull phase shifter. (d) Integrated photonic implementation of an arbitrary unitary 2x2 matrix transform using a cascade of $R_x(\theta)$ and $R_z(\theta)$ rotations. (e) Integrated photonic implementation of an arbitrary unitary 2x2 matrix transform using a cascade of $R_y(\theta)$ and $R_z(\theta)$ rotations (After [59]).

Rotation operators and their implementations are fundamental since by virtue of the Euler theorem [56], [57] any arbitrary 2x2 unitary matrix U can be expressed in either of the two following sequential rotation matrix concatenation forms:

$$U = e^{j\delta} R_z(\alpha) R_y(\beta) R_z(\gamma),$$
$$U = e^{j\delta} R_z(\alpha) R_x(\beta) R_z(\gamma), \tag{34}$$

where α, β, γ and δ are a set of four real and independent numbers. This means that compact configurations consisting of a preceding and succeeding differential phase shifting units enclosing either a dual-drive directional coupler or a 3-dB MZI unit as shown in Figures 8(d) and 8(e), respectively, can be employed to implement these arbitrary units.

The importance and applicability of reversible gates as basic building blocks in programmable photonics will become clear to the reader in sections 3 to 5.

3. Multiport interferometers

Integrated multiport interferometers were initially conceived and designed to implement fixed feed-forward linear optics unitary transformations between *N* input and *N* output ports to support mode transformations. They have been especially employed in quantum optics. However, the rapid development of this field and the possibility of applying these structures to other classical areas, such as deep learning and neurophotonics, stimulated the development of devices capable of supporting any arbitrary linear transformation by suitable programming and furthermore no longer restricted to square matrix transformations and unitary operators. In this section, we first review some basic concepts on unitary *NxN* matrices and then we will describe in detail the basic design principles and integrated optics implementations of the two most popular designs for multiport interferometers; the triangular and the rectangular designs.

3.1 Basic concepts on unitary matrices

Multiport optical interferometers implement unitary transformations between *N* input and *N* output ports [21]-[23], [59]. It is useful to review some salient properties of these transformations. If we assume a *NxN* unitary transformation *U*, then $UU^{\dagger} = U^{\dagger}U = I$, where † denotes the Hermitian conjugate and *I* the *N*x*N* identity matrix. We shall now describe five important properties of unitary matrices *U* that are relevant in the design of multiport interferometers. The complete demonstrations of these properties can be found in [59].

Property 1: *If all the matrix coefficients in a given row i are zero except u_{ii}, that is $u_{ij} = 0$ for $j \neq I$, then all the matrix coefficients in column i are zero, except u_{ii}, that is, $u_{ji} = 0$ for $j \neq i$. Furthermore, u_{ii} is a modulus one complex number.*

Property 2: *if all the matrix coefficients in a given column i are zero except u_{ii}, that is $u_{ji} = 0$ for $j \neq i$, then all the matrix coefficients in row i are zero, except u_{ii}, that is, $u_{ij} = 0$ for $j \neq i$ and, again, u_{ii} is a modulus one complex number.*

One matrix of special interest is the *generalized ZY cascade rotation matrix* in the plane defined by rows *m* and *n*:

$$T_{mn}(\varphi,\theta)=\begin{pmatrix} 1 & 0 & \cdots & \cdots & \cdots & \cdots & \cdots & 0 \\ 0 & 1 & \cdots & \cdots & \cdots & \cdots & \cdots & 0 \\ \vdots & \vdots & \ddots & \cdots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & \cdots & e^{j\varphi}\cos\theta & \cdots & -\sin\theta & \cdots & 0 \\ \vdots & \vdots & \cdots & \vdots & \ddots & \vdots & \cdots & 0 \\ 0 & 0 & \cdots & e^{j\varphi}\sin\theta & \cdots & \cos\theta & \cdots & 0 \\ \vdots & \vdots & \cdots & \cdots & \cdots & \cdots & \ddots & \vdots \\ 0 & 0 & \cdots & 0 & \cdots & 0 & \cdots & 1 \end{pmatrix}\begin{matrix} 1 \\ 2 \\ \vdots \\ m \\ \vdots \\ n \\ \vdots \\ N \end{matrix}, \qquad (35)$$

which, according to (32) and (33), corresponds to a tunable 3-dB MZI coupler between inputs *m* and *n* and outputs *n* and *m* in this order that performs a y-wise rotation of θ radians preceded by a phase shifter performing the *z*-wise rotation of φ radians. As it can be immediately checked, $T_{mn}(\varphi,\theta)$ is unitary and its inverse is given by:

$$T_{mn}^{-1}(\varphi,\theta)=\begin{pmatrix} 1 & 0 & \cdots & \cdots & \cdots & \cdots & \cdots & 0 \\ 0 & 1 & \cdots & \cdots & \cdots & \cdots & \cdots & 0 \\ \vdots & \vdots & \ddots & \cdots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & \cdots & e^{-j\varphi}\cos\theta & \cdots & e^{-j\varphi}\sin\theta & \cdots & 0 \\ \vdots & \vdots & \cdots & \vdots & \ddots & \vdots & \cdots & 0 \\ 0 & 0 & \cdots & -\sin\theta & \cdots & \cos\theta & \cdots & 0 \\ \vdots & \vdots & \cdots & \cdots & \cdots & \cdots & \ddots & \vdots \\ 0 & 0 & \cdots & 0 & \cdots & 0 & \cdots & 1 \end{pmatrix}\begin{matrix} 1 \\ 2 \\ \vdots \\ m \\ \vdots \\ n \\ \vdots \\ N \end{matrix} \qquad (36)$$

and corresponds to a tunable 3-dB MZI coupler between inputs *m* and *n* and outputs *n* and *m* that performs a y-wise rotation of $-\theta$ radians succeeded by a phase shifter the *z*-wise rotation of $-\varphi$ radians.

Property 3: *The product $UT^{-1}_{mn}(\varphi,\theta)$ is a unitary matrix that leaves all the columns in U unaltered with the exception of columns m and n and we can choose values for (φ,θ) to null whatever (but only one) coefficient in these columns.*

Property 4: *The product $T_{mn}(\varphi,\theta)U$ is a unitary matrix that leaves all the rows in U unaltered with the exception of rows m and n and we can choose values for (φ,θ) to null whatever (but only one) coefficient in these rows.*

Property 5: *If D is a diagonal matrix with $d_{jj} = e^{j\alpha_j}$, then for any $T^{-1}_{mn}(\varphi,\theta)$ one can find a diagonal matrix D' with $d_{jj} = e^{j\delta_j}$ and a matrix $T_{mn}(\varphi',\theta')$ such that $T^{-1}_{mn}(\varphi,\theta)D = D'T_{mn}(\varphi',\theta')$.*

3.2 Triangular interferometers

The triangular arrangement for a multiport programmable interferometer was proposed by Reck and co-workers in 1994 [21]. It is based on the iterative use of Property 3 described in the previous subsection to make zero all the off-diagonal elements in the unitary matrix *U*.

In a first step, *U* is multiplied from the right by a succession of matrices $T^{-1}_{Nq}(\varphi_q,\theta_q)$ with $q = N-1, \ldots 1$. This product is equivalent to the attachment of successive 2x2 tunable beam splitters to ports *q* and *N*. By making use of Property 3 after each product to null element (*q*,*N*) and then property 1, we have:

$$U(N)T_{NN-1}^{-1}T_{NN-2}^{-1}\cdots T_{N1}^{-1}=\begin{pmatrix} * & * & * & * & 0 \\ * & * & * & \cdots & 0 \\ \cdots & \cdots & \cdots & \cdots & 0 \\ * & * & * & * & 0 \\ 0 & 0 & 0 & 0 & e^{j\alpha_N} \end{pmatrix}=\begin{pmatrix} U'(N-1) & \mathbf{0} \\ \mathbf{0} & e^{j\alpha_N} \end{pmatrix}\cdot \tag{37}$$

Note that the effective dimension of the resulting matrix has been reduced to N-1. We can now apply the same procedure based on Property 3, bearing in mind that the elements in the last row will remain zero and thus will not be affected by successive multiplications from the right, to reduce the dimensions to N-2, N-3 and finally to 1, leading to:

$$U(N)T_{NN-1}^{-1}T_{NN-2}^{-1}\cdots T_{N1}^{-1}\cdots T_{32}^{-1}T_{31}^{-1}T_{21}^{-1}=\begin{pmatrix} e^{j\alpha_1} & 0 & 0 & 0 & 0 \\ 0 & e^{j\alpha_2} & 0 & \cdots & 0 \\ \cdots & \cdots & \cdots & \cdots & 0 \\ 0 & 0 & 0 & e^{j\alpha_{N-1}} & 0 \\ 0 & 0 & 0 & 0 & e^{j\alpha_N} \end{pmatrix}=D\,. \tag{38}$$

Hence, as D is a diagonal (and unitary) matrix, we have:

$$U^{-1}(N)=T_{NN-1}^{-1}T_{NN-2}^{-1}\cdots T_{N1}^{-1}\cdots T_{32}^{-1}T_{31}^{-1}T_{21}^{-1}D^{-1}, \tag{39}$$

which finally yields:

$$U(N)=DT_{21}T_{31}T_{32}\cdots T_{N-1N-2}T_{N1}\cdots T_{NN-2}T_{NN-1}=D\prod_{i=2}^{N}\left[\prod_{j=1}^{i-1}T_{ij}\right]. \tag{40}$$

Equation (40) provides the desired decomposition of the unitary operator into a set of beam splitter operations completed by a phase shifting operation. Each beam splitter relates two inputs and two outputs of the overall structure.

Reck and co-workers proposed for $T_{mn}(\varphi_{mn},\theta_{mn})$ the bulk optics configuration shown in Figure 9 (a), which is represented in chip layouts by the symbol shown in Figure 9 (b). Figures 9 (c) and 9(d) show as an example, the decomposition and the layout for a general 4x4 unitary matrix. The practical implementation of this method involves a triangular array of beam splitters, each diagonal row in the triangle reducing the effective dimension of the Hilbert space by one. The maximum number of required beam splitters to implement $U(N)$ is given by $N(N-1)/2$. For later comparison with the rectangular design, it is useful to define the *depth* of an interferometer [22] as the longest path through the interferometer, enumerated by counting the number of beam splitters traversed by that path. In the case of the triangular interferometer, this corresponds to the edges of the triangle and is given by $(N-1)+(N-2)=2N-3$.

Triangular interferometers can be integrated on a chip as suggested by Miller [11], [12] by replacing the tunable bulk optics beam splitter shown in Figure 9 (a) by its equivalent version in integrated optics, which is the tunable basic unit (TBU) shown in Figure 8(a)-(b) or Figures 8 (d)-(e). Up to now, this has been the preferred option for implementing most reconfigurable integrated optical quantum circuits [59], [13], [15], [60], [61] and some classical applications as well [23], [62], [12], [26]. Figure 9 (e) illustrates this equivalence for the 4x4 unitary transformer discussed above. The triangular interferometer has been reported in several material Platforms. We show now some examples and provide further discussion of these and other implementations in section 7, in the context of their applications.

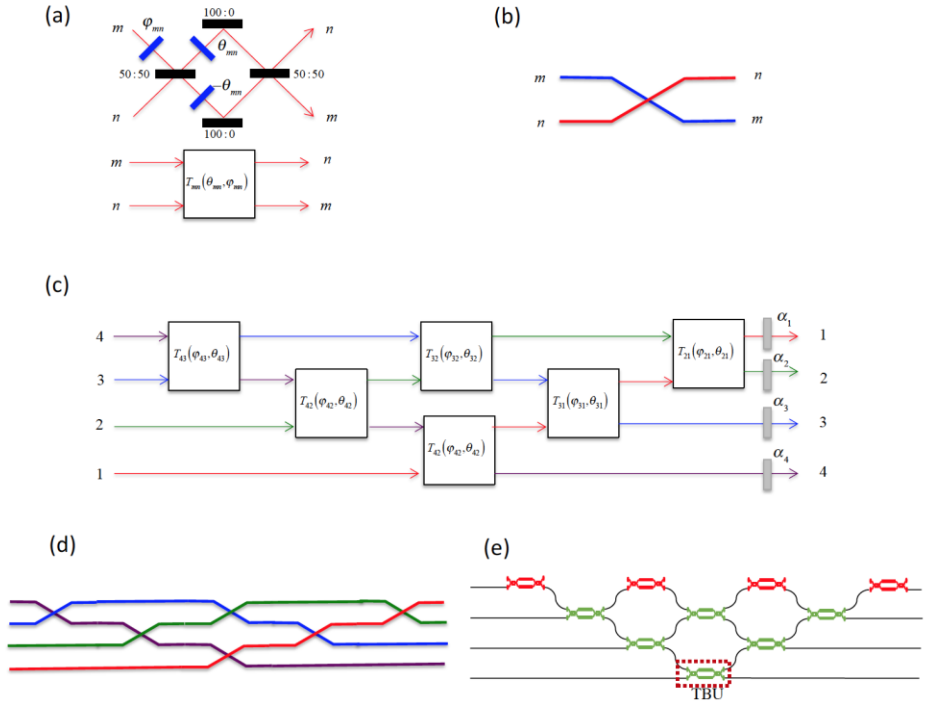

Fig. 9. (a) Bulk optics implementation of a tunable beam splitter (Adapted from [21]). (b) Symbol representation of the beam splitter layout. (c) Triangular decomposition implementing a general $U(4)$ 4x4 unitary transformation and layout (d). Colours represent the propagation of a given input port. (e) $U(4)$ layout of Figure 8(d) and its implementation using MZI based TBUs. TBUs in red colour operate as phase shifters.

3.2 Rectangular interferometers

The rectangular universal *N*x*N* interferometer has been recently proposed [22]. This design is based on an alternative arrangement of $U(2)$ beam splitters and phase shifters and outperforms the triangular arrangement in a series of figures of merit, including the optical depth, which is half of that of the triangular design and robustness against optical losses.

In the triangular decomposition [21], *successive columns or rows of the U*(*N*) *matrix are nulled* using either only matrices (multiplied from the left) or only matrices (multiplied by the right) respectively, making sure that nulled elements of $U(N)$ are not affected by subsequent operations. The rectangular decomposition [22], proceeds by *nulling successive diagonals* of $U(N)$ by alternating between T_{mn} and T^{-1}_{mn} matrices where $m = n-1$, in such a way that every nulled diagonal in the matrix corresponds to one diagonal line of beam splitters through the interferometer. The sequence of and matrices must both correspond to the desired order of beam splitters in the interferometer and guarantee that the nulled elements of $U(N)$ are not affected by subsequent operations. This is illustrated as an example in Figure 10 for the case of a $U(5)$ interferometer [22].

The process [22], starts by nulling the bottom-left element of $U(5)$ (first diagonal) with the T^{-1}_{12} matrix, which, according to property 3 causes the first two columns of $U(5)$ to mix. This corresponds to adding the top-left beam splitter in the interferometer as shown in the right hand-side of Figure 10(b). We then null the second diagonal using a T_{34} matrix followed by a T_{45} matrix, which correspond to the two bottom-right beam splitters in the interferometer as shown in Figure 10(b). According to property 4, T_{34} mixes rows 3 and 4, and T_{45} mixes rows 4 and 5. Note that since both the (4,1) and (5,1) elements of $U(5)$ have been previously nulled, they are

not affected by T_{45}. We then proceed at every next step to null a successive diagonal of the updated $U(5)$ matrix by alternating between T_{mn} and $T^{1}{}_{mn}$ matrices, which corresponds to adding diagonal lines of beam splitters to the interferometer. This is shown in Figure 10 (d) and (e).

The final expression after the decomposition process is:

$$T_{45}T_{34}T_{23}T_{12}T_{45}T_{34}UT_{12}^{-1}T_{34}^{-1}T_{23}^{-1}T_{12}^{-1} = D. \tag{41}$$

However, taking property 5 into consideration, we finally have:

$$U = D'T_{34}T_{45}T_{12}T_{23}T_{34}T_{45}T_{12}T_{23}T_{34}T_{12}. \tag{42}$$

The decomposition in (42) corresponds to the multiport interferometer shown in Fig. 10 (f), and the values of the θ and ϕ of the T_{mn} matrices determine the values of the beam splitters and phase shifts that must be programmed to implement $U(5)$.

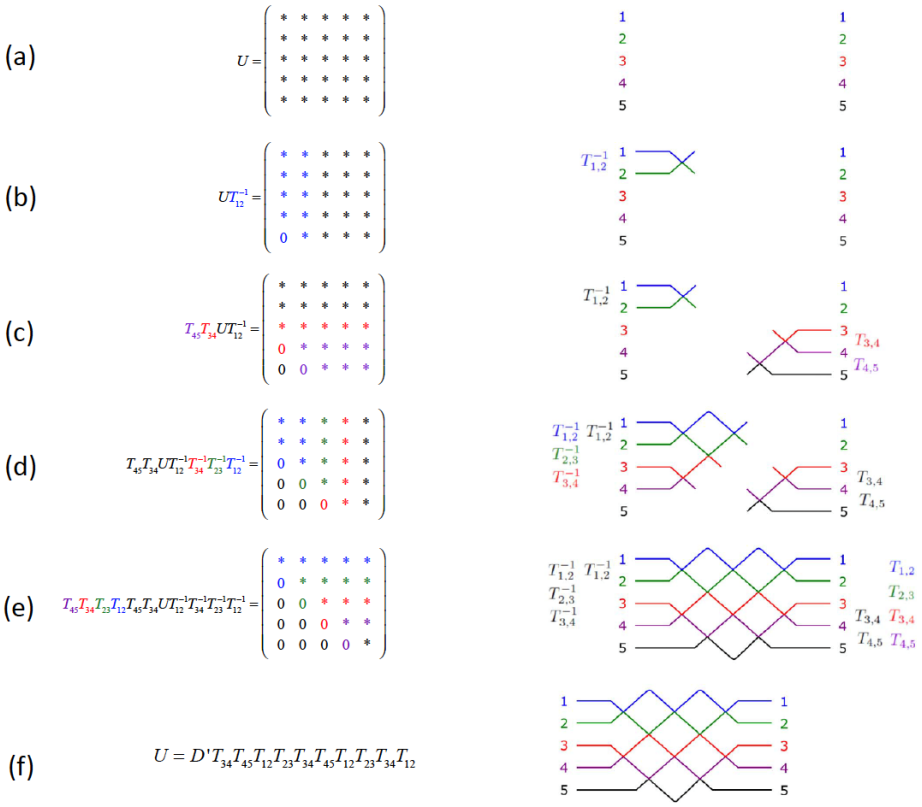

Fig.10. Illustration of the algorithm for programming a universal multiport interferometer for $U(5)$ interferometer. The left-hand side presents the decomposition procedure, and the right-hand side shows how the decomposition for building up the corresponding interferometer. (a) The starting point is any random unitary matrix $U(5)$ and a blank interferometer. (b)-(e) Successive stages of the implementation algorithm. (f) Final expression for $U(5)$ in terms of a cascade of $U(2)$ interferometers and a diagonal matrix. Reproduced from [22].

The rectangular interferometer requires $N(N\text{-}1)/2$ beam splitters to implement a $U(N)$ transformation, just like the triangular arrangement. However, its depth is only N, which is roughly half of those required for the triangular design and this leads to lower balanced losses, which are related to the propagation loss of the longest path in the interferometer [22]. In

addition, its symmetry leads to improved loss tolerance as related to the unbalanced loss, which is due to the different losses experienced by the signal propagating through the different paths of the interferometer. We provide more information regarding the comparative performance of these and other multiport interferometer later in this chapter.

Rectangular interferometers can also be integrated on a chip following a similar procedure to that of the triangular arrangement using, for instance, the tunable basic units of Figure 8. Figures 11 (a) and (b) show the layout of a $U(9)$ interferometer and its integrated optics design using 3-dB MZI TBUs. Due to their recent proposal, there have been few experimental reports of the rectangular interferometer. The first one was reported in [23], where a $U(4)$ interferometer was emulated in a silicon hexagonal waveguide mesh. Specific rectangular interferometer integrated designs have been very recently reported [63]. Figure 11 (c) shows the photograph of a modular set composed of 3 linear optical circuits. Each module consists of ten tunable MZIs placed side by side as shown in Figure 11 (d). Modules are to be tiled to build larger interferometers. For example, as we have seen above, N of such modules with at least $N/2$ MZI wide are enough to perform an arbitrary unitary transformation $U(N)$, with optimal circuit depth. In this case, the circuit was employed to implement up to $U(6)$ transformations for different applications.

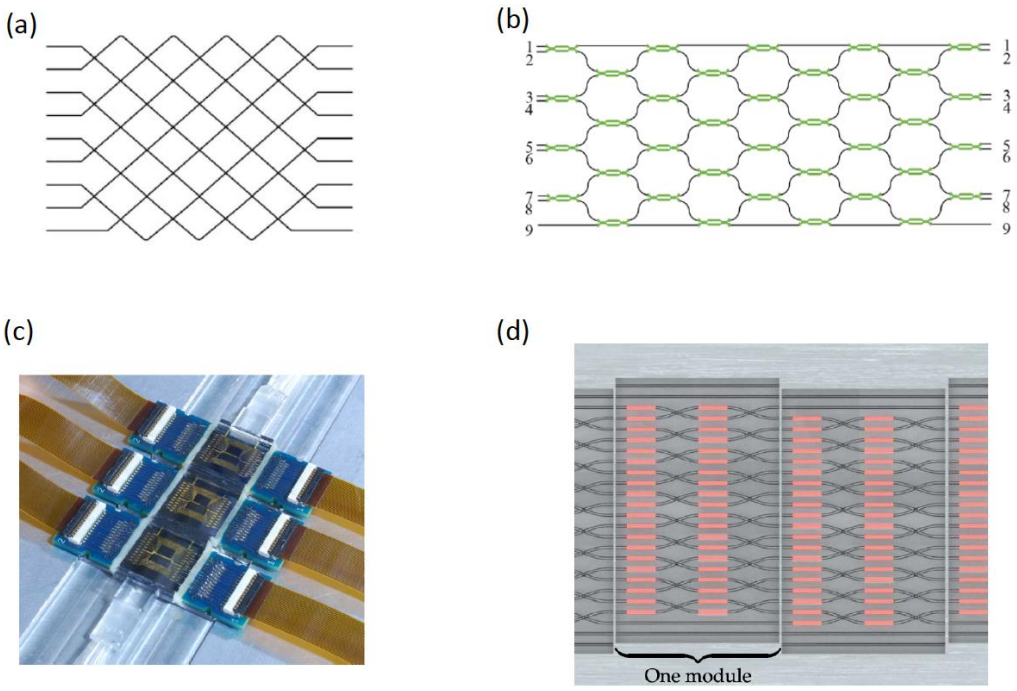

Fig. 11. Integrated rectangular interferometers. (a) Design Layout for a U(9) transformer (after [22]) and (b) implementation layout suitable for integrated optics using 3-dB MZIs (after [23]). (c) Photograph of a three-module silica on silicon rectangular interferometer. (d) Detail of an individual module showing 10 parallel TBUs. (c) and (d) are reproduced from [63].

4. Integrated photonic waveguide meshes

4.1 Concept of multipurpose Photonic waveguide mesh

Integrated waveguide meshes are 2D structures where a unitary cell composed of a subset of TBUs is spatially replicated [12]-[20], [64]-[66]. Several examples are shown in Figure 12. Each unitary cell is implemented by one or more sets of integrated waveguide pairs coupled by means of a TBU, the core of which can be any of the 2x2 reversible gate designs described in section 2 and shown in Figure 8. The application of external electrical signals to the TBU terminals allows the independent amplitude and phase control of the photonic signals coupled between the two waveguides. In particular, each TBU in the mesh can be configured to operate either as an optical crossbar switch or as an intermediate power divider. In this way, the combination of different TBUs in the 2D grid, -each individually configured as desired-, enables the synthesis of any kind of optical core circuit topology, including finite (FIR) and infinite impulse response (IIR) multiport interferometers and filters. Figures 12 (a) to 12 (c) show the main reported designs for waveguide meshes allowing for both feedforward and feed-backward propagation. Here the unit cell is composed by several TBUs following a geometrical configuration: square, hexagonal and triangular respectively. These are the most flexible waveguide mesh configurations allowing the implementation of both FIR and IIR multiport interferometers and filters. Although each mesh topology has inherent advantages, the hexagonal mesh is potentially the most flexible approach for implementing programmable photonic circuits, as we shall see later.

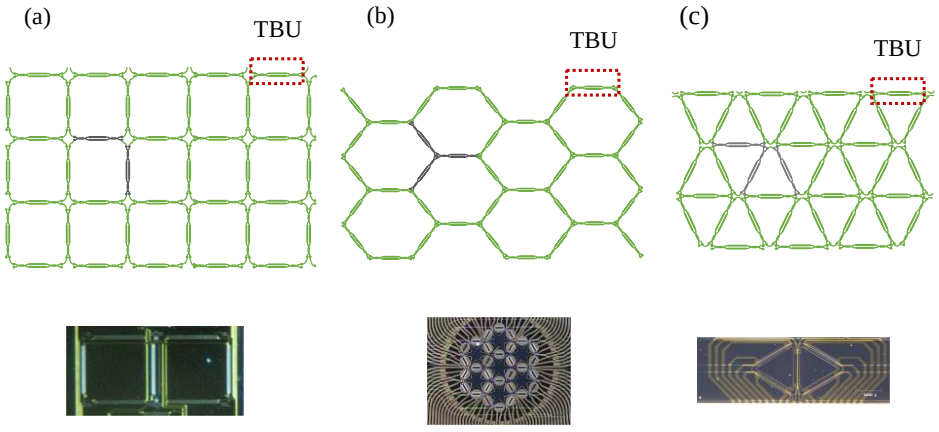

Fig. 12. Different integrated waveguide mesh arrangements: (a) Squared Feedforward/backward and implementation in Si_3N_4 (Photograph reproduced from [17]), (b) Hexagonal Feedforward/backward (Photograph reproduced from [20]), and implementation in SOI, (c) Triangular Feedforward/backward and implementation in Si_3N_4 (Photograph reproduced from [66]).

4.2 Rectangular, triangular and hexagonal waveguide meshes

Before considering the different geometries for waveguide meshes and their analysis, it is essential to remember that their primitive block, the TBU is implemented by means of a 2x2 reversible gate that must provide, independently, a complete splitting ratio tuning and phase response, [18], [64], [65]. By setting its control signals, this switching/tapping/dephasing mechanism can be potentially obtained in many different ways (i.e., exploiting thermo-optic, electro-optic of opto-mechanical effects, for example). The different alternatives for 2x2 reversible gates have been considered in section 2 and here, to provide some definitions, we consider, as an example, the case where the TBU is implemented by means of a 3-dB balanced MZI structure loaded with a thermal tuner on each arm, as illustrated in the lower part of Figure 13 (a). Nevertheless, the treatment is not restricted to this case and can be employed for alternative TBU structures and tuning mechanisms.

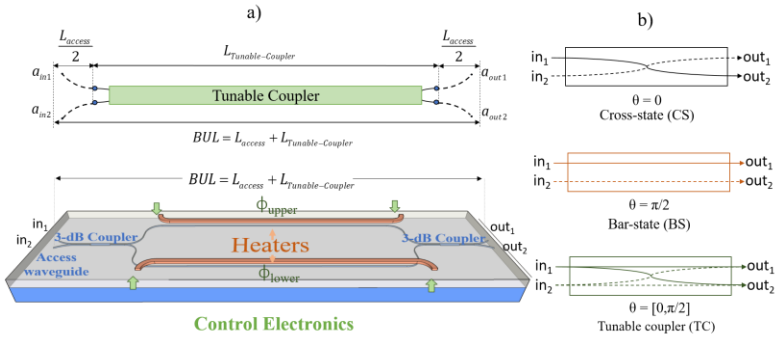

Fig. 13. (a) (Upper) Labelled schematic of a general tunable coupler acting as the basic building block of the mesh. The Basic Unit Length (BUL) is illustrated as the sum of the tunable coupler length and the arc length of the access waveguides. (Lower) Particular case of an integrated balanced MZI-based tunable coupler. (b) Signal flow for the different TBU configuration states. Figure reproduced from [18].

The upper part of Figure 13 (a) shows the TBU composed by the tunable coupler and its access (input/output) waveguides. The geometry of the latter is a function of the bending radius and varies for each mesh topology due to different angle between elements. The basic unit length (BUL) is, [18]:

$$BUL = L_{access} + L_{Tunable-Coupler}, \tag{43}$$

where L_{access} is the overall length of the access waveguide segment and $L_{Tunable\text{-}Coupler}$ is the length that describes the light-path in the tunable coupler. Most importantly, the time that takes the signal to go through the TBU is called the Basic Unit Delay (BUD):

$$BUD = n_g BUL / c, \tag{44}$$

where n_g is the waveguide group index and c is the speed of light in vacuum. Referring to Figure 13(b), the tunable basic unit can implement 3 different states: cross state switch (light path connects in_1 to out_2 and in_2 to out_1), bar state switch (light path connects in_1 to out_1 and in_2 to out_2) and tunable splitter.

For a balanced MZI loaded with heaters on both arms, the splitting ratio is obtained by increasing the effective index due to the Joule effect in the upper or lower arm, producing a ϕ_{upper} and ϕ_{lower} phase shift respectively. Once set, a common drive in both heaters will provide a common phase shift, leading to independent control of the amplitude ratio and the phase. The simplified device matrix is given by (25), where θ is (ϕ_{upper}- ϕ_{lower}) and Δ is (ϕ_{upper}+ ϕ_{lower}). A realistic description however must incorporate a general loss term γ that includes the effect of propagation losses in the access waveguides, the tunable coupler waveguide and the insertion losses for both 3-dB couplers. The device performance can be characterized in terms of the optical power by its insertion losses (IL) and optical crosstalk parameters (CT_{Bar} and CT_{Cross}):

$$\begin{aligned} IL(dB) &= 20\log_{10}(\gamma) = 10\log_{10}\left(\frac{|a_{out1}|^2 + |a_{out2}|^2}{|a_{in1}|^2 + |a_{in2}|^2}\right), \\ CT_{Bar/Cross}(dB)\Big|_{\substack{|a_{in1}|^2=1 \\ |a_{in2}|^2=0}} &= 10\log_{10}\left(\frac{|a_{out2,1}|^2}{|a_{out1,2}|^2}\right). \end{aligned} \tag{45}$$

These provide valuable information regarding the losses of the tunable units. Since they are connected in cascade configuration to build up the mesh, the overall *IL* of a certain synthetized device will be the sum of the *IL*s corresponding to the units across through which the light has travelled. As an example, if we assume overall device losses of 10 dB and IL of 0.2 dB for each TBU, then the longest path will be limited to 50 units. In the case of the optical crosstalk, the figure determines the leaking of signal that might cause optical reflections and undesired interferometric paths coupled to the desired photonic circuit to be programmed. In section 6 we address the impact that non-ideal behaviour of the TBU has over the waveguide mesh design. In order to reduce the footprint of the synthetized circuits, we allow the possibility of using all the TBU ports independently. For example, in a cross state set both in_1/out_2 and in_2/out_1 connections can be employed to configure a conventional crossing unit.

Square waveguide mesh arrangements were the first proposed mesh topology. In his pioneer work, Zhuang and co-workers [17] developed the concept where the interconnection of a large number of integrated balanced MZIs with two actuators could lead to the synthesis of a wide variety of PICs. This is achieved by discretizing conventional circuits into sets of TBUs with specific configurations. The proposed interconnection topology enables the routing of the optical signal path to follow orthogonal directions where the repetition of direction is not allowed for two consecutive TBUs. However, the topology is flexible enough to allow the synthesis of discrete waveguides or delay lines, tunable couplers as well as phase shifters and thus more complex building blocks like optical cavities and unbalanced MZIs. Fig. 14 illustrates the basic configuration of an optical ring resonator defined by a cavity length of 8 BULs, a delay line of 6 TBUs as well as an unbalanced MZI with arm lengths of 3 and 7 TBUs respectively.

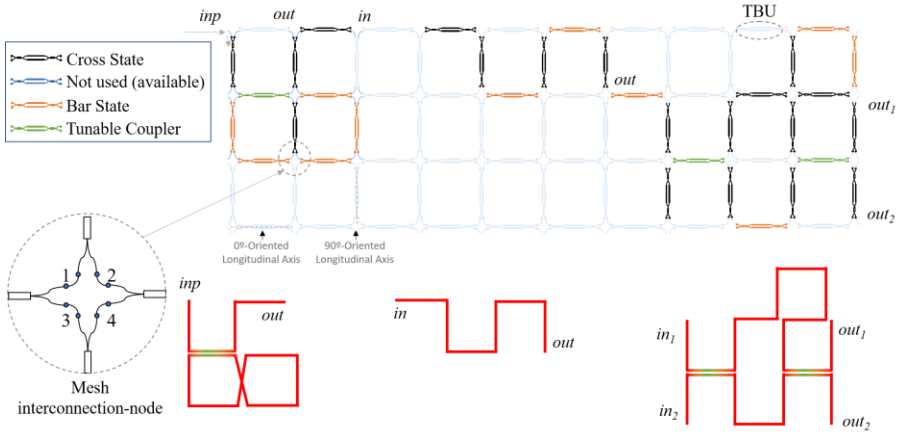

Fig. 14. Basic programming of medium-complex circuits in square waveguide mesh topology: delay line, unbalanced MZI and optical ring resonator (After [18]).

A second option is the triangular waveguide mesh topology proposed in [18]. In this case, three TBUs describing longitudinal orientations of 0º (horizontal plane), 60º and -60º are interconnected through 6 points resulting in a triangular pattern, as illustrated in Figure 15. Notice that the angle described by the longitudinal axis of two connected TBU is always 60º. Again, it can be shown that the interconnection scheme directly impacts on the degrees of freedom that the light has to flow across the structure and consequently the allowed light-paths and circuits that can be implemented inside the arrangement. These are particularly useful to increase the integration density of TBUs, and to implement optical cavities with reduced cavity lengths. The triangular pattern achieves a better discretization resolution of unbalanced filter structures as compared to the square topology. For more details, an in-depth comparative analysis is provided in the next section. The figure illustrates the synthesis of a ring resonator

with a cavity length of 6 BULs and an unbalanced MZI with arm lengths of 3 and 6 BULs respectively. In the latter an internal crossing is implemented.

Finally, the hexagonal topology proposed in [18], [20] yields a more efficient 3-point interconnection scheme that resembles the multiport interferometer configurations described in section 3, with the difference that the proposed pattern also allows the synthesis of optical feedback loops and optical cavities. As illustrated in Figure 16, the light flow propagates through TBUs with longitudinal axis orientation of ±60º and 0º. However, in contrast to triangular waveguide meshes, the angle described by the longitudinal axis of two connected TBU is always 120º.

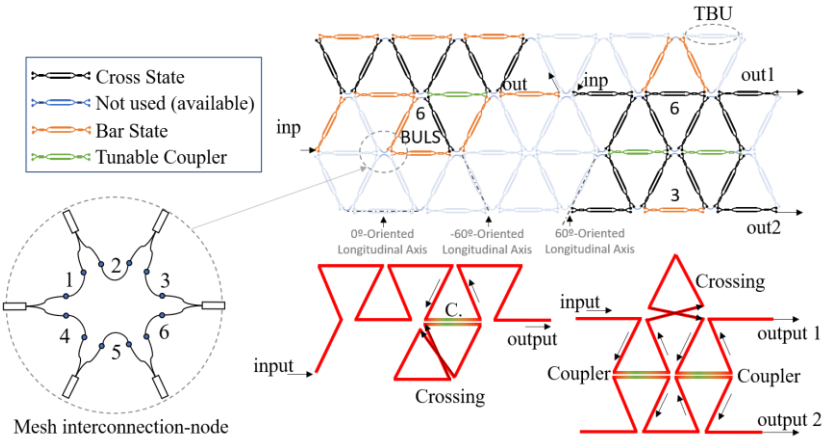

Fig. 15. Basic programming of medium-complex circuits in triangular waveguide mesh topology: delay line, unbalanced MZI and optical ring resonator (After [18]).

In the figure, we have represented an example of a 12-BUL optical cavity, an unbalanced MZI of arm lengths 1 and 5 BUL as well as a discrete delay line of 9 BULs. The main advantages are their versatility and flexibility in fitting conventional circuit programming, their enhanced resolution compared to the two previous topologies and their synthesis efficiency. One of the main drawbacks of waveguide meshes, that is exacerbated in the hexagonal topology, is that the overall mesh footprint can be compromised if the longitudinal TBU dimension is too large.

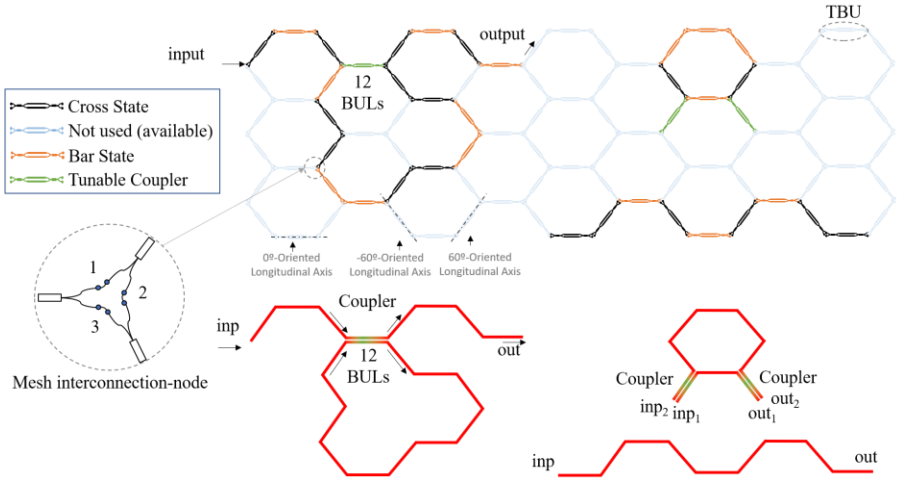

Fig. 16. Basic programming of medium-complex circuits in hexagonal waveguide mesh topology: delay line, unbalanced MZI and optical ring resonator After [18]).

4.3 Comparative analysis of waveguide meshes

We can compare the capabilities of the three waveguide mesh designs presented in the previous subsection by benchmarking their performance against a set of figures of merit, which are relevant from a chip integration point of view.

Spatial tuning resolution step: quantifies which is the minimum step in BUL units by which the arm length mismatch or the cavity length can be increased/decreased. The smaller the value of this figure of merit, the better, as this allows a finer discrete spatial sampling and therefore a wider range of interferometric lengths.

Reconfiguration performance: quantifies the number of filters with different spectral period values $\Delta\upsilon_{FSR}$ that can be implemented with a given waveguide mesh design. $\Delta\upsilon_{FSR}$ given by:

$$\Delta\nu_{FSR} = \frac{c}{n_g \cdot N \cdot BULs}, \tag{46}$$

where n_g is the group index of the waveguide and $N = L_{ORR}$ or $N = \Delta L_{MZI}$ is the representative interferometer length (normalized to the BUL) depending on whether an optical ring resonator (ORR) or a MZI is considered. The higher this figure the better.

Number of switching elements per unit area: For equal reconfiguration performance, a mesh design having a number of switching elements per unit area as low as possible is preferred as this represents a better usage of the available footprint.

Mesh replication flexibility: defined as the number of possible different alternative geometries that a given mesh design topology provides to implement a given ORR (with a fixed cavity length) or MZI configuration (with a fixed arm length imbalance). This metric is a good indicator of the potential for configuring complex devices involving cascaded photonic circuits and also for allocating a given circuit in different locations within the available or unused footprint of a waveguide mesh.

Losses and spatial resolution associated with TBU interconnections: Interconnections between the TBUs determine the spatial resolution and the losses due to bending radii and polarization rotation. To make a fair comparison between the meshes, we consider two benchmarking alternatives. In both cases, the tunable coupler length of the TBU is kept constant: In the first one, the bending radii of the curves are fixed while in the second it is the BUL that is kept constant.

Table 1 summarizes the results of a complete comparison study reported in [18] taking into account the different figures of merit defined above and the three mesh designs. With the exception of the replication ratio of ORRs, the hexagonal mesh design is the most versatile option featuring the best results in all the figures of merit. Its superior performance in terms of spatial tuning resolution step allows for a higher reconfiguration performance, that is, a wider range of spectral periods that can be implemented with complex structures built upon combining ORR and MZI based filters. The reduced value in the number of switching elements per unit area allows simpler configurations in terms of fabrication, electrode deposition, control pad interconnections and power consumption. Finally, and equally important, the hexagonal

lattice mesh provides shorter curved sections for a given access waveguide bending radius and a fixed BUL value, which, in turn, results in lower propagation losses.

Table 1: Summary of values for the figures of merit of the different waveguide mesh designs.

Figure of Merit	Triangular	Square	Hexagonal
ORR cavity spatial tuning resolution step in BUL units (the lower the better)	3	4	**2*** **The first and second step has a resolution of 6 and 4.**
MZI arm imbalance spatial tuning resolution step in BUL units (the lower the better)	3	4	**2**
ORR reconfiguration performance (the higher the better) (for X=25 *BUL*)	8	6	**9**
MZI reconfiguration performance (for X=25 *BUL*)	8	6	**12**
Switching elements per unit area compared to *square* % (the lower the better for a fixed value of reconfiguration performance)	+65.00%	0.00%	**-36.66%**
Replication Ratio for ORR structures up to 16 BUL cavity length (the higher the better).	1.00	**2.68**	1.31
Replication Ratio for MZI structures up to 12 BUL interferometric length (the higher the better).	1.00	3.00	**3.36**
$L_{access}/L_{access\ square}$ % for a fixed Ra (the lower the better)	+33.33%	+0.00%	**-33.33%**
Ra/Ra_{square} % for a fixed BUL (the higher the better)	-25.00%	+0.00%	**+50.00%**

4.4 Photonic circuit synthesis and emulation using waveguide meshes

Integrated waveguide meshes featuring the possibility of feed-backward signal propagation are the most complete configuration for a programmable processor core, since they can implement and emulate any kind of standalone as well as combinations of serial and parallel circuits. These include, as a particular case the feedforward-only multiport interferometers reviewed in section 3. We theoretically illustrate here these capabilities by showing several examples that cover a broad range of different circuits, while in subsection 6.1 we provide several experimental demonstrations validating these implementations. The examples shown in this section are based on a hexagonal mesh, but similar arrangements can be implemented through square and triangular waveguide meshes.

Waveguide meshes can implement in a quite straightforward way classical FIR and IIR discrete time impulse response filters. For instance, in the case of FIR filters, both transversal and lattice filters have been demonstrated. Lattice filters, for example are based on Unbalanced Mach-Zehnder interferometers (UMZIs), which are 2-input/2-output periodic notch filters [66]. UMZIs find multiple applications [67], including linear phase filters, multi-channel selectors, group delay compensators and biosensors. These filtering structures are all-zero filters in the z-plane. A multi-stage filter can be realized by cascading single UMZIs structures. In order to programme the optical core to produce a one-stage FIR filter, the first step is the location and configuration of the first TBU that will operate as the input tunable coupler defined by a coupling constant K_1. Then, two synthesised waveguide paths have to be configured fulfilling two conditions: They have to maintain the desired differential path length ($\Delta L = L_{Longer} - L_{shorter}$) or a desired FSR given by (46) accomplishing at the same time, that both final TBUs coincide

at each of the input ports of the closing coupler (K_2) of the UMZI. By suitably tuning each TBU within the mesh, we can implement UMZI devices with path unbalances given by $\Delta L = 2n$ *BUL*, for n = 0, 1, 2, 3, …. By taking the minimum possible value for the length of the shorter path, we can reduce the insertion losses of the filter and the number of TBUs. Figure 17 illustrates the targeted PICs with their corresponding settings of each TBU inside the mesh to obtain three different UMZI Filters with different FSRs. Note that the numbers accounts for the MZI arm lengths in BULs.

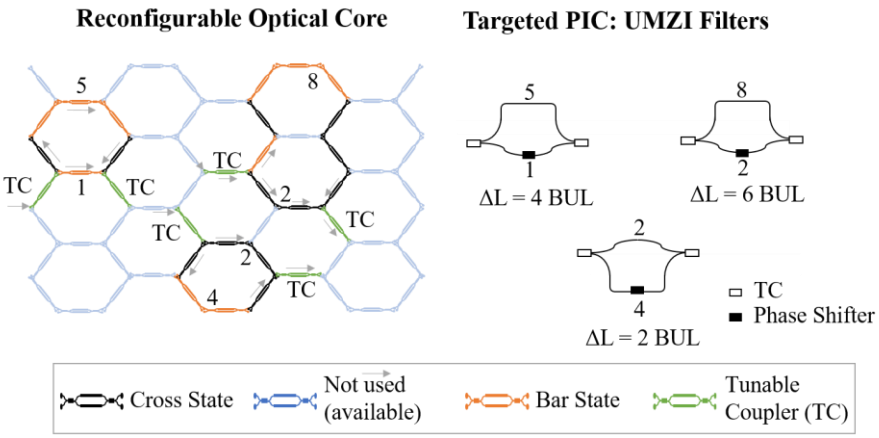

Fig. 17. FIR filter implementations (After [20]). (Left) hexagonal mesh setting for (Right) three different targeted UMZI Filters. Note the colour code that describes the programming status of each TBU in the mesh.

IIR filters are usually implemented through ring cavities, which are either 1-input/1-output or 2-input/2-output periodic filters. In the first case, they implement all-pole IIR notch filters, while in the second they can implement both IIR notch and FIR+IIR bandpass filters [66]. These are the basic building blocks for more complex filter designs such as CROWs and SCISSORs. Ring cavities find multiple applications [68] including integrators, differentiators and Hilbert transformers [69], dispersion compensators [68], as well as tunable radiofrequency phase shifters and true time delay lines, [70]. To program a single cavity filter, the first step is the location and configuration of the first TBU that will operate as the input coupler defined by a coupling constant K_1. Then a waveguide path has to be configured starting from one output port of the first TBU and ending in one of the input ports of the first TBU –providing the desired cavity length (ΔL_{ORR}) or FSR. One of the TBUs within the waveguide path can be set as a second coupler (K_2) to implement a second input/output port and therefore enable a 2-input/2-output filter. By suitably tuning each TBU within the mesh, we can implement single optical ring resonators with cavity lengths given by ΔL_{ORR} = 6, 10, 12, 14, … BULs. Different values of K_1 and K_2 set the values of the absolute magnitude of the zero and the pole [66]. Since any TBU in the waveguide implement the cavity can be operated as a constant-amplitude phase shifter from 0 to 2π, we can tune the filter resonance position along a full spectral period. Figure 18 illustrates the mesh configuration for three IIRs filters with different FSRs with cavity lengths corresponding to 6, 10 and 12 BULs, respectively. Note that, in this example, the shorter cavity has both tunable couplers activated (i.e., it is a 2-input/2-output filter).

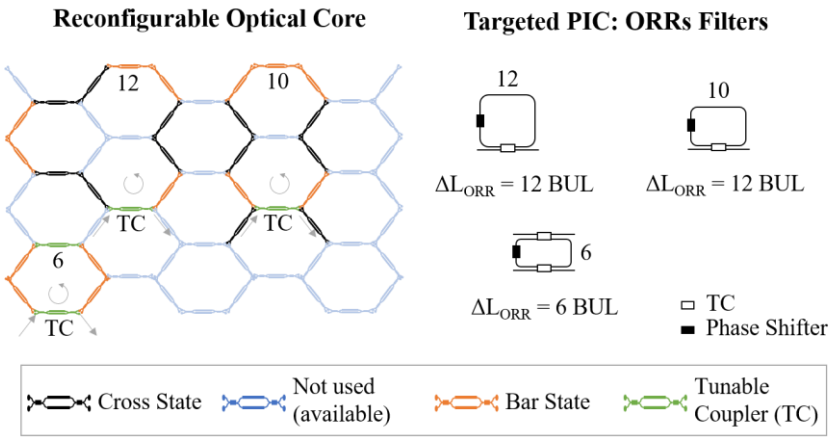

Fig. 18. Single-cavity IIR Filter implementations (After [20]). (Left) hexagonal mesh setting for (right) three different targeted ORR filters. Note the colour code that describes the programming status of each TBU in the mesh.

The former elements can be employed as building blocks to implement more complex (multicavity) signal processing structures like CROWs [71], SCISSORS [72], and ring-loaded MZIs [73]. These are usually 2-input/2-output filters that are characterized by transfer functions with a higher number of zeros and poles. By suitably tuning the coupling constants and additional phases, one can obtain, for instance, filters with special characteristics in the modulus or the phase response [68].

Beyond pure filtering structures based on FIR and IIR structures, waveguide meshes can also implement programmable delay lines and multiport interferometers. For instance, as it has been shown in figures 13-15 waveguide meshes can be employed for the implementation of delay lines with delays equal to N basic unit delays, where N is the number of TBUs that defines each configured light-path. More complex circuits featuring arrays of discrete true time optical delay lines with a sequential delay increment between output/input ports $\Delta\tau$ can also be emulated for beamforming networks. True time delay line operation can be programmed in waveguide meshes by configuring some of the TBUs as tunable couplers and some as optical crossbar switches, creating adjacent light-paths with an incremental length value ΔL (expressed in discrete values of BULs). This incremental length defines, in turn, the delay that characterized the path associated to each output port. Fig. 19 illustrates, as an example, the implementation of a 1x8 beamforming network based on a hexagonal waveguide mesh in a PIC layout.

By suitable configuring each TBUs using the defined color-code for crossbar and tunable coupling operation we illustrate the delay-array operation for different differential delays. In particular, for path length differences of 0, 2, 4, 6, 8, 10, 12, and 14 BULs. For each delay configuration, we have specified at each output port, the corresponding number of TBU that define the delay. Since larger delays suffer from greater losses. These can be compensated by tailoring the coupling constants of the TBUs configured as tunable couplers. A complete algorithm for loss compensation can be found in [22]. For instance, Figure 20 (a) shows an example of a 4 x 4 interferometer implemented by means of a triangular arrangement of beamsplitters, while Figure 20 (b) shows the equivalent structure implemented on a hexagonal waveguide mesh. Each beamsplitter can set a certain splitting ratio and a relative phase to the upper output. Reck et al. [21] and Miller [12] have developed algorithms to program and configure the triangular arrangement so it can implement any desired linear unitary transformation [74].

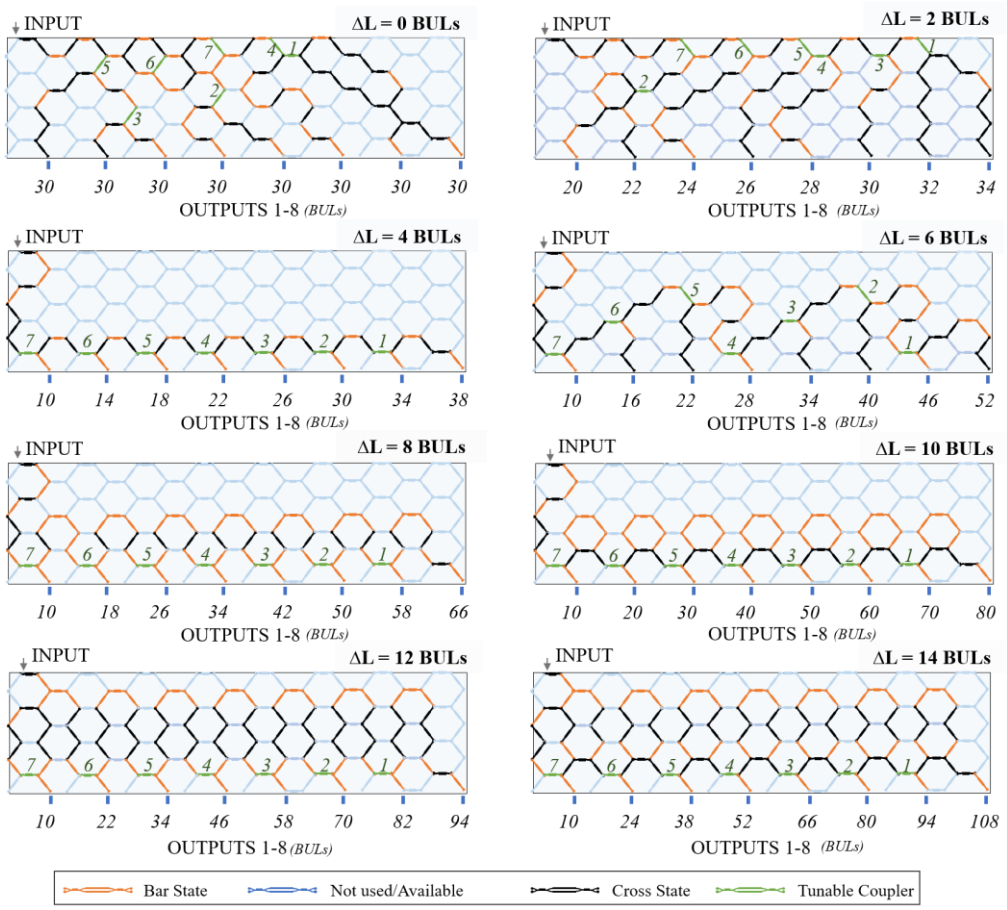

Fig. 19. 1X8 Delay-line array based on discrete optical delay lines (After [65]): Configuration examples for 0-, 2-, 4-, 6-, 8-, 10-, 12-, and 14-BUL path difference. Each path length is labelled at each output. The color-coded used for each TBU configuration is: Cross State (black), Bar State (Orange), Tunable Coupler (Green).

To adapt, for example, the synthesis algorithm developed by Miller to the hexagonal waveguide mesh we, first of all, need to consider the possible different phase contributions due to the different access paths established between the interferometer inputs and the internal processing elements forming the triangular arrangement of beam splitters and, from these, to the different outputs.

These different phase contributions must be compensated. Then, we need to establish an equivalent configuration, -using the available primitive elements in the hexagonal waveguide mesh-, to the MZI with a phase shifter in the upper output port employed by Miller and shown in Figure 20(c). In this case, as illustrated in Figure 20 (d), the equivalent "beamsplitter" is implemented using a TBU for the tunable coupler (with a transfer matrix defined by h_{TC} as in Eq. (25)), followed by two TBUs, which are biased in cross state and employed as output connections. In the latter, the upper TBU also implements a phase shifter and is defined by the transfer matrix h_{UPS}. The lower TBU is defined by the transfer matrix h_{LPS}.

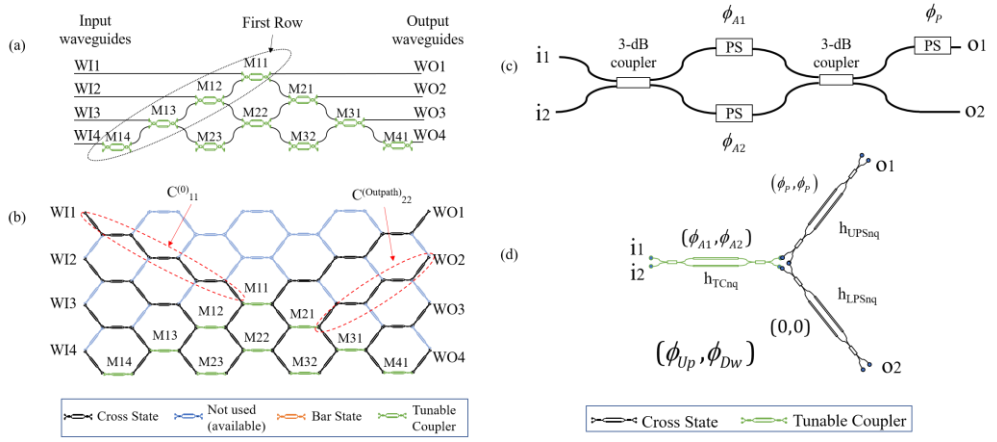

Fig. 20. Universal interferometers emulated using an hexagonal waveguide mesh (After [23]) : (a) Classical triangular arrangement and (b) hexagonal mesh-based implementation of a 4 x4 interferometer. (c) Beamsplitter for the classical approach and (d) corresponding beamsplitter implementation with 3 TBUs for the hexagonal waveguide Mesh.

5. Field Programmable Photonic Gate Arrays

5.1 The FPPGA concept

Throughout the paper we have stressed the objective that lies behind programmable integrated photonics, which is no other than seeking the design of common integrated optical hardware configurations able to implement a wide variety of functionalities by suitable programming. Waveguide meshes described in section 4 offer versatile hardware solutions for the implementation of programmable circuits. Standalone however they do not provide a complete architectural solution of a photonics device that could be programmed for the implementation of arbitrary simple, complex or even simultaneous circuits. PIP needs more than just a programmable integrated waveguide mesh.

In electronics, this concept is sustained by FPGAs and by Field Programmable Analog Arrays (FPAAs) [1], [3], [55], [75]-[77] and following a similar rationale behind the principles of these devices one could consider the implementation of a similar concept that can be realized by combining a set of Programmable Photonics Analog Blocks and a set of Reconfigurable Photonic Interconnects implemented over a photonic chip. This element, which we call FPPGA [78], can be able of implementing one or various simultaneous photonics circuits and/or linear multiport transformations by the appropriate programming of its main resources, which are the optical core and the high-performance building blocks and the selection of its input and output ports.

5.2 Programmable Photonic Analog Blocks and interconnections

The high-level concept of the FPPGA core is schematically shown in Figure 21 [78]. It consists of a set of programmable photonic analog blocks and reconfigurable photonic interconnects implemented through an array of photonic waveguide elements grown on a photonic chip substrate. The waveguide elements that compose the Reconfigurable Photonic Interconnects have programmable features as well and can propagate light in both directions. The layout in Figure 21 does not presuppose any particular waveguide array geometry and that the square layout depicted there is just for illustration purposes.

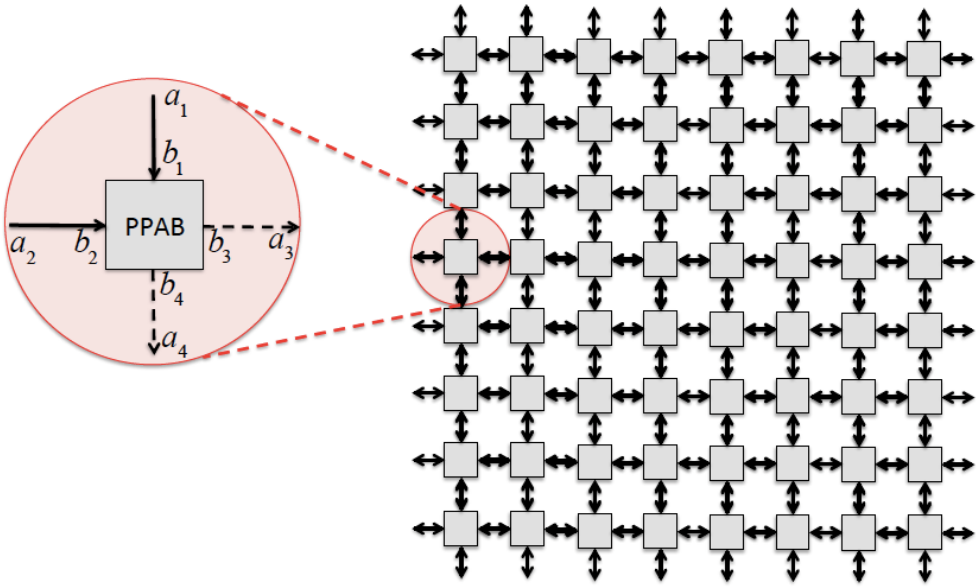

Fig. 21. Schematic diagram example of the proposed FPPGA device. The zoom shows a detail of the Programmable Photonic Analog Block (PPAB)as it pertains to the left-up to right-bottom direction of propagation. (After [78]).

Both programmable photonics analog blocks and reconfigurable photonic interconnects in FPPGAs are implemented by means of 2x2 reversible programmable unitary transformations. These, as shown by (34) in section 2.4, can be built using a concatenation of three rotation matrices, however, a reduced version of that construction, (i.e., the actual gates) can be employed [79]:

$$G = e^{j\delta} R_y(\beta) R_z(\gamma), \qquad G = e^{j\delta} R_x(\beta) R_z(\gamma). \tag{47}$$

Here, one of the phase shifter units is not included (in this case the one succeeding the tunable coupler in Figure 8). Programmable arrays can then be constructed by means of two-dimensional assemblies of 2x2 gates given by (47). This is shown in Figure 22(a). Note that as shown in Figure 22(b) since for every 2x2 *G* unit its input phase shifter (shown in blue) can be programmed to incorporate the effect of the required preceding phase shift as well as the fictitious succeeding phase shifter of the preceding 2x2 G unit then this configuration is actually equivalent to that of an array of arbitrary 2x2 unitary transformers. This structure can then be programmed to implement any arbitrary *NxN* unitary transformation as it has been shown in section 2. Furthermore, because of the reversible nature of the gates, both feedforward and feedbackward operations are possible, even simultaneously. This enables the possibility of implementing resonant and cavity structures with this field programmable reversible gate array configuration.

A question of practical interest is how the 2D structure shown in Figure 22(a) can be implemented by means of waveguide meshes. Figure 23 depicts several options that can be contemplated for the implementation of 2D arrangements of gates.

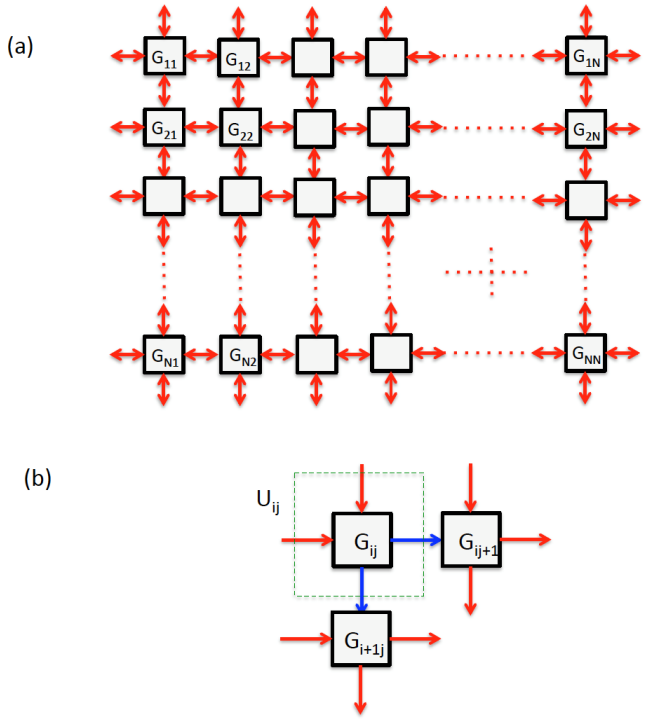

Fig. 22. a) Two-dimensional array arrangement of reversible *G* gates. (b) Detailed explanation of how the concatenation of a given Gate G_{ij} actually results in the possibility of implementing a unitary arbitrary transformation by the *ij* element. (Adapted from [79]).

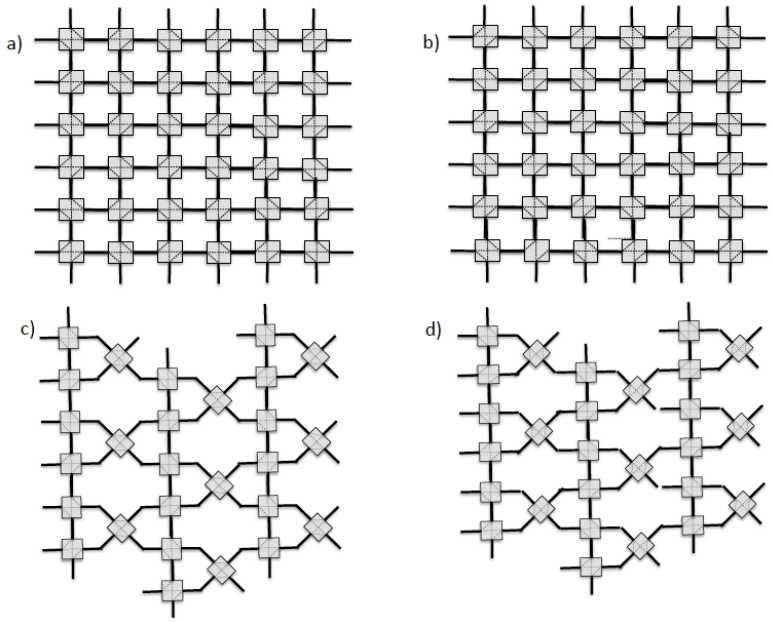

Fig. 23. Physical layouts for the implementation of the 2D gate array in Figure 21 (After [78]). Each square box represents a 2x2 tunable coupling element and a (preceding) phase shifter. The internal broken-dotted lines illustrate the possible physical connections between input and output ports. (a) and (b) show structures where the gates in adjacent columns are rotated by 180º. (c) and (d) show structures where the gates in adjacent columns are rotated by 90º.

The above 2D physical structures lead to immediate implementation by means of square, triangular and hexagonal waveguide meshes by means of the isomorphic relationship between the fundamental building blocks illustrated in Figure 24.

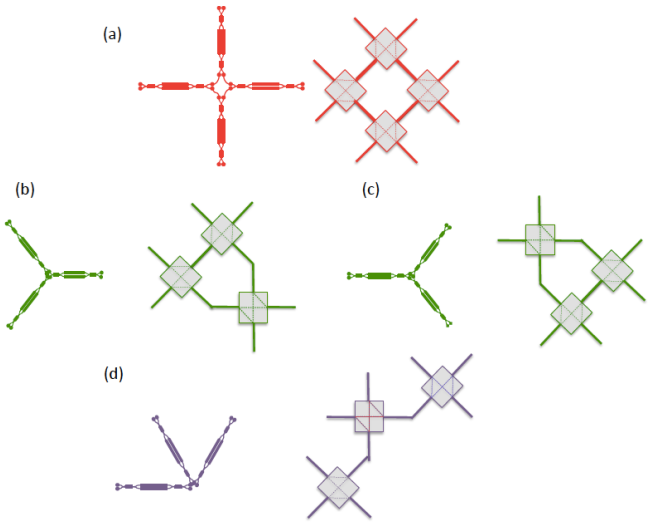

Fig. 24. Identification between the fundamental unit blocks employed to construct integrated waveguide meshes and the main physical layouts for 2D gate arrays shown in Fig. 23 (After [78]).

5.3 High-Level FPPGA concepts: Design Flow and Technology Mapping

The most general type of full FPPGA device consists of an array of uncommitted elements that can be interconnected according to a user's specifications and configured for a wide variety of applications. An FPPGA combines the programmability of the most basic reconfigurable photonic integrated circuits in a scalable interconnection structure, allowing programmable circuits with much higher processing density. Thus, processing complexity comes from the interconnectivity.

The left part of Figure 25 shows the main steps of the design flow process, which we now describe. The starting point for the design flow is the initial application entry or circuit configuration to be implemented. The specifications are then processed to optimize the area and performance of the final circuit. Then, specifications are transformed into a compatible circuit of FPPGA processing blocks (technology mapping), optimizing attributes such as delay, performance, accumulated loss or number of blocks.

The technology mapping phase transforms the optimized network into a circuit that consists of a restricted set of circuit elements (FPPGA processing blocks). This is done selecting a set from the available programmable photonics analog blocks and specifying how these will be interconnected. This interconnection step implies the setting of several reconfigurable photonic interconnects elements physically connecting the selected programmable photonics analog blocks. This determines the total number of processing blocks to be activated by programming. In a second stage, the processing block configurations (i.e., types of programmable photonics analog blocks and reconfigurable photonic interconnects) are chosen and performance calculation and design verification are carried out. This can be done either physically by feeding all the necessary configuration data to the programming units to configure the final chip or, more commonly, by iteratively employing accurate models of the FPPGA in the software plane.

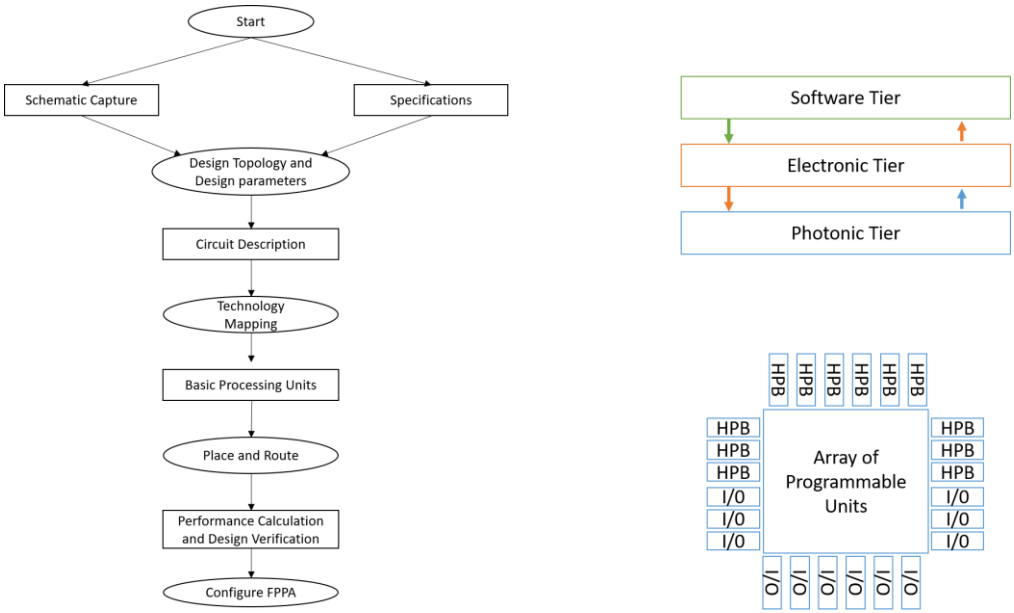

Fig. 25. Left: main steps involved in the design Flow of a FPPGA device (After [78]). Right: FPPGA soft and hard tiers and expanded layout including peripheral high-performance blocks.

The next step assigns each processing block to a specific location in the FPPGA core including, as well, the choice of the processing units that route the input signals to the core to the input/s of the programmed circuit and the output/s of the programmed circuit to the core outputs. Note that in contrast to FPGAs [55], [75], the proposed structure does not physically differentiate between processing blocks and interconnection resources.

From the aforementioned description, it can be appreciated that the FPPGA device involves considering not only the physical hardware of the photonic and control electronic tier, but also a software layer (see upper right part of Figure 25). For the control electronics, the scheme reviewed in section 6 applies. For dynamic operation, the steps contained in the generic design flow can be done automatically either by the software layer, the user, or by a mixture of both, depending on the autonomy and the capabilities of the FPPGA. In addition, a failure in any of the steps will require an iterative process till the specifications are accomplished successfully. Additional parallel optimization process (mainly self-winding), enable robust operation, self-healing attributes and additional processing power to the physical device.

In a similar way to modern FPGA families, FPPGA can include peripheral HPBs to expand its capabilities to include higher-level functionality fixed into the chip. This is shown schematically in the lower right part of Figure 25. Having these common functions embedded into the chip reduces the area required and gives those functions increased performance compared to building them from primitives. Moreover, some of them are impossible to be obtained by a discretized version of basic processing blocks. Examples of these include high-dispersive elements, generic modulation and photo detection subsystems, optical amplifiers and source subsystems and high-performance filtering structures to cite a few.

6. Programming and practical considerations

6.1 Experimental implementation of multiport interferometers and waveguide mesh circuits

The implementation of a multi-port interferometer or a feedforward/feedbackward waveguide mesh circuit requires the integration and independent driving of a great number of primitive processing elements or tunable basic units. The ideal behaviour of the TBU leads to the perfect

performance of the programmable PIC. However, in practice, several factors of degradation must be considered: imperfect splitting ratios, phase control, parasitic back-reflections, loss imbalances, fabrication errors (gradients through the circuit in thickness or temperature) and drifts in time. These constraints, combined with the high cost and large delays in PIC development, challenge the evolution of programmable photonics. Moreover, to achieve a practical use of programmable PICs, these systems demand non-trivial assistance from control electronics, the development of a software layer and packaging for the electrical and optical interface.

As expected, the first experimental demonstrations of programmable photonic circuits based on the replication of TBUs are to be considered as proof-of-concept examples. However, they are complex enough to highlight their potentiality and help to envision the main scalability issues experienced when more primitive elements are required.

Regarding feedforward multiport-interferometers, their first integration was mainly driven by quantum information processing community [13], [15], [61], and was later considered for other applications like mode-processing [25], [26], hardware acceleration for neural networks [24], [80], routing and general-purpose multi-port linear photonic processing [63], [81]. The number of TBUs integrated ranges between 6 to 88. The circuit application has influenced the choice of the integration platform. Silica was initially employed as a solution to exploit its low fibre-chip coupling loss demanded by required low-loss of quantum circuitry. However, the highest density demonstrations have employed silicon photonics technology. Table 2 summarizes the experimental demonstrations to date.

Regarding multipurpose mesh arrangements providing feedforward and feedbackward propagation of light, the first demonstrations have dealt with similar challenges to the described for multipurpose interferometers. In 2015, Zhuang and co-workers pioneered the field with the experimental demonstration of a square waveguide mesh topology illustrated in Figure 12 (a), [17]. The structure, fabricated in a silicon nitride platform, comprised two square cells, 5 TBUs and 9 phase shifters was fully programmable and was employed to demonstrate simple FIR and IIR impulse response filters with single and/or double input/output ports of synthetized ORRs.

Table 2: Experimental demonstrators of feed-forward meshes/ multiport interferometers

Year	Authors	TBU	PS	OP	dB /TBU	TE	Foundry	P (mW) / π	RT (us)	Topology	Size (mmxmm)	PS density ($1/mm^2$)	CL/facet (dB)	Chip-couplers
2016	Carollan et al. [13]	15	30	12	TBD	TO	Silica on silicon	400	TBD	Triangular	100x40	0.007	0.5	E
2016	Ribeiro et al. [25]	9	18	8	1	TO	Silicon	15	250	Triangular	1x3	6.000	TBD	V
2017	Anoni et al. [26]	6	12	8	1	TO	Silicon	10	10	Triangular	3.7 x 1.4	2.320	TBD	V
2017	Harris et al. [15,24]	88	176	52	TBD	TO	Silicon	10	8	Trapezoid	2.1 x 4.3	19.050	3.5	E
2018	Mennea et al. [63]	30	120	40	4.20	TO	Silica on silicon	10 V	TBD	Rectangular	3.05x1.9 (x3)	20.710	0.8	E
2018	Caterina et al. [61]	64	128	16	0.27	TO	Silicon nitride	3.35 V	TBD	Triangular (double)	16x16 TBD	0.500	2.9	E
2019	Zhou et al. [80]	20	48	8	TBD	TO	Silicon	27	TBD	Triangular SVD	1.3 x 7.5	4.920	3.5	V
2019	Zheng et al. [81]	10	18	10	0.63	TO	Silicon nitride	330	>1000	Rectangular	11x3	0.550	3.5	E

TBU: Number of TBU, PS: Number of phase shifters, OP: Number of optical ports, P: Power Consumption, RT: Response Time, CL: Fiber-chip coupling losses, E: edge-coupling, V: vertical-coupling

With a basic unit length (and basic unit delay of 3450 μm and 19.7 ps, respectively, Zhuang et al. demonstrated bandpass filters with a tunable centre frequency that spans two octaves (1.6–6 GHz) and a reconfigurable band shape (including flat-top resonance with up to passband–stopband 25 dB extinction). They also demonstrated notch filters with up to 55 dB rejection

ratio, Hilbert transformers and tunable delay lines as shown in Figure 26. The number of accessible optical ports was 4.

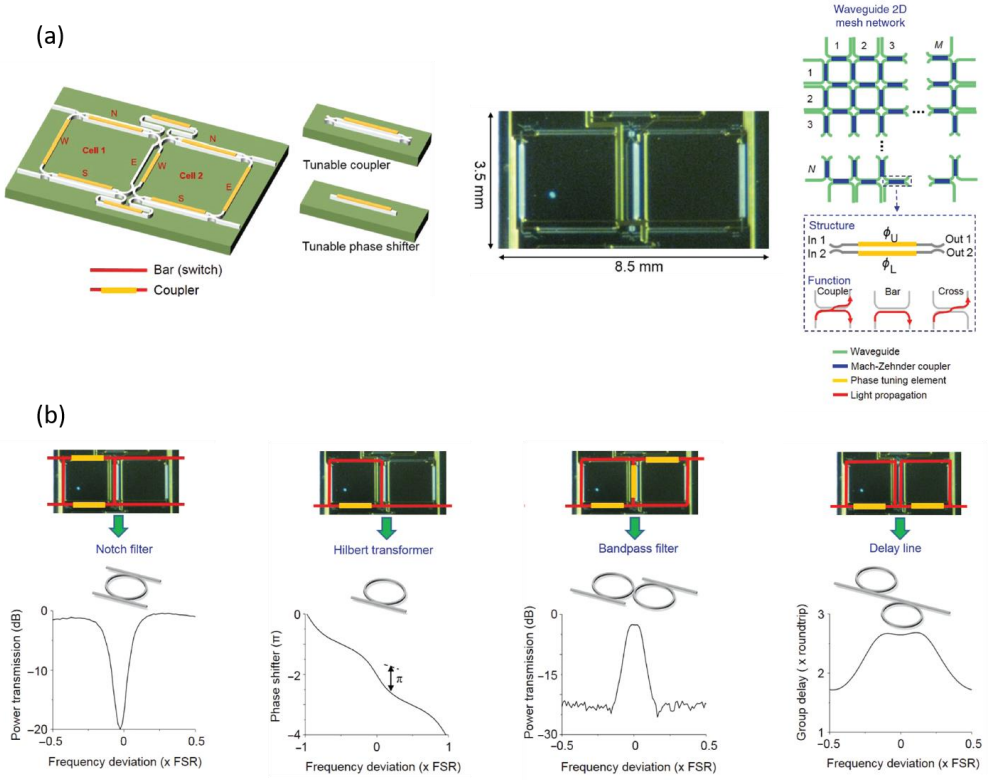

Fig. 26. (a) Schematic and photo of the Si_3N_4 waveguide technology (TriPleX) chip implementing a 2 square cell waveguide mesh reported in [17]. (b) Experimental results for different programmed circuit configurations obtained by varying phase-tuning elements in the chip and the measurements of their corresponding frequency responses. Reproduced from [17].

In 2017, Pérez et al., reported the results of the first hexagonal waveguide mesh composed of 7 cells (30 TBUs, 60 thermally- tuned phase actuators) fabricated in Silicon on Insulator, [20]. The chip photograph is shown in Figure 12 (b). The device was fabricated at the Nanofabrication Centre at the University of Southampton. Silicon on insulator wafers with a 220-nm thick silicon overlayer and a 3-µm thick buried oxide layer were used (for more details on fabrication and testing see [20], [64]). Figure 27 illustrates a single cavity optical ring resonator with a cavity length given by 6 BULs. The figure shows in (a) the waveguide mesh configurations (with the TBU device status according to the colour code previously described), (b) the circuit layout and (c) the modulus response for the OUT_1 port. The measured results correspond to different values of K_1 and K_2, which settle the positions of the zero and the pole. The IIR filter tunability, which is shown in Figure 27 (d), is achieved by exploiting the fact that the coupling constant and the phase shift in any TBU of the mesh can be adjusted independently. Hence, any TBU inside the cavity can be operated as a constant-amplitude phase shifter. Finally, Figure 27 (e) shows the time response of the ring resonator when the critical coupling is achieved.

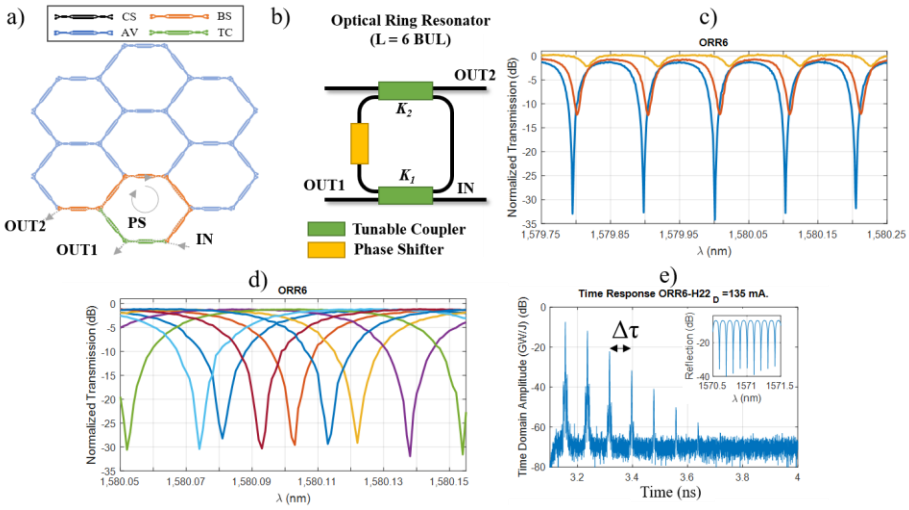

Fig. 27. Experimental results for 6-BUL ring resonator IIR and FIR+IIR filters (After [20]). (a) Waveguide mesh connection diagram, (b) circuit layout and (c) measured modulus transfer function for a IIR filter for different values of the coupling constants K_1 and K_2, (d) IIR filter along a full spectral period for different values of the optical ring resonator round-trip phase shift, (e) time response for critical coupling condition.

More recently, the triangular arrangement was demonstrated in a silicon nitride platform. The proof-of-concept involves the integration of 5 TBU describing two cells. In this case, the TBU employs a dual-drive directional coupler, for the first time. In this paper, as summarized in Fig. 28, few ring resonator configurations are configured, [66].

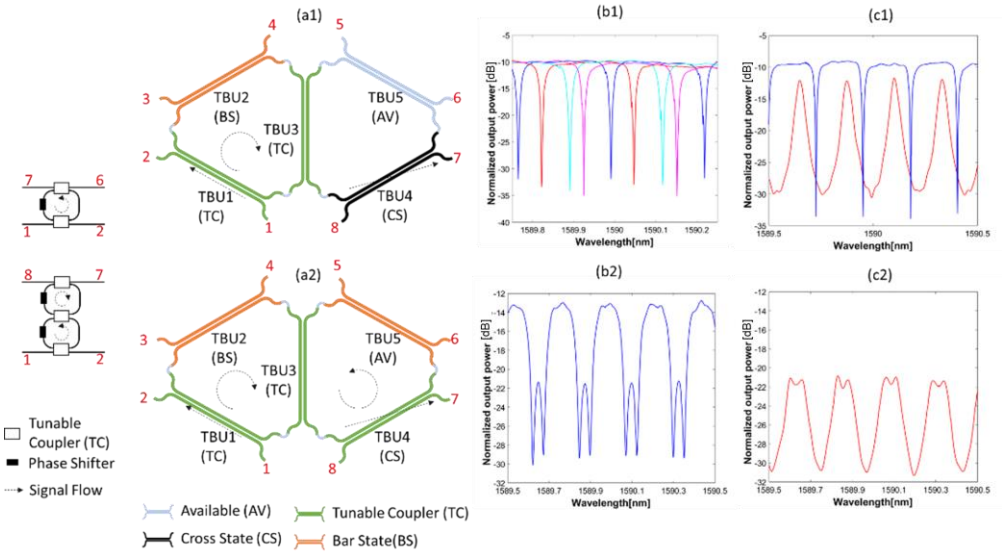

Fig. 28. Triangular feedforward/feed-backward waveguide mesh arrangement based on dual-drive directional couplers. (a) Targeted layout and TBU settings, (b) reflection response of optical circuits, (c) transmission response of optical circuits. First row: single ring resonator and add-drop. Second row: Coupled Ring Resonator Structure, (Reproduced from [66]).

We can summarize the main figures of the aforementioned experimental demonstrations in Table 3.

Table 3: Summary of the main figures of the multipurpose waveguide meshes.

Year	Authors	TBU	PS	OP	dB/TBU	BUL (um)*[1]	BUD (ps)*[2]	TE	P (mW) /pi	RT (us)	Topology	TBU	Size (mmxmm)	TBU density (1/mm^2)	C (CL)
2015	Zhuang et al., [16]	7	14	4	TBD	3450	19.7	TO	300	TBD	Square	MZI	3.5x8.5	0.235	E(TBD)
2016	Pérez et al., [1, 17, 18, 19]	30	60	24	0.59	975	13.5	TO	110	TBD	Hexagonal	MZI	15x15	0.133	V (6.5)
2017	Pérez et al., [20]	40	80	30	TBD	1315	8.4	TO	200	TBD	Hexagonal	MZI	11x5.5	0.661	E (3.5)
2018	Pérez et al., [21]	5	10	8	<0.14	1178	TBD	TO	300	TBD	Triangular	Dual-drive directional coupler	7x2.5	0.285	E (3.5)

TBU: Number of TBU, PS: Number of phase shifters, OP: Number of optical ports, BUL: Basic Unit Length, BUD: Basic Unit Delay, TE: Tuning effect, TO: Thermo-optic, P: Power Consumption, RT: Response Time, C (CL): Fiber-chip coupling method (losses in dB), E: edge-coupling, V: vertical-coupling

6.2 Design and analysis of large-scale programmable photonic circuits

A mesh performance analysis is incomplete without the involvement of the TBU design. In this section, we will look into such design challenges especially from the perspective of large-scale integration and we will start by considering the TBU to be a black box defined by parameters such as insertion loss, footprint, power consumption and uniformity as illustrated.

6.2.1. Number of TBUs

In both feed-forward-only and multiport-interferometers based on waveguide meshes, the number of accessible optical ports and hence the number of TBUs limit the size of the largest matrix of linear operation that can be emulated. Hence, a greater number of TBUs lead to greater versatility of the circuit which is shown in Table 4 as the required TBUs and phase shifters for a set of given maximum matrix sizes (N x N) for either Reck [21] or Clements [22] design. The TBUs and phase shifters required scale exponentially reaching numbers which are then way beyond the state-of-the-art.

The same idea holds true for multipurpose waveguide arrangements where larger number of TBUs lead to more versatility in their performance. Table 4 illustrates the number of TBUs and phase shifters required for a given cell size using a hexagonal mesh layout. The TBU number can vary depending on the exact design implemented but an approximation of 3.6 Nc + 4.54, where N_c is the number of cells can be extracted from the trend.

Although the numbers extracted from Table 4, for both the architectures are different, this can be used as a useful indicator of what is needed for future scalability. Such requirements need to be kept in mind while discussing such circuits no matter the architecture in order to invoke thought on how to tackle and overcome the issues arising from it, [20], [64].

Table 4. Required minimal number of TBU and Phase actuators for waveguide meshes. *N*: is the number of input modes for feed-forward interferometers and the number of hexagonal cells, respectively.

	*N*x*N* feed-forward interferometer		Hexagonal waveguide mesh	
N	Number of TBUs $N(N-1)/2$	Phase shifters $2N(N-1)/2$	Number of TBUs	Phase shifters
4	6	12	19	38
8	28	56	34	68
16	120	240	62	124
32	496	992	140	280
64	2016	4032	234	468
128	8128	16256	465	930
256	32640	65280	926	1852

6.2.2 Accumulated loss

Performance of such mesh circuits is also characterized by the overall losses which also have a dependency on the application and its specifications. Similar to a conventional circuit, the propagation losses and excess losses play a part in this but the difference is that in waveguide meshes, the cascaded interconnection leading to the creation of optical routes adds an additional factor which is the accumulation of losses encountered while traversing multiple TBUs. For example, in a *N*x*N* transformations, it corresponds to *N* and 2*N*-3 for the rectangular and the triangular approaches, respectively [22].

In order to estimate the maximum number of TBUs that can be traversed, we use three different overall mesh targeted loss of 5, 10 and 15 dB, respectively. Table 5 was computed on this basis where it can be seen that for a TBU of IL_{TBU} 0.2 dB and a maximum of 10-dB loss in the overall mesh, the longest light path is constrained to 50 TBUs leading to a 50x50 matrix with 1225 TBUs in a rectangular arrangement. Furthermore, chip-to-fiber coupling loss as well as loss of waveguides leading up to the mesh will increase the overall loss of any such circuit, immaterial of its layout. All in all, Table 5 reveals that for a system limited by loss, the maximum number of TBUs in the largest programmed light path will potentially range between 50 and 25 TBUs for state-of-the-art IL_{TBU}.

Table 5. Maximum number of TBUs defining a synthetized path for a mean insertion loss per TBU and maximum mesh loss.

	Max. mesh loss = 5 dB	Max. mesh loss = 10 dB	Max. mesh loss = 15 dB
IL_{TBU} = 0.05 dB	100	200	300
IL_{TBU} = 0.10 dB	50	100	150
IL_{TBU} = 0.20 dB	25	50	75
IL_{TBU} = 0.30 dB	16	33	50
IL_{TBU} = 0.40 dB	12	25	37
IL_{TBU} = 0.50 dB	10	20	30

6.2.3 Footprint

The footprint is related to the space constraints and thus limits the number of TBUs that can be integrated on chip. In most cases, the design area, defined by the size of the reticule, needs to incorporate all the components and its sub-parts like the waveguide, the actuators and the metal routing. To date, the largest circuit implementation is in the form of a matrix switch with than 450 structures similar to a TBU in a single die in a Silicon on Insulator platform, [82]

The reticle area used in most of the fabrication facilities is 400 mm^2. Assuming a compact TBU of longitudinal dimension of 300 µm, even the compact version given by the rectangular arrangement would approximately allow a maximum transformation of N equal to 64. Designs implementing components placed parallel to each other can be used to increase these numbers significantly.

6.2.4 Power consumption

The next scalability issue is associated with the power consumption of the overall circuit. The tuning efficiency of each TBU is defined by the amount of power required to produce a 180º-phase shift of the light (P_π). The intermediate coupling state requires less power, so the same power is not constantly applied to every actuator. Additionally, the setting of an independent phase shift with full flexibility will require a power consumption associated to tuning a phase between 0 and 360º and the total power consumption in its entirety depends on the numbers of active TBUs at a certain time. As an example, in Figure 29, we consider waveguide meshes of 50, 100 and 150 active TBUs in single-drive mode. We considered different tuning mechanisms, starting with 30mW for thermo-optics in SOI platforms, [83]. Optimized designs like under-etching allows figures lower than 1 mW, [84]. Since the power consumption depends on the configuration of each TBU, (not all of them will consume P_π), we have highlighted a range between 40 and 80% of the TBU consumption.

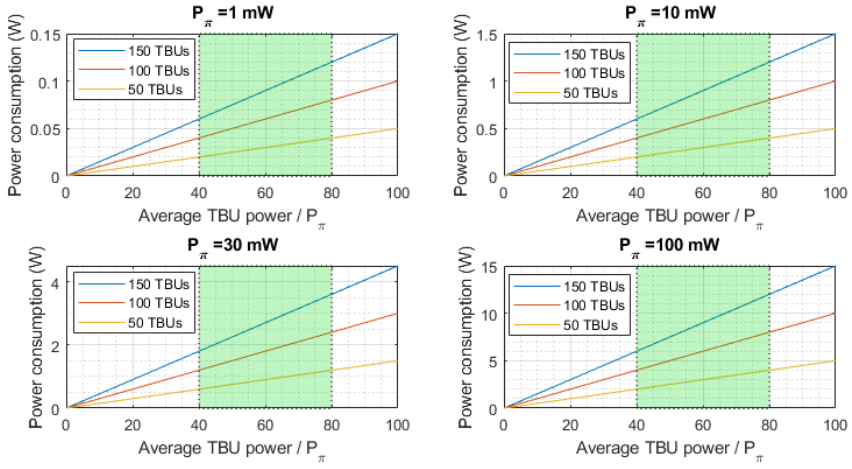

Fig. 29. Overall power consumption for waveguide meshes of 50, 100 and 150 activated TBUs for four different TBU power consumption (Reproduced from [18]).

Large values of power consumption also impose additional electronic interfacing challenges and call for the availability of high-performance multichannel electronic integrated drivers. Low power consumption or non-volatile phase shifting mechanism would avoid this scalability

limitation. For this purpose, both tunable and phase-change materials as well as phase shifters based on Micro Electro Mechanical (MEM) elements are receiving attention from the scientific community, [85]-[87].

6.2.5. Routing and metal layer design

We have already discussed that increasing the integration density will be a necessary step in the evolution of programmable photonic integrated circuits. Considering beyond state-of-the-art silicon-on-insulator TBUs with a footprint of 200 x 100 μm^2, one might think that it is possible to integrate up to 50 TBUs per mm^2, 20000 TBUs (40000 phase actuators) in a 20x20 mm^2 chip. Nevertheless, the routing of the electrical signals in the chip consumes space and hinders the design process. This is commonly done in electronic chips integration using multi-layer routing plus an actuator level, as available in most of the foundries, [88].

Interfacing the chip electrically is another major concern and design challenge. If a wire bonding is employed, all the electrical paths need to be routed to the external perimeter of the die, and to electrical pads at the top layer, need to be wire-bonded, preferably to a printed circuit board, [89]. If we consider two rows of electrical pad per side of the die with 80x80 μm^2 as dimensions, and a pitch of 50 µm, and considering the four sides of the die, this results in an approximate maximum number of pads of 1230. The number of directional coupler PADs is even reduced if we consider that one of the die sides will be employed to make room for the optical interface (a fiber array). On the other hand, if we consider a flip-chip approach with a minimum pitch of 200 µm, we can approximate the number of pads to be around 10000.

In order to reduce the number of pads required per actuator, we can employ the same solutions as the ones adopted in electronics and in optical switching matrices. In principle, two pads are required for signal a ground (or larger and lower voltage points). A first solution is based on using common grounds which might produce the drawback of electrical crosstalk due to the possible resistance variation between paths and actuators. In principle, this can be corrected through pre-processing by fully characterizing all shared resistances and calculating the voltage differences that compensate the resistance variations, [13]. Other solutions rely on sharing more pads in a matrix interconnection [90]-[92].

6.4.6. TBU optimization

During the design process of programmable waveguide meshes, the design of the TBU is also of importance especially in relation to the Basic Unit Length which is an essential attribute of the TBU. Partially coupled to the footprint concept, it accounts for the tunable coupler length and the access waveguides. In feed-forward-only arrangements, the TBU miniaturization helps to increase the integration density and in addition, in general-purpose arrangements waveguide meshes, the final BUL will limit the Free Spectral Range (FSR) of the interferometric structures and set the delay lines to a specific set of discrete values given by the BUL and the mesh architecture, [18], [64]. In this regard, a miniaturization trade-off appears between the BUL reduction and the accumulated delay per TBU. A reduction of the BUL implies that the signal must go through a greater number of TBUs to obtain a desired delay. If the 3-dB couplers limit the overall IL of the TBU, this miniaturization trade-off must be highly considered.

All in all, the previous features are coupled. The tuning mechanism impacts on the final BUL, the tuning crosstalk and the power consumption. The use of alternative tuning mechanisms like programmable phase-change materials [85]-[86], MEMS [93], piezoelectrics, or electromechanics [94] are promising solutions to reduce the power consumption while enabling a reduction of the distance between the two TBU arms. In order to further optimize the TBU and the overall mesh, it is essential to know the sources of non-ideal performance.

6.3 Error sources and impact on performance

The use of non-ideal components limits the scalability of the circuit. The circuit propagates and accumulates the performance failures of every component. Many sources of error and parasitic effects must be contemplated in the design of photonic integrated circuits and with more effort when dealing with large-scale programmable PICs, [95],[96].

6.3.1 Waveguide variations.

Loss in waveguides originate from three fundamental mechanisms: material absorption loss, scattering and radiation loss. Beyond conventional waveguide losses, geometry variations of the waveguides arise due to the non-uniformity in wafer thickness, and due to fabrication induced dimensional variations [94], [97], [98]. These changes, in the nanometer scale induce phase errors on the device level, severely affecting structures like directional couplers. A similar effect is found in PICs including multimode interferometers, array waveguide gratings, delay lines and, by extension, in Mach-Zehnder interferometers, and optical ring resonators. In programmable PICs, they mainly affect to the operation of 3-dB couplers and by extension to the operations carried out by interferometric structures.

6.3.2 Temperature drifts

Many properties of the materials employed in PIC design are temperature dependent. Similar to the previous point, during the design stage, the designer considers an operating temperature and employs this to compute the effective indices of the waveguide modes. The designer must take into account that a change in the PIC temperature during operation might modify the effective index of guided modes and this might lead to a non-functional behavior of the circuit. Temperature changes might be due to environmental changes or due to the presence of neighboring electronic integrated circuits dissipating heat. In addition, most of the programmable PICs exploit a micro-heater based localized thermo-optic effect for phase tuning. In this case, a careful design needs to be carried out, considering the undesired partial heating of waveguides in proximity of the one thermally actuated. This effect is known as thermal crosstalk and imposes a minimum safety distance between actuated waveguides in high-density programmable PICs.

6.3.3 Driving signal drifts in programmable PIC actuators.

During the tuning stage of programmable PICs, electrical signals are employed to drive the actuators and configure the PIC as desired. Either from voltage or current sources, these driving signals are not free from electrical noise and instability. Moreover, the precision range is limited to the resolution of each step that can be achieved. For example, an 8-bit voltage source ranging from 0 to 10 volt, will be limited to 256 bits, resulting in steps of 39.1 mV.

6.3.4 Impact of non-ideal components on the TBU performance

To fully understand these limits, we now focus our analysis in a standalone vision of the TBU and the implication of these non-ideal effects at a circuit level. For the remaining section we will consider MZI-based TBU architecture.

As in feedforward-only meshes, the non-ideal behavior of the TBUs leads to additional loss, scattering, and errors when setting the values for the phases and coupling factors. All in all, these lead to undesired and parasitic effects in both feedforward and feedforward/backward waveguide mesh arrangements. A common effect arising from this is signal leaking in the circuit leading to deterioration of the circuit performance. However, a smarter configuration of the circuits and a smart routing of these parasitic signals can enhance dramatically the final circuit performance, [96]. This optimization deals with the configuration of both used and non-used TBUs. For this to become practical, one can employ analytical models and their combination with optical power monitors at strategic points in the circuit. A similar approach

can be done in feedforward meshes, where tunable couplers are employed to define the 3-dB couplers of the TBU at the cost of increasing the overall chip complexity.
In both waveguide mesh arrangement approaches, a remarkable electronic circuitry and software framework is required to enable the configuration of the circuits as well as to fully exploit the benefits and advantages of programmable PICs. Both, control electronics and software are a fundamental part of the system and will be introduced in the next section.

6.4 Programming strategies, monitoring and control issues

In programmable photonics, the software framework calls for the aggregation of a wide variety of algorithms, methods or routines that are run by the electronic processing unit. They are mainly employed for setting certain functionality in the PIC and to perform necessary backplane optimisations.

We can classify these routines by their final goal or by their requirements. A set of basic routines deal with the calibration and pre-characterization of the photonic integrated circuit. For example, it is possible to run iterative routines to calibrate the electro-optical response of every phase shifter in the circuit without the need of incorporating optoelectronic monitors inside the waveguide mesh arrangement. These routines can also extract the power consumption of each unit, the accumulated loss and alert and memorize the defects in the circuit. The information gathered by these routines can be employed by a set of algorithms that optimize the circuit functionality and the resources, as the auto-routing algorithm.

6.4.1 Auto-routing algorithm in waveguide mesh arrangements

Most of the circuits programmed in waveguide meshes rely on the configuration of optical interconnections and delay lines. Moreover, as shown in Section 5, the FPPGA potentially allow the interconnection of its core with advanced components.

In short, the future evolution of large-scale programmable PICs demands the maturity of key enabling technologies such as low loss, low-power consumption and low-footprint unit cells, dense electrical interfacing for low-speed signals, and high-speed electronics co-integration. In parallel, the software layer capabilities will grow to mitigate the necessity for perfect components and enable resilient and fault-tolerant circuits. In both cases, the configuration of optical connections and optical delay lines requires the selection and configuration of the programmable unit cells in the arrangement that will define the path followed by the optical signal. For a given specification, (for example, a delay of 10 ns between two specific optical ports), there will be multiple solutions. In such a scenario, the implementation of a software routine capable of finding the drive power and automatically control the optimum path in term of loss, power consumption and other non-ideal effects is highly desired. After the translation of waveguide meshes to a graph mapping the nodes and the internal connections of the TBU, it is possible to apply graph theory and modified pathfinding algorithms to enable the search of the optimal circuit configuration [99], [100], [101]. The resulting configurations can be saved on presents and be employed to dynamically configure the circuit [102]. The auto-routing algorithm is employed to determine any optical path and/or interferometric structure automatically, given a waveguide mesh topology and a set of specifications. In addition, the routine leads to unprecedented self-healing and fault-tolerant capabilities of the PIC, where given a set of damaged areas of the circuit, the algorithm is able to find alternative sub-optimal paths through the photonic arrangement.

6.4.2 Advanced optimization methods. Self-configuration of waveguide mesh arrangements.

Computational optimization and machine learning techniques have become a new toolbox in different applications fields [103]. In addition, computational optimization methods and more

simplified routines have been applied for the configuration of optical filters [104] and multiport interferometers [12]. In all the former one single application is targeted.

Very recently, the challenging task of under the configuration of waveguide mesh arrangements have been demonstrated using advanced optimization methods. In this case, the phase shifters are the weights or variables in an optimization task. Routines such us gradient descent, and non-derivative methods can be used to minimize a cost function dealing with the targeted application [105]. In this case, the non-ideal effects (both dynamic and passive) are addressed automatically as part of the black-box system behaviour.

In short, the future evolution of large-scale programmable PICs demands the maturity of key enabling technologies such as low loss, low-power consumption and low-footprint unit cells, dense electrical interfacing for low-speed signals, and high-speed electronics co-integration. In parallel, the software layer capabilities will grow to mitigate the necessity for perfect components and enable resilient and fault-tolerant circuits, [106].

7. Applications

Programmable photonics can find applications in a myriad of areas, as we will illustrate in this section. Interestingly, one of the first fields in which it has had an earlier penetration is that of Quantum Information that encompasses, communications, computing, sensing and tomography. Proof of many of these topics using lightwave technology require the use of reconfigurable linear optics transformations and at earlier stages these have been implemented resorting to large scale bulk optics setups, which prevent the development of more complex and scalable quantum optics configurations requiring tens or hundreds of modes. On top of this, linear optic systems with the required fidelity require a strict control of interference though demanding phase stability mechanisms. Integrating a considerable number of photonic elements on a chip in order to implement multiport interferometers as described in sections 4 and 6 has been identified as the only viable path leading towards quantum information systems at a technological reach. Programmability brings the added value of enabling successive implementations of quantum optics experiments featuring random variation in the parameters of interest. We provide a brief introduction to the applications of programmable photonics to quantum information systems. Though the applications are many we focus in particular our attention to linear optical quantum gates and quantum transport simulation. Other applications such as boson sampling and complex Hadamard transformations the reader is directed to the literature [12], [107], [108].

The second and probably wider area of application of programmable photonics is in classical systems. While so far most of these systems have relied mainly on pure fixed application specific photonic circuits, the advantages brought by programmability can become decisive when these systems grow in complexity. Here we review several application areas where programmable photonics can become the pervasive enabling technology in the near future. We start with optical switching interconnection and routing, which is, arguably, the classical area of application where integrated photonics has been adopted at an earlier stage. Here programmable photonics provides a myriad of powerful solutions that encompass not only pure spatial switching and routing, but also broadcasting and wavelength selective operation. A second emerging field of application is Artificial Intelligence and neurocomputing. Programmable photonics enables the implementation of reconfigurable analog cores required for the operation of neural networks and neurophotonic systems. Recent works have reported first proof of concept results showing very promising outputs. Microwave and analog photonics is a particularly appealing area for programmable photonics as it can provide substantial cost reductions and broadband operation flexibility by enabling the possibility of implementing most of the required functionalities in a single chip. The use of these functionalities spans a huge area of applications including 5G communications, satellite payloads, electromagnetic and photonic radar, Internet of Things, and autonomous driving, among others. We have not

tried to be exhaustive, but rather show through different examples of the broad range of applications in which programmable photonics is called to play a relevant role within the next future.

7.1 Quantum information processing

Quantum photonics relies on the encoding of photons into input quantum states, the processing of these states through a reliable linear optics unitary transformation and subsequent measurement of the resulting output quantum state via optical detection [13], [56], [57], [109-116]. Through this scheme novel and powerful techniques for computation, measurement and communications can be developed leveraging on the properties of quantum superposition and entanglement [56]. Many experiments have been reported during the last years [111], [112], that have demonstrated systems with increased complexity that have required a migration from bulk optics configurations to integrated optics implementations to provide a higher spatial mode count, phase stability and fidelity [13], [59], [113]-[116]. Integrated optics provides additional advantages that include low loss, potential for high-density circuit integration, strict optical path and interference control and strong photon interaction exploiting nonlinearities. The merging of these two technologies has led to the new field of integrated quantum photonics [114], [116]. The initial work on integrated quantum photonics focused on glass-based waveguide circuits, most notably by planar and laser-written Silica on Silicon technologies [113], [114], which enabled mode field dimensions comparable to those of single-mode optical fibers. Quantum logic, bosonic sampling, teleportation, and multi-particle quantum walks were demonstrated among other functionalities. The low refractive index contrast nature of these technologies that featured an excellent performance in terms of propagation and coupling losses limits at the same time the circuit footprint principally as a consequence of the high values of their minimum allowed waveguide-bending radius. Circuits with even modest complexity require footprints in the order of several cm and this precludes the use of this technology for scaling their complexity and functionality. To overcome these limitations, one needs to resort to high-index contrast material platforms such as silicon on insulator [59], [116], Si_3N_4 [117], $LiNbO_3$ [118] and InP bearing in mind that reducing photon propagation losses is also a key requirement. Recent experimental results have shown [116], for example, that SOI nanophotonic platforms can implement systems with hundreds of optical components in the same chip. Figure 30 (a) shows a schematic diagram of a programmable photonics quantum processor including its main relevant blocks.

The processor requires one or several *quantum sources*, mainly single photon, with different photon statistics to obtain the required input quantum states/modes. In many cases as we will see, quantum sources need a bright pumping lightwave to generate single photons and therefore, *highly selective tunable filters* will be required at their output to supress the undesired remaining pump signal in order to avoid detector saturation. The input quantum states/modes are then processed by means of a *NxN programmable unitary transformer* based on a linear optics configuration. This is the core element of the quantum processor. Either multiport interferometers, or waveguide meshes, can be employed to implement this block, which might as well include tunable delay lines and switches. Both architectures can implement arbitrary unitary transformations. While multiport interferometers are built to implement either the triangular or rectangular multiport architectures, integrated waveguide meshes can be programmed to emulate any of the two.

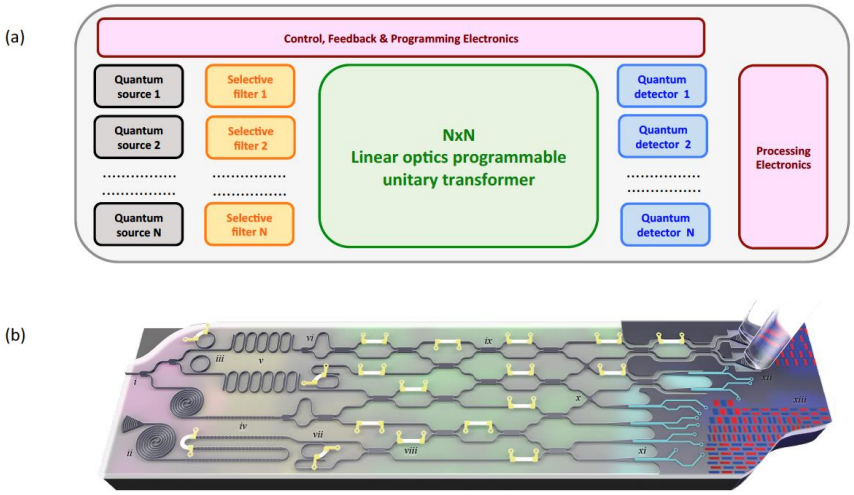

Fig. 30. (a) Schematic Bulk optics implementation of a programmable photonic quantum processor including all the relevant optical and electronic elements. (b) A proposed mock-up for implementation of the main parts of the processor in SOI technology (after [116]). From left to right: photon sources (magenta), pump-removal filters (yellow), passive and active optics (green), single-photon detectors (cyan), and control and feedback electronics (blue). Labels indicate: i. pump input and splitter, ii. Spiralled waveguide photon-pair source, iii. Ring resonator photon-pair source, iv. Bragg reflector pump removal filter, v. coupled-resonator optical waveguide (CROW) pump removal filter, vi. Asymmetric MZI wavelength division multiplexer (WDM), vii. Ring resonator WDM, viii. Thermal phase tuner, ix. Multi-mode interference waveguide coupler (MMI), x. Waveguide crossing, xi. Superconducting nanowire single-photon detector, xii. Grating based fibre-to-chip coupler, and xiii. Control and logic electronics. (The whole figure is reproduced from [59])

In the first case, promising results have been obtained, especially in Silicon Photonics. For instance, a large core with up to 88 MZIs and the capability of providing 26 mode connections has been recently reported. In [13], a $U(6)$ unitary transformer based on a germanium doped Silica PLC in a triangular interferometer arrangement has been demonstrated, where phase shifters are implemented by thermal modulators. Both circuits have been employed in the demonstration of several quantum information processing tasks as will be highlighted later. In the second case, an integrated waveguide mesh can be suitably programmed to emulate the operation of either triangular or square multiport interferometers [23]. For instance, Figure 31 shows an emulation of a square interferometer implementing a $U(9)$ transformation by means of a hexagonal integrated waveguide mesh.

The outcome from the unitary transformer is an output quantum state from which we need to extract some classical information by means of measurement. This is achieved by using quantum or *single photon detectors*. The classical information will need to be further processed by electronic circuits to extract the relevant content. Finally, if the output classical information is required outside the processor then fiber-to-chip couplers can be employed for this task. To achieve full programmability and stable performance the processor needs an *electronic block for control, supervision and programming*. Control and supervision electronics are required first to track and keep the bias points of all programmed photonic components stable against environmental drifts and secondly to supervise the result of any heralding operation. Programming electronics takes care of setting the bias points of all required photonic components to the values provided by the software.

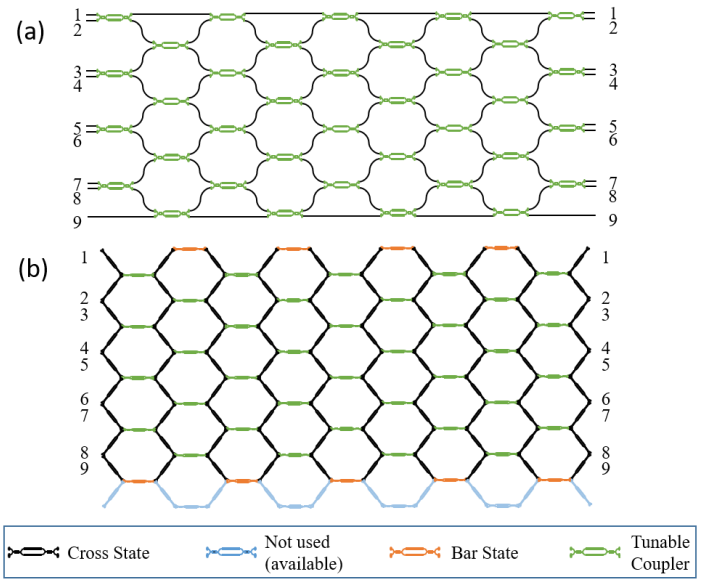

Fig. 31. (a) Rectangular arrangement of a 9x9 interferometer as proposed in [22]. (b) Equivalent implementation using the hexagonal waveguide mesh (after [23]).

Operations required in quantum computing can be implemented using two main approaches [119]. In the first, known as *circuit model*, single or multiqubit gates operate sequentially one after the other on qubits. In the second, known as *cluster state or measurement-based model*, a large entangled state is first created with the aim of using it as a resource state and then single qubit gates are performed to encode the processing. A considerable number of single quantum gates implemented using integrated optical chips have been reported. An interesting example is a large-scale silicon photonic circuit that realizes a fully programmable two-qubit quantum processor has been reported in [120]. The circuit is based on the implementation of a universal two-qubit 4x4 unitary $U \in SU(4)$ by means of a four-operator linear combination:

$$U = \sum_{i=0}^{3} \alpha_i A_i \otimes B_i = \sum_{i=0}^{3} \alpha_i \left(P_1 \sigma_i Q_1\right) \otimes \left(P_2 \sigma_i Q_2\right), \tag{48}$$

where P and Q are single (2x2) qubit gates, σ_i are the identity and the Pauli gates (σ_0 = I; σ_1 = X; σ_2 = Y; σ_3 = Z) and α_i complex coefficients satisfying $\sum_i |\alpha_i|^2 = 1$. Figure 32 shows the layout of a probabilistic implementation of the transformation, $\sum_{i=0}^{2^n} \alpha_i V$, which is implemented when all the n control bits are in the $|0\rangle$ state. U_{LC} is a unitary matrix where the first row is given by $\{\alpha_0, \alpha_1 \ldots \alpha_{n-1}\}$ and the rest are obtained in order to make U_{LC} unitary. For 2-qubit circuits n= 2 and the success probability is ¼. Figure 32 shows a block diagram of this conceptual approach.

The processor was implemented by means of a silicon photonic chip, which was operated in combination with an external electrical control, laser input and fibre-coupled superconducting detectors. The chip footprint was 7.1 × 1.9 mm and consisted of 4 spiral-waveguide spontaneous four wave mixing photon-pair sources, 4 laser pump rejection filters, 82 MMI beam splitters and 58 simultaneously running thermo-optic phase shifters. The device includes five functional parts. An initial front-end comprising three parts implemented the required $SU(4)$ operation, with one partencoding the linear-combination coefficients α_i, another implementing linear terms A_i and B_i, and the third realizing the linear combination of terms $A_i \otimes B_i$ together with post-selection. In a separate area another prepared arbitrary separable two-qubit states $|\psi_{in}\rangle = |\psi_1\rangle \otimes |\psi_2\rangle$ as the input. A final part was employed to rotatee the output state

so that it could be measured at desired basis. The circuit was programmed to implement 98 different two-qubit quantum logic gates and its operation verified by means of tomography. Fi delity results for a variety of gates, including CNOT, CZ, CH, SWAP and iSWAP yield values over 92.4% ill all the cases. Further programming of the chip allowed for the experimental demonstration of a two-qubit quantum approximate optimization algorithm, and efficient simulation of Szegedy directed quantum walks.

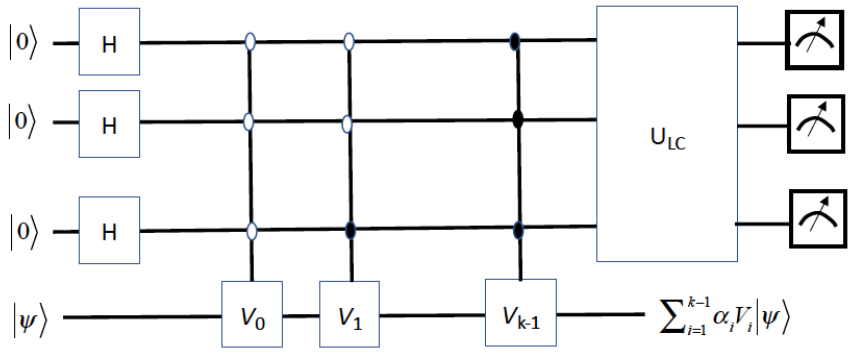

Fig. 32. Layout of a probabilistic implementation of a linear combiner of operators. The linear combination is implemented when all *n* control qubits are measured to be 0. The success probability is 1/*k*. (Adapted from [120]),

Integrated optics is a particularly interesting platform for implementing quantum transport simulation circuits. Both static and dynamic disorders have been introduced by fabricating circuits with random parameter variations or post-processing. Furthermore, linear photonic quantum walks along discrete lattice sites can be implemented by means of waveguides and beam splitters in programmable nanophotonic circuits. In a recent experiment [15] Harris and co-workers reported a complex quantum transport simulator based on a silicon photonics processor composed of 88 MZIs, 26 input modes, 26 output modes, 176 phase shifters. It is capable of implement up to $U(9)$ linear transformations. Figure 33 provides a circuit layout implemented using the silicon chip that includes the cross sites (black points) implemented via the MZIs and the connections between them implemented by means of integrated waveguides. The circuit operation is described as follows: an input state at the left of the circuit will undergo a quantum walk on a one-dimensional chain as it propagates in time to the right. Through the internal phase shifters of the MZIs (θ_i) it is possible to program the splitting ratios of the sites and therefore explore different quantum transport scenarios implemented over a set of discrete sites. In [15] researchers have explored a single quantum walker subject to both static and dynamic phase disorders.

Initially each MZI was set to implement a 50:50 splitting ratio but the external phase shifters (ϕ_i) were programmed to exhibit either static or dynamic phase variations or a combination of both. With this configuration the circuit implements a discrete-time balanced coin 1-D quantum walk. If, for example, a static-only phase variation with sufficient dynamic range is implemented, then photons can be confined to local vicinity in similarity with the Anderson localization.

On the other extreme, if strong dynamic phase variations are incorporated, then ballistic photon diffusion is enabled. The ratio between static and dynamic disorder can be optimized to favour a given ballistic diffusion to a given output waveguide,. The implemented programmable photonic circuit enabled up to 64000 different and unique parameter settings of static and dynamic disorder, which correspond to different quantum transport experiments.

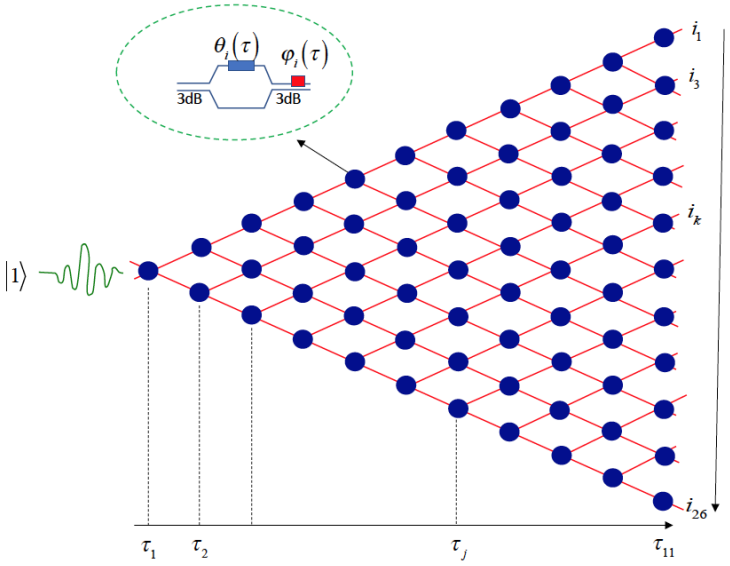

Fig. 33. Layout of the one photon quantum walker circuit (Adapted from [15]). Time (τ) is defined from left to right. Space (i) is defined from top to bottom.

7.2 Switching, interconnections and routing

Optical switching, routing and interconnections implemented by means of integrated photonic chips and controlled by electronic means has been proposed to replace partially or completely electronic switches in two application scenarios [121-123]. The first one is in metro and long-haul communication networks [121], the second is in short-reach communication networks within data centers and even inside the processors of high-performance multicore computers [122], [123]. In the first case the features of dense photonic integration can be crucial for reducing the cost over current switching technologies. This is especially significant if silicon photonics technology is considered for leveraging large-scale integration. In the context of short-reach networks the use of photonic switching avoids the pin and power limitations imposed by electronic switches, eliminate costly and inefficient optoelectronic and electrooptic conversions and therefore enable higher bandwidth operation. In this case it is envisaged that optical switches will co-exist with conventional electronic switches.

The core element of an optical switch is the 2x2 switch cell [121], which is nothing but a unitary 2x2 gate U usually programmed or driven to be either in the cross or the bar state (i.e., (23) with either $\theta = \pi$ or $\theta = 0$, respectively). Several design approaches and technologies can be employed to implement integrated switch cells and switch fabrics and the reader can find a very complete description, for instance, in [121], [122]. For programmable photonics, the most interesting are, on one hand, those that employ integrated interference-based switch cells based on integrated directional couplers [124], MZIs [53], [125], [126] and Ring resonator devices [127]-[130] and, on the other hand, those based on MEMs [130]-[133]. Switch cells can be grouped and assembled to form switch fabrics in a variety of topologies. Some of these, like the Butterfly and the Benes architectures [134]-[136] are not particularly well suited for programmable integrated photonics since they either do not provide path diversity or result in a considerable level of crosstalk (requiring, in addition, several waveguide crossings per established path). Cross-point switch matrix structures are much more amenable for integrated photonic implementations [129], [133], [137]-[140]. Several programmable cross-point switch

fabrics have been reported in the literature both in InP as well as in Silicon Photonics. For instance, a 8x8 switch fabric arranged in an *N*-stage planar topology of 28 MZIs, shown in Figure 34 (a)-(b), was recently reported [140] that constitutes the largest integrated MZI circuit in InP platform so far.

This configuration suffered from various limitations that affect scalability. In first place, non-uniform polarization behaviour degraded the crosstalk level from -20 to -11 dB for the TE polarization. This non-uniformity can be corrected as it was attributed to fabrication variability. More important, however is the limitation due to insertion losses, which can be compensated by combining the MZI-based switch cells with semiconductor optical amplifiers [144], where these elements help in addition to improve the crosstalk to values close to -40 dB. The availability of these low-crosstalk cells shown in Figure 34 (c) with almost negligible losses and crosstalk enables their intermediate assembly into dilated Benes 4x4 blocks shown in Figure 34 (c), extending the scale of InP switch fabrics to up to 128x128 port counts [141].

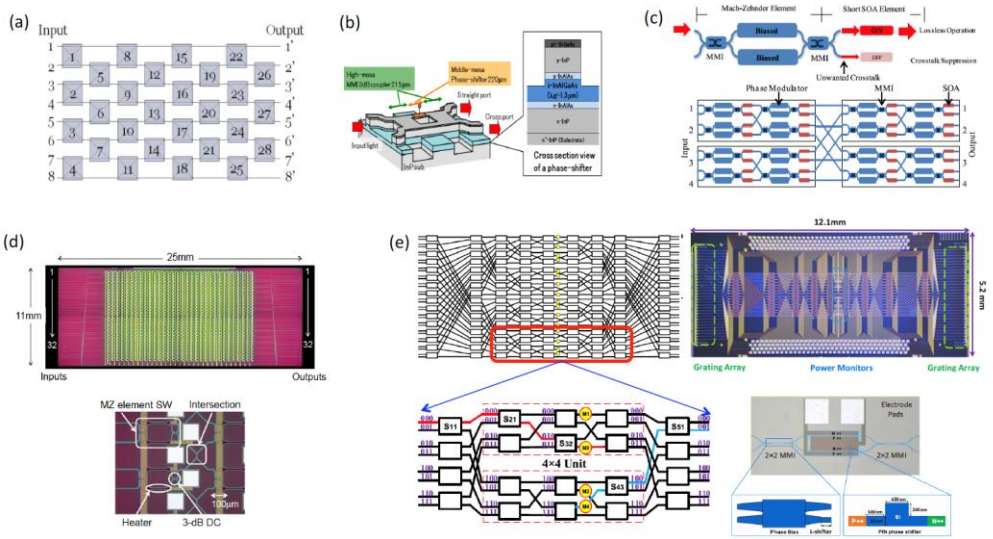

Fig. 34. (a) Layout of a passive 8x8 InP switch fabric (after [140]). (b) Detail of the elementary 2x2 switch cell corresponding to (a). (c) Active 2x2 interferometric InP switch cell combining an MZI and semiconductor optical amplifiers and construction of a 4x4 switch fabric by dilated combination of such cells (after [141]). (d) Photograph and detail of a 2x2 switch cell of a Silicon Photonics 32x32 switch fabric incorporating 1024 MZIs switching cells and thermo-optic phase shifters (after [142]). (e) Layout and chip photograph of a 32x32 switch fabric incorporating 144 MZIs switching cells and carrier injection PIN activated phase shifters. Also shown the basic switch cell unit with push-pull biasing and the 8x8 Benes building block (after [143]).

A 32x32 monolithic silicon MZI path-independent loss switch fabric shown in Figure 34 (d) implementing 1024 MZIs switching cells and thermo-optic phase shifters has been recently reported [142]. The fabric is electrically packaged by flip-chip attachment to a ceramic interposer with > 2000 bond pads. The thermo-optic phase shifters were operated by means of tunable pulse-width modulation signal generated by a field-programmable gate array. Chip metrics included a total on-chip loss of 6.4 dB, overall coupling losses from 2.8 to 6.8 dB, single path crosstalk around 20 dB below the signal level and a power consumption of 1.9 W with a reconfiguration speed of 30 μs. A more recent design reported a 32x32 switch fabric based on 448 MZI cells activated by thermo-optic phase shifters [143]. The MZI devices were arranged in 12 stages following a dilated topology. The chip also included 900 monitor photodiodes and its metrics included an on-chip loss range of 13-35 dB, single path crosstalk below -30 dB and power consumption below 20 mW. Designs incorporating electro-optic

activated MZIs have also been recently reported. These have the potential for nanosecond scale reconfigurability. In this context carrier injection PIN junctions are the preferred option for phase shifters as they feature higher efficiencies in terms of nm/V leading to a much smaller footprint and lower operating voltage when compared to carrier depletion PN junctions. However, as compared to thermo-optic phase shifters, electro-absorption is an undesired side effect that needs to be compensated. 16x16 configurations have been reported in wire-bonded packages and arranged in a Benes topology. These structures suffered from considerable loss and crosstalk as the effect of free carrier absorption compromised the achievement of ideal cross and bar states in the MZI cells. The high crosstalk effects can be partially mitigated by the use of push-pull configurations for the MZI phase shifters, which brings the additional advantage of reducing their footprint and by migration towards dilated topologies. A 32x32 configuration has been recently reported employing the Benes topology [143]. The basic layout, chip photograph, configuration of the basic building 8x8 Benes fabric and detail of the push pull MZI units are shown in Figure 34 (e). The chip has 144 phase-bias 2×2 MZI-switch units and 288 electrode pads; 16 bi-directional power taps were also implemented in the switch to detect the operation statuses of all 144 units. On-chip insertion losses were 12.9 to 16.5 dB, and the crosstalk ranged from −17.9 to −24.8 dB when all units were in the 'Cross' status. The on-chip insertion losses were 14.4 to 18.5 dB, and the crosstalk ranged from −15.1 to −19.0 dB when all units were in the 'Bar' status.

Switch fabrics have also been proposed using MEMs and ring resonators as basic building blocks. The interested reader can find a detailed account of the most significant results reported so far in the literature [121], [122].

7.3 Artificial intelligence and neurophotonics

The recent demise of different scaling laws that have ruled for several decades in microelectronics is challenging the current dominating Von Neumann approach in computing, characterized by the principal role of a central processing unit (CPU) [145]-[154]. In first place, the breakdown of Moore's law by which the transistor count duplicates each two years is limiting the number of basic processing units per unit of surface. Second, the limitation in microprocessor clock rates caused by current leakage in nm transistors has frozen the growth rate in clock speeds. In third place, severe power consumption restrictions arise in nanometer-scale transistors as the well-known Dennard's scaling law (smaller transistors consume less power) no longer applies and hence the power density of microelectronics no longer stays constant as chips get denser. This is giving rise to the dark silicon phenomenon [146], by which a given percentage of an integrated circuit cannot be powered at the nominal operating voltage to meet power consumption restrictions. In 8-nm nodes, this percentage is estimated to reach a 50%. All in all, the conclusion is that current CPUs have reached a limit in their operating speeds and, as a consequence, interest is shifting towards alternative computing paradigms and hardware architectures that can provide increased processing speed with a reasonable consumption [146].

A paradigmatic example [148] is the human brain, which is capable of a huge processing capacity (around 1020 MAC/s) that is around nine orders of magnitude beyond that of current supercomputers, consuming only 20 W. This is possible because it features a highly distributed processing architecture, where around 10^{11} of basic computing elements known as neurons are highly interconnected (around 10^4 connections per neuron). Inspired by this example neuromorphic computing aims to produce large-scale hardware towards achieving efficiencies commensurable to those of the human brain.

The central hardware supporting a neuromorphic processor is a highly connected platform of neurons known as artificial neural network [154]. This architecture is composed of two basic elements: a set of nonlinear nodes or neurons and a network of reconfigurable (i.e., weighted) interconnections. These are bundled together into the neuromorphic processor itself that

incorporates other external circuitry and systems in charge of implementing learning algorithms, controlling the interconnection weights etc as shown in Figure 35.

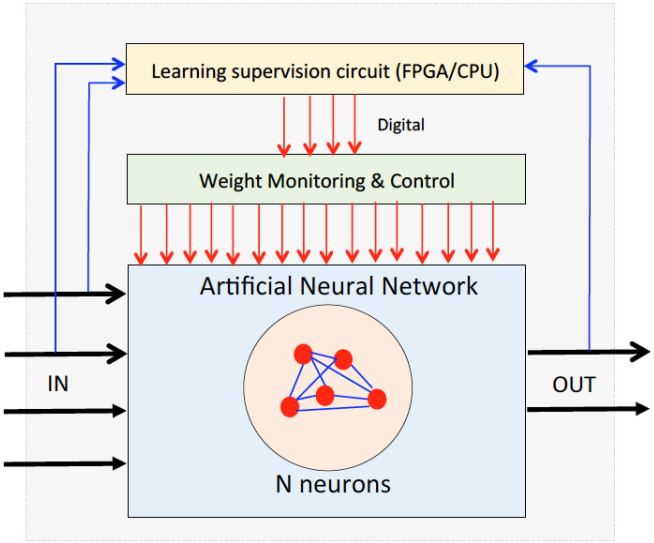

Fig. 35. Schematic description of a neuromorphic processor (Adapted from [148]). While two layers of electronics provide control, supervision and reconfigurability, the programmable artificial neural network operates as the core processor.

While some efforts have been carried to implement electronic neuromorphic systems, these are potentially limited by latency, speed and interconnection bandwidth. Thus, the attention has been turned to leverage on the properties of integrated photonics in terms of high bandwidth, low propagation losses and low latency. An integrated photonic artificial neural network is composed by a set of Processing Network Nodes (PNNs), which can be either all optical or optical/electrical/optical (O/E/O) [146]-[149] as will be explained below and a network of reconfigurable interconnections implemented by means of integrated photonic waveguides.

Recently a multiport interferometer configuration has been proposed for the implementation of *N*-layer feedforward optical artificial neural network [24]. It is based on an integrated programmable nanophotonic processor featuring a cascade array of 56 programmable MZIs in a silicon photonic integrated circuit. The emulated artificial neural network is shown in Figure 36 (a). It is composed of a set of input artificial neurons represented by circles, which are connected to at least one hidden neuron layer and an output neuron layer. Each neuron is then followed by the application of a nonlinear activation function.

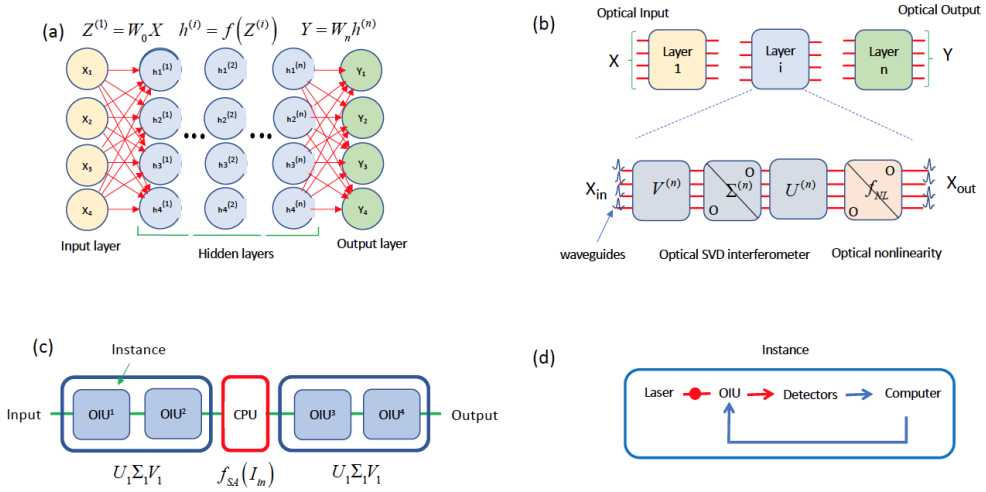

Fig. 36. (a) The schematic feedforward artificial neural network architecture implemented in [24] composed of an input layer, a number of hidden layers and an output layer. (b) Decomposition of the general neural network into individual layers with a detail of the optical interference and nonlinearity units that compose each layer of the artificial neural network. (c) Representation of the two-layer ONN experiment reported in [24]. (d) Experimental feedback and control loop used in the experiment. Laser light is coupled to the OIU, transformed, measured on a photodiode array, and then read on a computer (drawings adapted from [24]).

The internal operation of each artificial neural network layer is shown in Figure 36 (b). Each layer or instance basically consists of two stages. The first is an optical interference unit (OIU) where an arbitrary unitary linear transformation is performed over the input vector $\mathbf{X_i}$ by means of the Singular Value Decomposition (SVD) technique [12]. This linear matrix transformation implements the weighted connections between neurons of adjacent layers. Once the linear transformation has been applied an intermediate vector $\mathbf{Z_i}$ is obtained, the elements of which are individually transformed by a second stage composed of optical nonlinear units (ONUs) that provide the required activation functions and the output vector $\mathbf{Y_i}$.

In the experiment reported, a SVD was implemented using two OIU stages connected by and intermediate layer of MZIs providing the diagonal matrix and the ONUs where implemented offline using a computer CPU. Figure 36 (c) shows the operation of two instances in series and Figure 36 (d) the internal operation of one instance. The ONUs where implemented using CPU that ran a program emulating the response of a saturable absorber.

To implement the OIU a silicon programmable processor was fabricated and employed. It implements a multiport 4x4 triangular architecture and is composed of 56 programmable MZIs each of which comprised a thermooptic phase shifter between two adjacent 50% evanescent directional couplers followed by a second phase shifter. Triangular interferometers implemented 4x4 structures for either the *U* or the *V* unitary matrix in the SVD decomposition [12], while the diagonal matrix interconnecting the *U* and *V* unitary matrices was implemented by means of a linear array of MZI devices. Two chips were required to implement the full SVD decomposition. A two-layer neural network was then assembled using 4 OIU chips and trained for vowel recognition.

7.4 Microwave Photonics

Several basic reconfigurable and programable photonic circuits have been proposed up to date for applications in Microwave Photonics (MWP) [155]-[157]. For instance, in [157], Zhang and Yao proposed a scalable photonic field-programmable disk array signal processor to

perform different MWP signal processing functionalities, including signal filtering, temporal differentiation, time delay, beamforming and spectral shaping. The fundamental units of this processor's core are given by ultra-compact microdisk resonators.

We focus here in programmable systems based on a general-purpose photonic integrated processor using a reconfigurable optical core based on a hexagonal waveguide mesh. We will show that this configuration can be software-defined to perform multiple applications required in MWP by suitable tuning of each element in the processor. Hence, the same hardware can be configured to perform the main functionalities in MWP: Optical delay lines, RF-photonics filtering, optical generation of radiofrequency and millimetre waves, photonic-assisted RF-mixing, instantaneous frequency measurements, etc.

Figure 37 represents a processor architecture suitable for a wide range of RF-photonics applications. All the elements are connected to the reconfigurable optical core in such a way that, not only they produce the desired filtering or delay schemes, but also connect the internal and the external elements required for different functionalities. As highlighted in the right part of the figure, a hybrid design might be needed to achieve the most efficient performance. In this case, a natural choice can be silicon photonics platform (ochre colour) for the passive devices and Indium Phosphide (red colour) for the active devices.

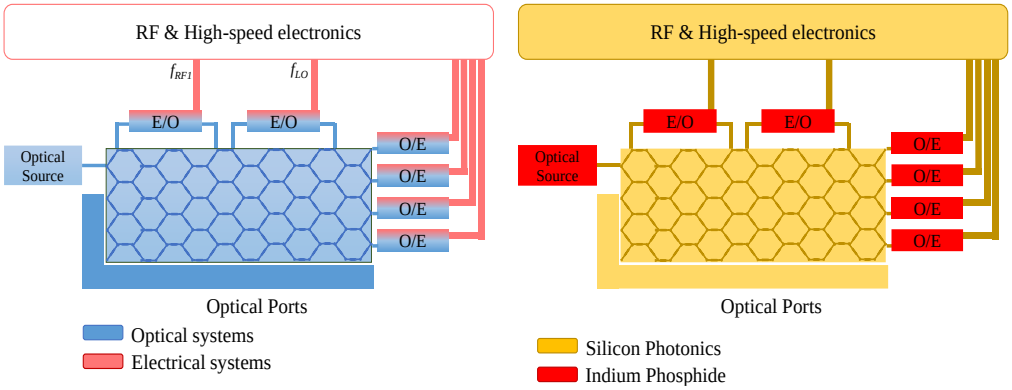

Fig. 37. General-purpose photonic integrated processor architecture and candidate fabrication platforms for each subsystem (After [27]).

Note that an array of optical amplifiers in this platform might be required to overcome the large conversion losses when moving from the radiofrequency to the optical domain. These losses are mainly related to the conversion efficiency of modulators and photodetectors as well as the propagation losses.

To benchmark the multi-purpose processor in terms of frequency response, we consider four different attainable values of BULs for a silicon photonics platform with a group index of 4.18. BUL_1 = 119.5 μm, BUL_2 = 239.7 μm, BUL_3 = 358.6 μm and a larger one of BUL_4 = 597.7 μm. Some of the MWP applications described in this section will be limited to a set of FSR values, a discrete frequency grid or delay given by the chosen BUL. For these examples featuring different BUL values, the resulting FSRs of the filters (ORRs and MZIs) that can be synthesised on the hexagonal mesh are shown in Table 6. The ITU frequency grid has been highlighted for comparison. Radiofrequency bands ranging from the K (20 GHz) up to the E (60 GHz) band are covered by all the proposed examples. In addition, the Vernier effect [158] could be exploited to overcome this limitation and produce greater FSRs. We now discuss a couple among the wide range of MWP functionalities that can be implemented using the programmable processor.

All-optical microwave signal filtering is probably the most widespread application in integrated MWP processors. Specifically, this application brings the possibility of designing fully integrated tunable photonic devices to meet flexible wideband spectral processing requirements for actual and future RF communication bands.

The general scheme of a microwave photonic system consists of an optical source modulated by an external modulator with the RF signal to be processed, followed by an optical core where the RF signal, up-converted to the optical region of the electromagnetic spectrum (at hundreds of THz), is processed by optical techniques and components, such as filters and amplifiers. Finally, the signal can be distributed to large distances or can be down-converted back to the RF domain with a high-speed photodetector resulting in the processed signal in the electrical domain. This scheme leverages on the unique characteristics inherent to photonics like high bandwidth, low losses, tunability and reconfigurability.

Depending on the operation regime, the filter can be based on a summation of optical intensities (ruling out the optical phases) in the case of incoherent operation, or a summation of electric fields, where optical phases are key, in the coherent regime case. In the first one, the shortest delay experienced by the signal inside the filter is much longer than the coherence time of the optical source. It is commonly implemented with discrete and large optical components, where the coefficients are set by optical amplification or attenuators and the delay is given by tunable delay lines to obtain tunable frequency responses. Filters built using optical discrete delay lines and fibre Bragg gratings reach up to 40 dB of Extinction Ratio and quality factors up to 325 with a high number of taps and, hence, require a considerable number of components. Some of them have demonstrated reconfigurability and tunability up to around tens of GHz, but it is quite difficult to maintain the resulting bulky system stable in temperature. Implementation of integrated incoherent MWP is not easy on a chip scale as the inherent small footprint delays call for the use of broadband optical sources to meet the incoherent operation condition.

Table 6: Frequency grid associated to 4 different BULs. The interferometric structure (Ring and/or MZI) available for the hexagonal core is also indicated.

Interferometric length (BULs)	BUL_1 = 119.5 µm FSR(GHz)	BUL_2 = 239.7 µm FSR(GHz)	BUL_3 = 358.6 µm FSR(GHz)	BUL_4 = 597.7 µm FSR(GHz)
2	300.00	150.00	**100.00**	60.00
4	150.00	75.00	**50.00**	30.00
6	**100.00**	**50.00**	33.33	20.00
8	75.00	37.50	**25.00**	15.00
10	60.00	30.00	20.00	12.00
12	**50.00**	**25.00**	16.67	10.00
14	42.86	21.43	14.29	8.57
16	37.50	18.75	12.50	7.50
18	33.33	16.67	11.11	6.67
20	30.00	15.00	10.00	6.00
22	27.27	13.64	9.09	5.45
24	**25.00**	12.50	8.33	5.00
26	23.08	11.54	7.69	4.62
28	21.43	10.71	7.14	4.29
30	20.00	10.00	6.67	4.00

On the other hand, coherent filters, where the longest delay experienced by the signal is much shorter than the coherence time of the optical source are amenable for integration. Integrated optics circuits have been demonstrated recently for the implementation of tunable

coherent optical filters [17], [73], [159]-[162]. In [159], the basic building block for a cascaded coherent filter structure with reconfigurable features was demonstrated in InGaAsP-InP, incorporating a ring resonator in one arm of the MZI. Further passband filtering improvement was reported by the same authors in [160] by extending the number of cascaded stages. Optical Single Side Band Modulation is an interesting particular approach for the implementation of coherent MWP filters as it allows the direct transmission of the transfer filter implemented by the optical core to the RF region of the spectrum. In this case, the detected photocurrent is then proportional to the frequency response of the optical filter at the carrier frequency multiplied by the optical filter response at the RF sideband, mapping the shape of the optical filter transfer function into the electrical domain [163]:

$$i(t) \propto s\left|H(f_o)\right|\cdot\left|H(f_o+f_{RF})\right|\cdot\cos(2\pi f_{RF}-\angle H(f_o)+\angle H(f_o+f_{RF})), \tag{49}$$

where $H(f)$ is the optical filter response at a given RF frequency f.

Furthermore, different modulation and detection schemes can be employed to increase the tunability range, the dynamic range, the gain and the noise figure of the whole system, such as self-heterodyning systems [164], where full-FSR frequency response tunability can be achieved by adding a phase shift into the optical filter and employing a copy of the carrier that was sent to a different path prior modulation.

Coherent filters are usually based on optical filters built from the concatenation of single unit cells such as MZIs (zeros), ring resonators (poles) and ring-loaded MZIs. Tuning can be achieved by adding a simultaneous phase to all the filtering structures. Optimum passband filters like Chebyshev, Butterworth, and Elliptic are possible, where the filter order is related to the number of ring resonators in the structure [54]. The concatenation of unit cells increases the insertion losses of the whole device (if each cell has no zero insertion losses), but, on the other hand, can produce more selective filters as the result of multiplication of their individual frequency responses. Integrated solutions outstand due to their versatility and low SWaP, offering at the same time similar figures of extinction ratio and selectivity comparing to bulk optics designs.

Figure 38 illustrates an application example of the multi-purpose processor hexagonal core for the implementation of MWP filters. It corresponds to a RF-photonic filter employing a self-homodyne modulation/detection scheme. The optical filter stage synthesises, in this case, a 6th order optical filter based on a SCISSOR structure. For the case of RF-photonics filters, the limitation will depend on the modulation scheme: Double side band modulations would have the half-FSR of the optical filter whereas Single-side band modulations map the full FSR of the optical filter to the electrical domain.

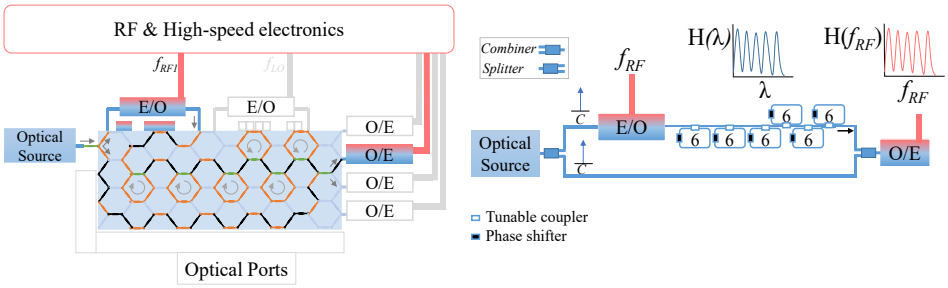

Fig. 38. General-purpose signal processor configuration for RF filtering implementation (left) based on a self-homodyne modulation/detection scheme (right). The optical filter is composed of six cascaded ORRs defined by a cavity length of 6 BULs (After [27]).

Following the values provided in table 6, the optical filter corresponds to an FSR associated to ORRs of 6 BULs of 100, 50, 33.33 and 20 GHz for each selected BUL. A wide variety of optical filters can be synthesised on the hexagonal waveguide core as it has been shown in section 6, which are amenable to be translated into the RF bands by suitable downconversion.

Optical generation of high-quality CW microwave and millimetre-wave (mm-wave) signals can be applied in many fibre-supported microwave and mm-wave systems (including antenna remoting and phased array antennas) with a special interest in the upcoming 5G radio access networks [18], [165]. This functionality allows the generation and distribution of high-frequency RF signals by taking advantage of inherent properties of optics, such as low propagation losses of standard fibres and the availability of fibre amplifiers. Actually, the purely electrical approach faces problems in the generation of signals above 25 GHz, while their distribution is highly challenging due to the propagation losses of coaxial cables. In addition, the increasing bandwidth demand in communications has driven the attention towards the mm-wave band because of the wide bandwidth available for high-data-rate wireless transmission where propagation losses are even higher for purely electrical/RF systems. The main performance figures of photonic-generated RF signals systems are the frequency range where the signal can be generated and the linewidth of the tone. As in every PIC, it is also important to evaluate the power consumption and the potential integration percentage of the system.

There are different reported approaches to generate microwave and mm-wave signals, but most of them are based on optical heterodyning, in which two optical waves of different wavelengths beat at a photodetector generating a tone up to the THz band with a frequency coincide on the difference between the two tones. The phase of the resulting tone will be the difference between the two phases. Thus, in order to generate low-phase noise, the use of correlated optical waves is advisable. The maximum achievable frequency is mainly limited by the photodetector bandwidth (among other specific limits related to each approach).

Methods to generate RF signals can be classified into six groups: Optical injection locking, optical phase locking, optical injection phase locking, external modulator based, optoelectronic oscillators and dual parallel MZMs. The first three have not been able to break the 42-GHz barrier and need two lasers to be working at the same time.

The approach employing an external modulator takes advantage of the frequency up-conversion inherent when a continuous wave signal provided by a laser is modulated by an RF tone. By employing different modulation biasing points, the input frequency can be doubled or even quadrupled by suppressing the odd- or even-order modes, (together with the use of an optical filter to suppress the optical carrier). The linewidth is limited by the input signal and can be as low as 5 Hz. The lowest frequency is limited by the bandwidth of the filter employed to suppress the carrier, while the highest achievable frequency is limited by the photodetector bandwidth and the modulator bandwidth. This technique has reached tone generation up to 60 GHz. The use of a phase modulator instead of an intensity modulator avoids the bias drift problem that would need a control circuit in order to increase the robustness, [166]. An interesting alternative that has achieved an outstanding integration degree is optoelectronic oscillation. The oscillator operates by modulating a continuous wave signal from a laser with an external intensity modulator. The signal goes through a high-Q optical storage stage (Fabry Perot filter or optical delay line) in order to suppress the unwanted modes and provide a cavity round-trip delay. The photodetected signal is injected again into the modulator after the electrical stage as a feedback loop. This architecture has provided a linewidth under 200 Hz and tones ranging from 10 up to 40 GHz, [167].

Finally, the use of a dual parallel MZM maintains a good trade-off between linewidth obtained, (in the range of tens of Hz), and achievable frequency, (that ranges from very low frequencies up to 60 GHz and is actually limited by the photodetector and the modulator bandwidth). In this case, a MZM is connected at each arm of an outer MZM forming a third interferometric structure. This structure can provide optical carrier suppressed modulations

without using an optical filter. The generated tone is then the difference between the optically modulated tones. Regarding power consumption, this structure only needs an optical source and an optical amplifier to increase the conversion gain.

While none of the aforementioned analysed structures has been completely integrated on a complex PIC, recently an integrated optoelectronic oscillator, where the optical components, including a directly modulated laser source, a spiral-shaped optical delay line and a high-speed photodetector, were fabricated on an indium phosphide substrate has been reported [168].

The multi-purpose programmable MWP processor architecture enables the synthesis of different schemes for generating continuous wave RF signals. Figure 39 shows, for instance the processor configurations implementing different approaches: (a) the external modulator approach, (b) the optoelectronic oscillator approach. Note that if a dual parallel MZM were included in the architecture, this technique could be integrated as well. The achievable frequencies would mainly depend on the modulator and photodetector performance. Particularly, the bandwidth limitation in (a) due to the optical filter might be determined by the UMZI FSR of ΔL = 2 BULs, ranging from 300 up to 60 GHz for the selected BUL examples.

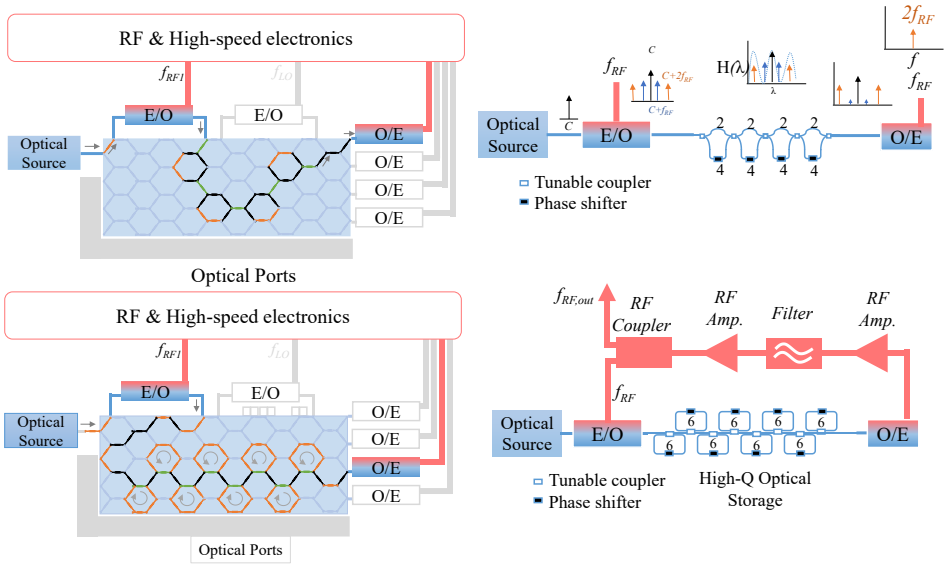

Fig. 39. General-purpose signal processor configuration for microwave and mm-wave tone generation based on (upper) external modulator approach, (bottom) optoelectronic oscillation approach. The right figures illustrate the targeted configuration schemes (After [27]).

8. Summary, conclusions, challenges and future avenues of research

We have reviewed some of the basic principles, fundamentals, technologies and architectures for the implementation of programmable integrated photonic circuits and systems. As we have outlined at the beginning of this paper, programmable photonics is in a way following similar steps as programmable electronics did in the last two decades of the last century. Figure 40 shows a time frame evolution of both fields, where some salient milestones are outlined.

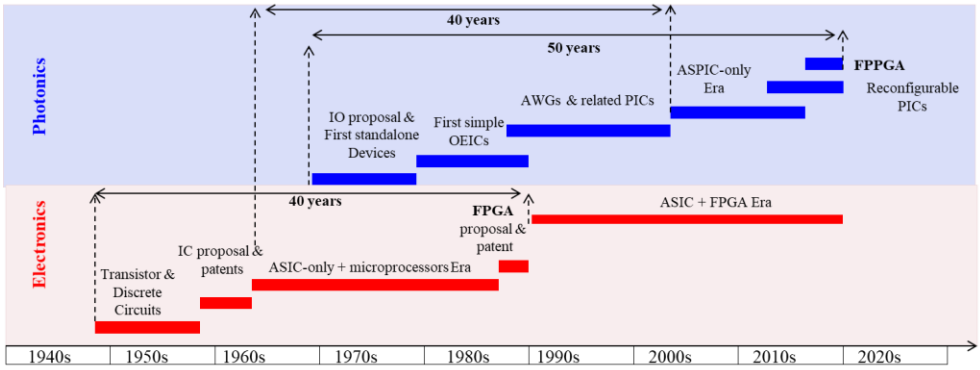

Fig. 40. Significant milestones and evolution periods in integrated electronics and photonics (Authors elaboration).

While the similarity of the main evolution paths can be identified, it is important to acknowledge that there are as well important differences. The first important difference is that signal processing in PIP is analog as opposed to the digital character of integrated electronic chips. The lack of optical memories precludes digital operations for which a previous analog to digital conversion plus bit storage is required. All optical signal processing has to be performed on the fly, as the analog signal propagates. Rather than being a limitation, this should be considered as a complementary feature brought by photonics which, if conveniently leveraged and complemented to the digital nature of electronics can open a completely new signal processing paradigm where both worlds cooperate synergistically to benefit a given application field. One example is artificial intelligence, where computing paradigms based on analog signal processing are being now considered as a means to emulate basic operations carried out by neurons, which are complementary and outperform some of those carried by digital processing.

To fully exploit the capabilities of PIP and analog signal processing research is necessary in different areas:

a) The development of a theoretical background for analog optical gates based on a $SU(2)$ algebra of rotation matrices that can play a similar role as Boole algebra in digital electronics.
b) Further investigation on efficient decompositions of complex multiport interferometric and waveguide mesh architectures in terms of $SU(2)$ gates.
c) Developing arbitrary circuit synthesis algorithms for PIP structures.
d) Developing power-efficient mechanisms for the implementation of phase-shifters, possibly using non-volatile approaches.
e) Developing monitoring and control hardware and software capable of supervising an extensive number of TBUs in real time.
f) Developing routing and placement software to optimize the allocation of the programmed circuit/s within the available real estate in the chip and reroute connections in case of one or multiple TBU failures.
g) Investigation on the alternatives to scale interferometers and waveguide meshes by increasing the number of TBUs. In particular, by adding active elements for loss compensation, by the reduction of the TBU footprint and by reducing the insertion losses of the passive elements.
h) Developing the technology to co-integrate PIP circuits with sophisticated programming and control electronics.

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Acknowledgments

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