Ferroelectric, Analog Resistive Switching in BEOL Compatible TiN/HfZrO₄/TiO_x Junctions

Laura Bégon-Lours^{1}, Mattia Halter^{1,2}, Youri Popoff^{1,2} and Bert Jan Offrein¹*

Dr. L. Bégon-Lours, M. Halter, Y. Popoff, Dr. B. J. Offrein

IBM Research GmbH - Zurich Research Laboratory, CH-8803 Rüschlikon, Switzerland

E-mail: lbe@zurich.ibm.com

M. Halter, Y. Popoff

Integrated Systems Laboratory, ETH Zurich, CH-8092 Zurich, Switzerland

Keywords: neuromorphic hardware, memristors, hafnium zirconate, ferroelectrics

Abstract: Thanks to their compatibility with CMOS technologies, hafnium based ferroelectric devices receive increasing interest for the fabrication of neuromorphic hardware. In this work, an analog resistive memory device is fabricated with a process developed for Back-End-Of-Line integration. A 4.5 nm thick HfZrO₄ (HZO) layer is crystallized into the ferroelectric phase, a thickness thin enough to allow electrical conduction through the layer. A TiO_x interlayer is used to create an asymmetric junction as required for transferring a polarization state change into a modification of the conductivity. Memristive functionality is obtained, in the pristine state as well as after ferroelectric wake-up, involving redistribution of oxygen vacancies in the ferroelectric layer. The resistive switching is shown to originate directly from the ferroelectric properties of the HZO layer.

1. Introduction

Mimicking the brain, “deep-learning” algorithms are structured into layers of interconnected neurons. As the information flows from one layer to the next, matrix-vector multiplications are performed. The matrix elements, called “synaptic weights” by analogy with the biological synapses, are updated during the training of the neural network. With current “classical” computer architectures, vector-matrix multiplications demand a large computing power. To keep pace with the ever increasing workload and neural network complexity, efficient bio-inspired hardware accelerators supporting deep-learning are being developed.^[1,2] Their building block, emulating the synapse, is the memristor:^[3] a resistance whose value can vary reversibly upon an external stimuli, in a persistent way. The matrix vector multiplication is then performed by applying input potentials on a cross-bar array of memristors, and measuring the output currents.^[4] Among the technologies explored to demonstrate memristors^[5,6], the choice of ferroelectric materials is attractive as the polarization can be changed by the application of an external electric field and is remnant: the non-destructive read-out of the synapse is possible for bias fields across the ferroelectric layer lower than its coercive field. The growth of high-quality epitaxial thin-films allowed the demonstration of two and three terminals ferroelectric memristors: Ferroelectric Tunnel Junctions (FTJs) with perovskites^[7–10] as well as recently with HfZrO₄ (HZO),^[11] Ferroelectric Field-Effect Transistors (FeFETs)...^[12] However, integrating such synapses on CMOS neurons remains challenging and expensive, requiring flip-chip or wafer-bonding techniques. Recently, the discovery of ferroelectricity in doped hafnium oxide^[13], in particular HZO^[14] enabled the demonstration of ferroelectric memristors in the Front-End-Of-Line (FEOL),^[15–17] and transistors with Back-End-Of-Line (BEOL) compatible processes.^[18,19] The latter is made possible by annealing, permitting a crystallization in the ferroelectric phase with a low thermal budget.^[20] BEOL processes not exceeding 400°C is critical for industrializing beyond-Von-Neumann hardware in CMOS based silicon technology.

A two-terminals ferroelectric memristor consists of a ferroelectric layer separating two different electrodes. Upon polarization reversal, the energy profile and thus the transport probability of carriers across the ferroelectric layer is modified. Their fabrication is challenging as the ferroelectric layer must be thick enough to stabilize ferroelectricity, a fortiori in multiple configurations, but thin enough to allow electric conduction. These conditions have been obtained for polycrystalline HZO at temperatures above 450°C.^[21–25] A reduced thermal budget is less critical for thicker films: 10 nm layers have been for example crystallized at 400°C.^[26–28] In this paper, we demonstrate non-volatile resistive switching (memristive functionality) in a 4.5 nm thick ferroelectric layer in a BEOL compatible stack. A reduced thermal budget (~375°C) is used as well as abundant and CMOS compatible materials (Hf, Zr, Ti). We show that resistive switching is enhanced after ferroelectric wake-up and that it originates from the ferroelectric polarization.

2. Fabrication of a ferroelectric resistive memory:

The co-integration of ferroelectric memristive synapses in the BEOL with CMOS neurons is challenging because the thermal budget should not exceed 400°C to avoid any damage to the FEOL circuitry. The choice of materials – TiN, HZO and an interlayer of conducting TiO_x – is motivated by the moderate temperature of the Atomic Layer Deposition (ALD) growth process, as well as the conformal growth mode enabling eventual 3D integration. First, a 20 nm thick bottom electrode of TiN is deposited on a SiO₂//Si substrate. Then, a 3.5 nm thick TiO_x interlayer is deposited to create an asymmetry in the energy profile of the oxide barrier, necessary for resistive switching upon ferroelectric polarization reversal.^[23] On top is a 4.5 nm thick HZO layer and a 10 nm thick TiN top electrode. All the above layers are amorphous after the ALD deposition. The choice of TiN as a capping layer is to promote the crystallization of HZO in the ferroelectric phase by a mechanical constraint during the annealing.^[29] The crystallization at a moderate thermal budget is obtained using a ms-Flash Lamp Annealing (ms-

FLA)^[20] where the wafer is pre-heated to 375°C, then exposed to a 20 ms long flash of 70 J.cm⁻². The I_d - V_g characteristics of P- and N-MOS (130 nm) test transistors were not affected by such treatment, showing the CMOS compatibility of the process. The Grazing Incidence X-Ray Diffraction (GIXRD) spectra in **Figure 1** shows HZO crystallized in the orthorhombic or tetragonal phase and that no fraction of monoclinic phase is found. The Scherrer fit of the HZO peak at 30 deg indicates that the in-plane grain size is 3.5~4.5 nm, for a k factor of 0.7~1. X-Ray Reflectivity (XRR) spectra indicate sharp interfaces with small roughness (**Figure S1**). After deposition of a top W electrode, circular capacitors are then fabricated using standard optical lithography techniques described in the experimental section. The diameter is chosen in the range 40-140 μ m to enable the measurement of the resistance for voltages smaller than the coercive field of the 4.5 nm thick HZO, i.e. in the $10^{-3} \sim 10^{-2}$ V range. With this constraint, the footprint of the devices can in principle be reduced by thinning the HZO layer: ferroelectricity was demonstrated in HZO films (here, epitaxial) as thin as 2 nm.^[30,31]

3. Non-volatile resistive switching:

To demonstrate memristive functionality of the resistive memory, we first apply “write” DC pulses of a voltage V_{write} across the device, while the bottom electrode (HZO/TiO_x/TiN interface) is grounded. The bias is then set back to zero, and, approximatively ten seconds later, the resistance of the junction is measured by applying a “read” voltage of only 100 mV to the top electrode. The value of 100 mV is chosen to remain below the coercive field of the ferroelectric, thus not modifying the state of the device (non-destructive read-out). The results of this write/read experiment for three different devices of same dimensions (variability ~ 6%) are plotted in **Figure 2**.

After applying $V_{\text{write}} = -1.5$ V, the junction is in a Low Resistive State (LRS). Upon the application of pulses of increasing voltage, the resistance remains stable until it increases sharply at $V_{\text{write}} = 0.3$ V. The resistance then gradually increases (RESET), and the device

reaches a High Resistive State (HRS). With pulses of decreasing voltage, the resistance remains stable until it decreases sharply at $V_{\text{write}} = -0.45$ V. A gradual decrease in resistance is then observed until it reaches its initial value (low resistive state, SET). In the conditions of the experiment, a moderate drift of the LRS is observed (a few tens of kOhms from cycle to cycle). A drift is also observed on a longer timescale: three devices poled in the LRS, HRS and in an intermediate state all see their resistance increase by 0.5 GOhms after six days (see **Figure S2**). The memory of the state (LRS, HRS or intermediate) is preserved. The experiment demonstrates the non-volatile, analog, reversible resistive switching in the 4.5 nm thick HZO device.

To get further insights on the mechanisms of conduction through the diode, capacitors of various sizes (40 to 140 μm) were measured. The resistances in the low and high resistive state scale with the inverse of the area of the junction (see **Figure S3**) indicating that the conduction is homogeneous and not due to the formation of a filament^[32] through the HZO. The ON/OFF ratio, defined as the ratio of the resistances in the high and the low resistive states, does not vary with the dimension of the devices, indicating that no pinning occurs at the edges and further pointing to a homogeneous conduction through the whole area of the device. In addition, similar devices with amorphous HZO were measured, and did not show resistive switching, as shown in **Figure S4**.

In **Figure S5** is shown the I-V characteristics for a pristine device and for a device after a “wake-up” of 10^5 cycles at ± 2 V, 100 kHz: the shape of the characteristics at small bias are similar before and after wake-up, as well as in the HRS and the LRS, but the current is proportionally larger in the LRS and after wake-up. The I-V characteristics around $V_{\text{read}} = 100$ mV can be well described by a direct tunneling current (Brinkman model^[33]) through a symmetric barrier height of 0.42 to 0.48 eV. However, temperature dependent measurements show that the current increases with the temperature, indicating that direct tunneling is not the dominant mechanism.

For comparison, direct tunneling was observed at low temperature (50 K) in magnetic tunnel junctions on 2 nm thick epitaxial HZO films.^[30]

Around 300 K and at small bias ($V < 50$ mV), Ohmic conduction is dominant (see **Figure S6**) and is observed in a conduction band at 0.24 eV above the Fermi level in the LRS and 0.26 eV in the HRS: this difference of energy explains the resistive switching observed for $V < 50$ mV but also at V_{read} (see **Figure S5**). This value of energy difference between the conduction band and the Fermi level is small compared to the band gap of HZO (~ 3.5 eV) which indicates the presence of an impurity level in the band gap, from which the electrons are excited.^[34]

The change in the energy barrier between the LRS and the HRS is less than what is measured in epitaxial films of the same thickness^[35], which can be explained by the smaller effective polarization in polycrystalline films and the presence of defects at the interfaces of the ferroelectric film, screening the ferroelectric field-effect.

In thicker (10 nm) films, the read voltage is generally higher to obtain a measurable current, and the conduction mechanisms are different: in ref^[36], the conduction around $V_{\text{read}} = 2$ V is described with thermionic injection, with a change in the barrier height as high as 0.1 eV. In junctions based on a dielectric interlayer^[25,37] (e.g. Al_2O_3), the energy profile is engineered in such a way that the electrons see the full width of the 10 nm HfO_2 film in the HRS and only the interlayer in the LRS, resulting in a large ON/OFF but in small current densities in the HRS: typically 10^{-7} A.cm⁻² at a read voltage of 2 V,^[17] compared to 10^{-6} A.cm⁻² at a read voltage of 100 mV for the devices presented in this work.

4. Improved resistive switching with ferroelectric wake-up

Figure 3 shows Dynamic Hysteresis Measurements (DHM) of an 80 μm diameter device during wake-up. The polarization of the pristine loop (in pink, thick line) is pinched and the remnant polarization is $2P_r = 7.5$ $\mu\text{C}\cdot\text{cm}^{-2}$. After $1\text{E}5$ cycles, the polarization increases to $2P_r = 24.6$ $\mu\text{C}\cdot\text{cm}^{-2}$. The wake-up effect is known for HZO films and is attributed to the redistribution

of oxygen vacancies.^[38,39] From the current loops (thin lines) we observe that for the pristine device, the switching current is maximal at -1.6 V and 1.8 V. These values then reduce to -0.7 V and 0.7 V. This effect is explained by a strong ferroelectric domain pinning due to interfacial defects,^[40] released by cycling the device at bias larger than the coercive field after wake-up. Similarly, smaller voltages are needed to switch the device from the HRS to the LRS, indicating that the electroresistance originates from the ferroelectricity, as further discussed in section 5. Fatigue measurements (see **Figure S7**) at an amplitude of 2 V and a frequency of 100 kHz show a maximal polarization after 5E6 cycles and a rupture after 2E8 cycles.

The experiment described in Section 3 is repeated on an 80 μm diameter device after wake-up. The resistance measured at 100 mV for varying V_{write} bias before and after the wake-up is shown in **Figure 4**.

The logarithmic scale emphasizes the increased ON/OFF ratio after wake-up, from 1.3 to 2.0. In section 3, we established the existence of an impurity level in the gap of HZO, which could be due to oxygen vacancies.^[41] In this scenario, the decrease of the resistance in the LRS is by a factor 5 could be a consequence of the redistribution of oxygen vacancies during wake-up from the interface to the bulk of the HZO layer.^[39] For negative voltages, the saturation is reached at -1.0 V, compared to -1.4 V before wake-up, indicating a more efficient screening of the polarization in the low resistive state, as further discussed in section 5.

5. Ferroelectric switching mechanisms

Figure 5 shows Positive Up Negative Down (PUND) measurements on the woken-up devices: the ranges within which resistive switching is observed correspond to the switching current (yellow regions in the inset showing the current as a function of the voltage: [-1.2 V;-0.2 V] and [0.1 V;1.6 V]), confirming the ferroelectric origin of the resistive switching.

The I-V characteristics of an 80 μm diameter device with and without wake-up are represented in **Figure S5**. The inset shows the I-V characteristics at small fields in the high and the low resistive states, reflecting the measurements shown in Figure 2 and Figure 4.

The I-V are highly non-linear, which is of technological interest for neuromorphic computing: in selector-less cross-bar arrays, non-linear characteristics can prevent current sneak paths by blocking unselected devices.^[42] In comparison, the I-V characteristics of a TiN/HZO (3 nm)/TiO_x (3 nm)/TiN/SiO₂//Si device are quasi linear (not shown) and the current density is two orders of magnitude higher: this indicates that the TiO_x/TiN contact is ohmic and that the resistance of the junction is dominated by the transport through the HZO layer. Ferroelectric diodes with metallic electrodes typically show p-n behavior for one polarization direction and n-p behavior for the opposite polarization direction^[27,43]. In this work, before wake-up the I-V characteristics are almost symmetric. After wake-up, the I-V characteristics keep the same polarity regardless of the polarization direction, showing that the energy band diagram of the TiN/HZO/TiO_x junction is not structurally modified upon polarization reversal.

The proposed mechanism is represented in **Figure 6** and is as follows: during the application of $V_{\text{write}} = -1.5$ V, the ferroelectric layer is polarized towards the TiO_x layer (i). The polarization remains after setting V_{write} to zero. In the TiN (metallic) layer, the polarization is screened across a distance of less than one angstrom. However, the carrier density in the TiO_x layer is lower, and consequently the screening occurs over a larger distance.^[44] Oxygen deficient TiO_x is a n-type semiconductor.^[45] When the ferroelectric layer is polarized towards the TiO_x layer, electrons screen the ferroelectric polarization and accumulate in the TiO_x layer, which therefore becomes more conducting (low resistive state). Applying further pulses in the range from -1.35 V to 0.1 V does not modify the resistance (no cumulative switching), consistent with an unchanged ferroelectric domain configuration. The HZO film is polycrystalline: above $V_{\text{write}} = 0.1$ V, a fraction of domains sees their polarization reverse for each additional pulse of increasing V_{write} (ii). The broad distribution of coercive fields is due to the polycrystalline nature

of the film and the size of the device that is large compared to the size of the HZO grains (see Figure 1). Reducing the lateral dimensions of the devices to several nanometers would typically lead to a discretization of the available intermediate states, as observed in nanoscale FeFETs.^[16] Note that in epitaxial ferroelectric tunnel junctions (in absence of crystalline grains) analog resistive switching is also observable, with the gradual switching of nanometric ferroelectric domains.^[46,47] The distribution appears broader when a positive bias is applied (ii) than when a negative bias is applied (iv): as the ferroelectric domains are polarized outwards the TiO_x layer, the latter is locally depleted in electrons and the polarization is not well screened. Consequently, some of the domains do not switch or switch back to the initial direction, until sufficient surrounding domains have switched to stabilize the ferroelectricity. After poling the ferroelectric polarization outwards the TiO_x layer (iii) two effects can explain the high resistive state: on one hand, the TiO_x layer is depleted near the HZO interface, which increases the thickness of the insulating barrier. On the other hand, the polarization field increases the energy barrier height at the TiO_x /HZO interface.

6. Conclusion

Analog resistive memories were fabricated with a CMOS compatible BEOL process. Ferroelectricity was obtained in a 4.5 nm thick HZO layer crystallized with a moderate thermal budget of $\sim 375^\circ\text{C}$. A 3.5 nm thick semi-conducting TiO_x interlayer was used to create an asymmetry in the energy profile of a $\text{TiN}/\text{HZO}/\text{TiN}$ capacitor. The synaptic functionality (non-volatility and plasticity) was further enhanced after a ferroelectric wake-up of the devices. Electrical characterization confirms that the resistive switching originates from the ferroelectric properties of the HZO layer. These preliminary results raise interest in further understanding the role of the oxygen vacancies in the conduction mechanisms and the polarization to enhance the memristive functionality of HZO diodes.

Experimental Section/Methods

Fabrication:

200 nm of SiO₂ were deposited on an Si n⁺ substrate by Plasma Enhanced Chemical Vapor Deposition (PECVD) at 300 °C. Then, 15 nm TiN was deposited in a Plasma-Enhanced Atomic Layer Deposition (PEALD) system using a tetrakis-(dimethylamino)titanium (TDMAT) precursor and N₂/H₂ plasma at 300°C. Subsequently, 3.5 nm TiO₂ was deposited using TDMAT precursor and O₂ at 300°C, followed by 4.5 nm HZO that was grown in a process using alternating cycles of tetrakis-(ethylmethylamino)hafnium (TEMAH) and ZrCMMM ((MeCp)-2Zr(OMe)(Me)) at 300°C. The composition of HZO for these conditions was determined to be Hf_{0.57}Zr_{0.43}O₂ (not shown) by Rutherford backscattering (RBS) analysis. Finally, a capping layer of 10 nm TiN was additionally grown. The sample was then annealed at 375°C with a millisecond flash lamp anneal (ms-FLA)^[20] and then transferred to a sputter chamber for the deposition of 100 nm W. Capacitors were defined by a optical lithography step and Reactive Ion Etching (RIE) etch step of the W using a SF₆/O₂ plasma.

Characterization:

GIXRD and X-ray Reflectivity XRR measurements were performed by a Bruker D8 Discover diffractometer equipped with a rotating anode generator. The electrical characterization was carried out on a Agilent B1500A semiconductor analyzer and an AixACCT TF Analyzer 2000.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This work is funded by H2020 “FREEMIND” (n° 840903), H2020 "ULPEC" (no732642) and H2020 “BeFerroSynaptic” (n° 871737).

Received: ((will be filled in by the editorial staff))

Revised: ((will be filled in by the editorial staff))

Published online: ((will be filled in by the editorial staff))

References

- [1] A. Sebastian, M. Le Gallo, R. Khaddam-Aljameh, E. Eleftheriou, *Nat. Nanotechnol.* **2020**, DOI 10.1038/s41565-020-0655-z.
- [2] H. Zhang, G. Chen, B. C. Ooi, K.-L. Tan, M. Zhang, *IEEE Trans. Knowl. Data Eng.* **2015**, 27, 1920.
- [3] L. Chua, *Semicond. Sci. Technol.* **2014**, 29, 104001.
- [4] J. J. Yang, D. B. Strukov, D. R. Stewart, *Nat. Nanotechnol.* **2013**, 8, 13.
- [5] S. Yu, *Proc. IEEE* **2018**, 106, 260.
- [6] M. Chi, in (Eds.: F. Gan, Z. Song), Changzhou, China, **2016**, p. 981801.
- [7] V. Garcia, M. Bibes, *Nat. Commun.* **2014**, 5, 4289.
- [8] M. Ye. Zhuravlev, R. F. Sabirianov, S. S. Jaswal, E. Y. Tsymbal, *Phys. Rev. Lett.* **2005**, 94, 246802.
- [9] C. Ma, Z. Luo, W. Huang, L. Zhao, Q. Chen, Y. Lin, X. Liu, Z. Chen, C. Liu, H. Sun, X. Jin, Y. Yin, X. Li, *Nat. Commun.* **2020**, 11, 1439.
- [10] P. Stoliar, H. Yamada, Y. Toyosaki, A. Sawa, *Sci. Rep.* **2019**, 9, 17740.
- [11] Y. Wei, P. Nukala, M. Salverda, S. Matzen, H. J. Zhao, J. Momand, A. S. Everhardt, G. Agnus, G. R. Blake, P. Lecoeur, B. J. Kooi, J. Íñiguez, B. Dkhil, B. Noheda, *Nat. Mater.* **2018**, 17, 1095.
- [12] C. H. Ahn, *Science* **1997**, 276, 1100.
- [13] T. S. Böske, J. Müller, D. Bräuhäus, U. Schröder, U. Böttger, *Appl. Phys. Lett.* **2011**, 99, 102903.

- [14] J. Müller, T. S. Böske, D. Bräuhäus, U. Schröder, U. Böttger, J. Sundqvist, P. Kücher, T. Mikolajick, L. Frey, *Appl. Phys. Lett.* **2011**, *99*, 112901.
- [15] M. Trentzsch, S. Flachowsky, R. Richter, J. Paul, B. Reimer, D. Utess, S. Jansen, H. Mulaosmanovic, S. Müller, S. Slesazeck, J. Ocker, M. Noack, J. Müller, P. Polakowski, J. Schreiter, S. Beyer, T. Mikolajick, B. Rice, in *2016 IEEE Int. Electron Devices Meet. IEDM*, **2016**, p. 11.5.1-11.5.4.
- [16] H. Mulaosmanovic, E. Chicca, M. Bertele, T. Mikolajick, S. Slesazeck, *Nanoscale* **2018**, *10*, 21755.
- [17] B. Max, M. Hoffmann, S. Slesazeck, T. Mikolajick, *IEEE J. Electron Devices Soc.* **2019**, *7*, 1175.
- [18] M. Halter, L. Bégon-Lours, V. Bragaglia, M. Sousa, B. J. Offrein, S. Abel, M. Luisier, J. Fompeyrine, *ACS Appl. Mater. Interfaces* **2020**, *12*, 17725.
- [19] M.-K. Kim, J.-S. Lee, *Nano Lett.* **2019**, *19*, 2044.
- [20] É. O'Connor, M. Halter, F. Eltes, M. Sousa, A. Kellock, S. Abel, J. Fompeyrine, *APL Mater.* **2018**, *6*, 121103.
- [21] Y. D. Lin, S. S. Sheu, T. H. Hou, W. C. Lo, M. H. Lee, M. F. Chang, Y. C. King, C. J. Lin, H. Y. Lee, Y. T. Tang, P. C. Yeh, H. Y. Yang, P. S. Yeh, C. Y. Wang, J. W. Su, S. H. Li, in *2019 IEEE Int. Electron Devices Meet. IEDM*, IEEE, San Francisco, CA, USA, **2019**, p. 15.3.1-15.3.4.
- [22] V. Mikheev, A. Chouprik, Y. Lebedinskii, S. Zarubin, A. M. Markeev, A. V. Zenkevich, D. Negrov, *Nanotechnology* **2020**, *31*, 215205.
- [23] J. Yoon, S. Hong, Y. W. Song, J.-H. Ahn, S.-E. Ahn, *Appl. Phys. Lett.* **2019**, *115*, 153502.
- [24] S. S. Cheema, D. Kwon, N. Shanker, R. dos Reis, S.-L. Hsu, J. Xiao, H. Zhang, R. Wagner, A. Datar, M. R. McCarter, C. R. Serrao, A. K. Yadav, G. Karbasian, C.-H. Hsu, A. J. Tan, L.-C. Wang, V. Thakare, X. Zhang, A. Mehta, E. Karapetrova, R. V.

- Chopdekar, P. Shafer, E. Arenholz, C. Hu, R. Proksch, R. Ramesh, J. Ciston, S. Salahuddin, *Nature* **2020**, 580, 478.
- [25] B. Max, M. Pešić, S. Slesazeck, T. Mikolajick, *J. Appl. Phys.* **2018**, 123, 134102.
- [26] A. Chouprik, S. Zakharchenko, M. Spiridonov, S. Zarubin, A. Chernikova, R. Kirtaev, P. Buragohain, A. Gruverman, A. Zenkevich, D. Negrov, *ACS Appl. Mater. Interfaces* **2018**, 10, 8818.
- [27] Q. Luo, Y. Cheng, J. Yang, R. Cao, H. Ma, Y. Yang, R. Huang, W. Wei, Y. Zheng, T. Gong, J. Yu, X. Xu, P. Yuan, X. Li, L. Tai, H. Yu, D. Shang, Q. Liu, B. Yu, Q. Ren, H. Lv, M. Liu, *Nat. Commun.* **2020**, 11, 1391.
- [28] T. Francois, C. Pellissier, S. Slesazeck, V. Havel, C. Richter, A. Makosiej, B. Giraud, E. T. Breyer, M. Materano, P. Chiquet, M. Bocquet, L. Grenouillet, E. Nowak, U. Schroeder, F. Gaillard, J. Coignus, P. Blaise, C. Carabasse, N. Vaxelaire, T. Magis, F. Aussenac, V. Loup, in *2019 IEEE Int. Electron Devices Meet. IEDM*, IEEE, San Francisco, CA, USA, **2019**, p. 15.7.1-15.7.4.
- [29] M. Hyuk Park, H. Joon Kim, Y. Jin Kim, T. Moon, C. Seong Hwang, *Appl. Phys. Lett.* **2014**, 104, 072901.
- [30] Y. Wei, S. Matzen, G. Agnus, M. Salverda, P. Nukala, T. Maroutian, Q. Chen, J. Ye, P. Lecoeur, B. Noheda, *Physical Review Applied* **12.3** **2019**, 031001.
- [31] A. Chernikova, M. Kozodaev, A. Markeev, D. Negrov, M. Spiridonov, S. Zarubin, O. Bak, P. Buragohain, H. Lu, E. Suvorova, A. Gruverman, A. Zenkevich, *ACS Appl. Mater. Interfaces* **2016**, 8, 7232.
- [32] A. Sawa, **2008**, 11, 9.
- [33] A. Gruverman, D. Wu, H. Lu, Y. Wang, H. W. Jang, C. M. Folkman, M. Ye. Zhuravlev, D. Felker, M. Rzechowski, C.-B. Eom, E. Y. Tsymbal, *Nano Lett.* **2009**, 9, 3539.
- [34] F.-C. Chiu, *Adv. Mater. Sci. Eng.* **2014**, 2014, 1.

- [35] M. C. Sulzbach, S. Estandía, X. Long, J. Lyu, N. Dix, J. Gàzquez, M. F. Chisholm, F. Sánchez, I. Fina, J. Fontcuberta, *Adv. Electron. Mater.* **2020**, *6*, 1900852.
- [36] H. Y. Yoong, H. Wu, J. Zhao, H. Wang, R. Guo, J. Xiao, B. Zhang, P. Yang, S. J. Pennycook, N. Deng, X. Yan, J. Chen, *Adv. Funct. Mater.* **2018**, *28*, 1806037.
- [37] S. Fujii, Y. Kamimuta, T. Ino, Y. Nakasaki, R. Takaishi, M. Saitoh, in *2016 IEEE Symp. VLSI Technol.*, IEEE, Honolulu, HI, USA, **2016**, pp. 1–2.
- [38] S. Starschich, S. Menzel, U. Böttger, *Appl. Phys. Lett.* **2016**, *108*, 032903.
- [39] C. Liu, F. Liu, Q. Luo, P. Huang, X. X. Xu, H. B. Lv, Y. D. Zhao, X. Y. Liu, J. F. Kang, in *2018 IEEE Int. Electron Devices Meet. IEDM*, IEEE, San Francisco, CA, **2018**, p. 16.4.1-16.4.4.
- [40] A. Chouprik, M. Spiridonov, S. Zarubin, R. Kirtaev, V. Mikheev, Y. Lebedinskii, S. Zakharchenko, D. Negrov, *ACS Appl. Electron. Mater.* **2019**, *1*, 275.
- [41] K. Ota, J. Deguchi, S. Fujii, M. Saitoh, M. Yamaguchi, R. Berdan, T. Marukame, Y. Nishi, K. Matsuo, K. Takahashi, Y. Kamiya, S. Miyano, in *2019 IEEE Int. Electron Devices Meet. IEDM*, IEEE, San Francisco, CA, USA, **2019**, p. 6.2.1-6.2.4.
- [42] K.-H. Kim, S. Gaba, D. Wheeler, J. M. Cruz-Albrecht, T. Hussain, N. Srinivasa, W. Lu, *Nano Lett.* **2012**, *12*, 389.
- [43] T. Choi, S. Lee, Y. J. Choi, V. Kiryukhin, S.-W. Cheong, *Science* **2009**, *324*, 63.
- [44] D. Davis, *Phys. Rev. B* **1973**, *7*, 129.
- [45] R. N. Blumenthal, J. Baukus, W. M. Hirthe, **n.d.**, 6.
- [46] S. Boyn, J. Grollier, G. Lecerf, B. Xu, N. Locatelli, S. Fusil, S. Girod, C. Carrétéro, K. Garcia, S. Xavier, J. Tomas, L. Bellaiche, M. Bibes, A. Barthélémy, S. Saïghi, V. Garcia, *Nat. Commun.* **2017**, *8*, 14736.
- [47] H. Yamada, V. Garcia, S. Fusil, S. Boyn, M. Marinova, A. Gloter, S. Xavier, J. Grollier, E. Jacquet, C. Carrétéro, C. Deranlot, M. Bibes, A. Barthélémy, *ACS Nano* **2013**, *7*, 5385.

Figure 1. GIXRD spectra of a TiN (10 nm)/HZO (4.5 nm)/TiO_x (3.5 nm)/TiN (20 nm)/SiO₂ (100 nm)//Si structure after ms-FLA. The HZO peak at 30,4 deg is fitted by a Gaussian, a crystallite size of 4 nm is estimated with the Scherrer model ($k=0.9$, $\text{CuK}\alpha_1 \lambda = 1.5406 \text{ nm}$).

Figure 2. Resistance of three pristine devices with a diameter of 80 μm measured at 100 mV, after applying a bias V_{write} and after a waiting time of ~ 10 seconds. The arrows indicate the chronological order. The bottom electrode (TiO_x layer) is grounded.

Figure 3. Dynamic Hysteresis Measurements (DHM) of an 80 μm diameter device during wake-up. Fatigue Frequency: 100 kHz. Amplitude: 2 V. Left axis, upper curves (thick lines): polarization. Right axis, lower curves (thin lines): measured currents. The different curves correspond to polarization and currents measured after a given number of cycles, indicated in the legend. Leakage current result in overestimation of the polarization.

Figure 4. Resistance of an 80 μm pristine capacitor (black curve) and woken-up (green curve), measured at 100 mV, after applying a bias V_{write} . The bottom electrode (TiO_x layer) is grounded.

Figure 5. PUND measurement of an 80 μm diameter device after wake-up: polarization versus voltage loop. In inset is the corresponding current. Frequency: 100 Hz; amplitude: 2 V; write pulse time: 5 ms, write pulse rise time: 25 ms.

Figure 6. scheme of the SET, LRS, RESET and HRS. The green layer and the white arrow represent the HZO layer and the ferroelectric polarization. The blue layer is the TiO_x *n*-type semiconducting layer represented in its accumulated state (white gradient) and depleted state (black gradient).

An analog resistive memory device is fabricated with a Back-End-Of-Line compatible process. Two TiN electrodes are separated by a ferroelectric, 4.5 nm thick HfZrO₄ (HZO) layer and a semiconducting TiO_x interlayer. Synaptic functionality is obtained, in the pristine state as well as after wake-up, and originates from the ferroelectric properties of the HZO layer.

Keyword Ferroelectric memristor

L. Bégon-Lours*, M. Halter, Y. Popoff, B. J. Offrein

Ferroelectric, Analog Resistive Switching in BEOL Compatible TiN/HfZrO₄/TiO_x Junctions

ToC figure

© Copyright 2020. WILEY-VCH GmbH.

Supporting Information

Ferroelectric, Analog Resistive Switching in BEOL Compatible TiN/HfZrO₄/TiO_x Junctions

Laura Bégon-Lours^{1}, Mattia Halter^{1,2}, Youri Popoff^{1,2} and Bert Jan Offrein¹*

Figure S1. XRR symmetric scan of a TiN (10 nm)/HZO (4.5 nm)/TiO_x (3.5 nm)/TiN (20 nm)/SiO₂ (100 nm)//Si structure after ms-FLA.

Figure S2: retention of three devices poled in the LRS, intermediate and HRS states.

Figure S3. Product of the area and the resistance of pristine devices measured at 100 mV, after applying a bias V_{write} . The arrows indicate the chronological order. The bottom electrode (TiO_x layer) is grounded.

Figure S4. I-V characteristics of an 80 μm diameter device in the pristine state (black) and after wake-up (green). The inset shows the I-V measurement between 0.01 and 0.1 V after polarizing the diode in the high (resp. low) resistive state, in the pristine state (light blue, resp. orange data points) and after wake-up (blue resp. red data points.). For comparison, the red, resp. blue, orange and light blue lines represent calculated direct tunnel current with a symmetric barrier height of 0.42, resp. 0.43, 0.47 and 0.48 eV and a thickness of 4.5 nm, with the Brinkman model [Reference: A. Gruverman, D. Wu, H. Lu, Y. Wang, H. W. Jang, C. M. Folkman, M. Ye. Zhuravlev, D. Felker, M. Rzechowski, C.-B. Eom, E. Y. Tsymbal, *Nano Lett.* **2009**, 9, 3539.]

Figure S6. Resistance of a device with a diameter of 40 μm , in a TiN/HZO/TiO_x/TiN//Si++ stack where the HZO layer is amorphous, measured at 100 mV, after applying a bias V_{write} .

The bottom electrode (TiO_x layer) is grounded. No resistive switching is observed.

Figure S7. Fatigue measurements on a 60 μm diameter junction. The device is cycled at 100 kHz. Each data point corresponds to a DHM measurement at 2 V and 5 kHz. Leakage current result in overestimation of the polarization.