Variability-aware Design of a Bandgap Voltage Reference with 0.18% Standard Deviation and 68 nW Power Consumption

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Abstract— **In this paper we present a design approach based on a reassessment of design priorities in order to obtain robust circuits with respect to process variability. We show that if we address variability as one of the main issues in circuit design, and make it inform our very first design choices, we are able to significantly reduce dispersion of circuit characteristics without degrading of the other performance figures. We apply this variability-aware approach to the design of a nanopower reference voltage generator in 0.18 μm CMOS technology. The result is a BJT-based topology, which provides a reference voltage of about 241 mV from a 1 V supply voltage. Measurements on 20 samples from a single batch show that the reference voltage exhibits a relative standard deviation of 0.18%, while consuming only 68.3 nW. This is comparable with the performance of references that are either trimmed or consume much more power. This reduced process sensitivity comes at the cost of a significant increase of die area (0.28 mm^2).**

Index Terms— **Bandgap reference voltage generator, variability-aware design, analog design, low power.**

I. INTRODUCTION

One of the main design challenges posed by CMOS technology scaling is coping with process variability. Indeed, it is apparent that new process innovations and improvements will not be sufficient to completely solve the variability challenge caused by scaling, and that the hurdles will be in large part transferred to circuit designers [1], [2]. This issue involves both digital and analog design, and translates in the fact that circuit performance is typically not able to take full advantage of the nominal improvements offered by aggressively scaled technologies.

Proposed approaches to tackle variability often involve complex feedback systems, based on monitoring circuits that assess process variability and actuation knobs which adjust transistor bias points [3]. In other cases, ad-hoc trimming procedures are envisaged ([4]-[6]). More recently, a method has been presented based on an "internal" compensation, which requires the designer to devise and exploit circuits using the combination of two quantities with reverse-correlated process variations [7]. This type of approach is able to provide a significant reduction of the relative standard deviation of the desired circuit performance figures (between few tenths and a factor 3) [7], [8]. To achieve stronger reduction, the circuit must have access to a reference quantity, such as a stable external resistor, or - to a lesser extent - mobility [9], [10].

Here we use a variability-aware approach [11], [12], so our first design choices are informed by the aim of achieving circuits with minimum process sensitivity. We show that such reordering of design priorities enables a large improvement of circuit precision without degrading other performance figures. In particular, we obtain a low process sensitivity together with a very low power consumption, with the main drawback of a sizeable increase in chip area. We use this approach in the design of the ubiquitous voltage reference in a 0.18 μm CMOS technology.

The reference voltage generator is an important building block for a wide range of analog and mixed signal circuits, such as A/D converters, DRAMs, flash memories, low dropout regulators and oscillators. It generates a voltage which has to be stable against process, temperature and line variations. A precise voltage reference with ultralow power consumption can be extremely useful especially in implantable systems or in passive and semi-passive transponders: it can be used as an inexpensive and low-power solution to provide a reference quantity in data converters, oscillators, and more complex circuits.

The "classical" architecture to obtain a voltage reference is the bipolar bandgap one, proposed by Widlar in [13]. A temperature-compensated reference voltage is obtained by adding to the base emitter voltage of Q1, V_{BE}, which has a negative temperature coefficient, a term RI_{PTAT} proportional to temperature. This architecture is also very useful in order to obtain a reference voltage with low process sensitivity (the typical relative standard deviation of the reference voltage is close to 1% [14], [15]). The main drawback is represented by the difficulty to use a low power supply voltage. Indeed, to achieve temperature compensation, V_{ref} must be close to $E_{gap}/q \sim 1.2$ V, where E_{gap} is the silicon gap and q is the elementary charge [13]. This however implies that the reference voltage is "anchored" to the silicon energy gap, which is hardly dependent on process, and therefore enables to achieve a reference voltage with very low process sensitivity.

However, modern low-power low-voltage circuits need reference voltages well below 1 V. Several techniques have been proposed in order to design sub-1 V CMOS bandgap references [16]. Among them, a remarkable one is based on the sum of two currents, instead of two voltages, with opposite temperature coefficients [17]. The drawback is a higher noise level due to the contribution of the current mirrors [18]. Another important technique is based on the reverse bandgap principle [18], which obtains the reference voltage as the sum of a PTAT voltage and a fraction of the bipolar transistor V_{BE} voltage.

In recent years, however, in order to meet the requirements of low power consumption and reduced area occupation, voltage reference generators have also been proposed [19]-[25] based on the use of only MOSFETs with standard CMOS process. These generators can have a very small power consumption (down to 2.2 pW in [25]), because MOSFETs can be biased in the subthreshold region, however they are intrinsically prone to large process variability, as in all cases the expression of the reference voltage contains as an addendum the MOSFET threshold voltage, which is subject to significant process variations.

If we accept as our priority a robust reference voltage with respect to process variability, the BJT-based bandgap topology is the most effective. Actually, the BJT-based topology continues to be very popular, also in standard CMOS technologies, and it allows to obtain good results also in terms of area occupation [15], [26], low supply voltage and low power consumption [26]. For example[26], which uses a reverse bandgap principle with a switch-capacitor voltage sampling scheme, obtains a low power consumption of less than 200 nW with a process sensitivity of the reference voltage still of the order of 1%. A better result has been obtained by [15] (σ=0.8%), but with a current consumption of 1.4 μA at 1.1 V.

We show in the following a BJT-based topology which couples low power consumption (smaller than 100 nW) with a record-low dispersion of the reference voltage (0.18%). The main drawback is a sizeable increase in area occupation.

The rest of the paper is organized as follows: in Section II we describe in more details the chosen topology and in Section III we analyze the major sources of variability for the reference voltage. We present the circuit design and experimental results in Section IV and V, respectively, and compare them to the relevant literature in Section VI. Finally, we present our Conclusion.

II. Circuit description

In order to operate with a low power consumption and a low power supply voltage, we consider the topology proposed by Banba [17], implemented in a standard CMOS process using substrate pnp transistors.

In Fig. 1 the bandgap core is shown, which provides the current proportional to temperature. Diode-connected transistors Md1-Md2 constitute a voltage divider which will be explained later. Let us call m

the current mirror ratio of M1-M2 ($I_1 = mI_2$, where I_1 and I_2 are the emitter currents of Q1 and Q2, respectively), and n the ratio of the emitter-base diode inverse saturation currents of Q2 and Q1, I_{s2} and I_{s1} ($I_{s2} = nI_{s1}$): for example, Q2 consists of n copies of transistor Q1 connected in parallel. Furthermore, we call α_1 the current mirror ratio of M2 and M3 ($I_{out1} = \alpha_1 I_2$) and $I = I_1 + I_2$. With these assumptions we can write:

$$\Delta V = R_1 I_2 = V_T \ln\left(\frac{I_1}{I_{s1}} \frac{I_{s2}}{I_2}\right) = V_T \ln(nm) = \frac{IR_1}{(m+1)} \qquad (1)$$

where ΔV is the voltage drop across R_1.
Furthermore:

$$I_{out1} = \alpha_1 \frac{V_T \ln(nm)}{R_1}. \qquad (2)$$

This current is proportional to the absolute temperature, as required.

The complete bandgap voltage generator is shown in Fig. 2. The second operational amplifier is used in order to impose on R_2 a fraction α of the base-emitter voltage of Q1, obtained from a voltage divider (Fig. 1), consisting of diode-connected pMOSFETs in series, each realized in a different well in order to suppress the body effect. The divider itself has a negligible power consumption and provides the advantage of reducing the voltage drop on - and the current through - R_2. The current in R_2 is mirrored to R_3 and added to I_{out1}. The reference voltage V_{ref} is:

$$V_{ref} = R_3\left(I_{out1} + \alpha_2 \frac{V_{be1}}{\alpha R_2}\right) = R_3\left(\alpha_1 \frac{V_T \ln(nm)}{R_1} + \alpha_2 \frac{V_{be1}}{\alpha R_2}\right), \qquad (3)$$

where α_2 is the current mirror ratio of M5 and M4 ($I_5 = \alpha_2 I_4$). We note from (3) that we can minimize temperature sensitivity by properly choosing the coefficients of the two terms.

III. Variability Sources Analysis

A. V_{BE} variation

The process sensitivity of the reference voltage (in terms of inter-die and inter-batch variability) mainly arises from the second term in (3), in which the base-emitter voltage of Q1 appears. We can highlight some design parameters connected to process sensitivity of V_{BE1}, which reads:

$$V_{BE1} = V_T \ln\left(\frac{I_1}{I_{s1}}\right) = V_T \ln\left(\frac{mV_T \ln(nm)}{R_1 I_{s1}}\right) \qquad (4)$$

where

$$I_{s1} = \frac{qA}{Q_b}\left(N_C N_V e^{-\frac{E_g}{KT}}\right)V_T \mu_h \qquad (5)$$

In this expression N_C (N_V) is the effective density of states of silicon conduction (valence) band, and is proportional to $T^{3/2}$ [27] through a constant K_1 (K_2). In addition, A is the junction area, Q_b is the base charge for area unit, μ_h is the carrier mobility [27].

Substituting (5) into (4) we have:

$$V_{BE1} = \frac{E_g}{q} - V_T \ln\left(\frac{R_1 A K_1 K_2 T^3 KT \mu_h}{mV_T \ln(nm)Q_b}\right) = \frac{E_g}{q} + V_T \ln\left(\frac{IQ_B \delta}{KT\mu_h A K_1 K_2 T^3}\right) \qquad (6)$$

where $\delta = m/(m+1)$. In order to reduce the process sensitivity of V_{BE1} it is important to reduce the weight of the second term in (6). This requires large n, large m and small A and R_1. From this expression we can also highlight the expected trade-off between the bandgap core current consumption I and the process sensitivity of V_{BE1}.

B. Resistor variations

In (3) only resistance ratios appear explicitly, and it can be made very precise with a proper layout. However, also V_{BE1} depends on R_1, as can be seen in (6), and this introduce a source of variability in terms of inter-die and inter-batch variations (which produces correlated variations between resistor parameters). In order to mitigate the latter issue, we propose a method which is based on the fact that the relative process sensitivity of poly resistance increases in a predictable way with decreasing resistor width W. For example, Fig. 3 shows the relative process variation of the high-resistivity non-silicide poly resistors in the UMC 0.18 μm process as a function of their width W, considering the maximum resistors variation as predicted by corner analysis. We can note that this relative variation rapidly increases if W is reduced below 2 μm. This property can be successfully used in order to reduce the effect of resistor process sensitivity on the reference voltage. Indeed, we can write the second term of reference voltage expression in (3) as $V'=V(R_1)R_3/R_2$, where V is a function of R_1, resistance R_i (i=1, 2, 3) is a function r of its width W_i, i.e. $R_i=r(W_i)$, and $\partial R_i/R_i=g(W_i)$. We can express the relative variation of V' ($\partial V'/V'$) as:

$$\frac{\partial V'}{V'} = \frac{\partial V}{V} + \frac{\partial R_3}{R_3} - \frac{\partial R_2}{R_2} = \frac{\partial V(R_1)}{\partial R_1}\frac{1}{V(R_1)}g(W_1)R_1 + g(W_3) - g(W_2) \tag{7}$$

From this expression, we can note that by properly choosing resistor widths we can reduce the process sensitivity of V_{ref} in (3). The effectiveness of this method is based on the hypothesis that uncorrelated variations of resistor geometries are negligible with respect to the correlated ones.

In summary, since the two terms of (3) contain the resistance ratio as a multiplying factor, by properly selecting resistor widths we can adjust the process sensitivity of resistance ratios as to compensate the process sensitivity of other resistance-dependent terms (in this case V_{BE1}).

C. Mismatch analysis

In this subsection we consider the impact of main mismatch sources on the dispersion of the reference voltage. In particular, we will consider:
-   the input offset voltage of the two operational amplifiers;
-   the mismatch in current mirrors;
-   the mismatch in bipolar transistors.

In Section IV we also consider the impact of mismatch in the voltage divider MOSFETs.

Input Offset Voltage of the Operational Amplifier

The two operational amplifiers have a single stage, as shown in Fig. 4, and MOSFETs are biased in subthreshold in order to reduce the total power consumption. The input offset voltage mainly depends on the mismatch of MOSFET threshold voltages. Since the input offset voltage of the core operational amplifier directly adds to the voltage drop across R_1, it is important to reduce the standard deviation of threshold voltage mismatch with the use of large size MOSFETs. Furthermore, considering (1), the voltage drop across R_1 can be increased (until the desired error in the reference voltage due to the operational amplifier offset voltage is obtained, for example 0.5%) by increasing n and R_1 and by decreasing m. This also allows to obtain a good trade-off between process sensitivity of the reference voltage and core power consumption.

The offset voltage of the second operational amplifier is directly added to V_{BE1}/α, so - through coefficient $\alpha_2 R_3/R_2$ - it adds to the dispersion of the reference voltage. Also for this operational amplifier we can reduce the entity of offset with the use of large size MOSFETs.

Mismatch in current mirrors

We consider the current mirror M1-M2 (Fig. 1), with source resistors R' and R'', and assume a mismatch ΔI between the two currents I_1 and I_2 ($I_2 = \frac{I_1}{m} + \Delta I$), with $R'' = mR'$. We consider the M1 parameters as the nominal ones and the M2 parameters as affected by a variation due to mismatch: $\beta_2 = \frac{\beta_1}{m} + \Delta\beta$ and $V_{th2} = V_{th1} + \Delta V_{th}$.

Starting from:

$$R' I_1 + V_{GS1} = R'' I_2 + V_{GS2}, \qquad (8)$$

we obtain, at the first order:

$$\Delta I = \frac{-\Delta V_{th} + \eta V_T \ln\left(1 + \frac{m\Delta\beta}{\beta}\right)}{\left(mR' + \frac{m\eta V_T}{I_1}\right)} \qquad (9)$$

From this expression we can note the importance of the insertion of the source resistors in order to reduce ΔI. The ratio of the two currents can be expressed as:

$$\frac{I_2}{I_1} = \frac{\beta_2}{\beta_1} \exp\left(\frac{-mR'\Delta I - \Delta V_{th}}{\eta V_T}\right). \qquad (10)$$

Similar considerations can be made for the other current mirror (M4-M5 of Fig. 2) and enable to dimension MOSFET areas and source resistors to achieve desired mismatch in current mirror.

Mismatch in bipolar transistors

The effect of mismatch between Q1 and Q2 can be important, especially by considering the large value of n and hence the very different current densities for transistor Q1 and each of the individual transistors in Q2. This could imply a difference in their inverse saturation current value and temperature and/or process dependence. The accurate model provided by the design kit allows us to evaluate these effects by means of corners analysis and Monte Carlo simulations.

All these relations and considerations support our choice of the design parameters and enable us to assess the effect of mismatch sources on the reference voltage.

IV. CIRCUIT DESIGN

The design of the proposed reference voltage generator in a UMC 0.18μm CMOS process is based on the above discussion. In particular, we obtain a very good trade-off between power consumption and process sensitivity of the reference voltage. Obviously the choice of the design parameters not involved in this trade-off (as for example the current mirror ratios α_1 and α_2) has been done in order to obtain a low temperature sensitivity of the reference voltage.

We reduced the process sensitivity of V_{BE1} mainly with the use of pnp transistors with the minimum emitter area provided by the design kit. Their area (5 μm x 5 μm) is not the minimum area achievable on the basis of layout rules, but for transistors with a very small emitter area, due to three-dimensional edge effects, the current component proportional to the perimeter becomes predominant, limiting the advantages achievable with area reduction.

We estimate a standard deviation of the input offset voltage of the operational amplifier V_{OScore} of 0.72 mV using a single stage with M11-M22 width W=60 μm, length L=50 μm and M33-M44 W=10 μm,

L=50 μm.

On the basis of (1), in order to increase ΔV to make it insensitive to V_{OScore} without a large increase of the total current drawn from the power supply, it is important to have a small m (we choose m=3), large n (we choose n=50), and a large R_1 (R_1=20.94 MΩ). With this choice we obtain a ΔV=134.5 mV with a core current consumption of 26.16 nA. The main price to pay for this choice is the obvious large increase of the total area occupation due to large resistors and large n.

We also choose α_1=1, α=2, α_2=1/3, R_2=16.31 MΩ, R_3=19.5 MΩ, obtaining V_{BE1}/α =286.6 mV. The effect of the offset voltage on the reference voltage (in terms of relative standard deviation) has been assessed in 0.21% for the core operational amplifier and 0.12% for the second one.

The current mirrors have been realized with pMOS of width larger than 100 μm and length of 50 μm, and with source resistance R'=2 MΩ and R_4=4 MΩ. This gives I_1=19.7 nA and I_4=17.6 nA. With this choice we obtain a relative variation of the reference voltage (σ/μ) of 0.12% due to the core current mirror mismatch, and of 0.08% due to the other current mirror (composed by M4-M5). The main drawback of the use of large source resistors is the large area occupation, but they are very effective in the reduction of the mismatch impact on the reference voltage: without these resistors, the effect of core current mirror mismatch on the reference voltage is 0.33% (M1-M2) and 0.32% (M4-M5).

We consider the divider composed by two diode-connected pMOSFETs in series with short-circuited source and well (see Fig. 1). We consider $V_{thd2} = V_{thd1} + \Delta V_{thd}$ (so we neglect the difference in the beta value of the two nominally identical MOSFETs and we consider only a difference in the threshold voltage with respect to the one of Md1). We can express the V_{BE1}/α voltage as:

$$\frac{V_{BE1}}{\alpha} = \frac{1}{2}V_{BE1} - \frac{1}{2}\Delta V_{thd} \qquad (11)$$

The mismatch in the voltage divider has been assessed in a negligible 0.09% relative variation of the reference voltage.

The effect of process variation of bipolar transistors and resistors on the reference voltage is respectively 0.25% and 0.19%, as obtained from Monte Carlo analysis.

Start up circuitry is not used because we verify with simulation that the circuit has no stability or start up problems. This is also verified by experimental results. The start up time is of a few hundred ms, due to the presence of high impedance nodes in the circuit. Table I summarizes circuit component values.

V. Experimental results

Two versions of the described circuit were manufactured, the one described in the previous sections (final version, 1 run) and a preliminary version (2 runs), for a total of three runs. The preliminary version differs from the described circuit in some minor details (it has, for example, n=200 and hence a slightly larger area) and has broadly similar performances.

All the results of this section are referred to the final version. However, since two batches from the preliminary version are available, and can provide usefully information about inter-batch variability, they will be discussed at the end of the section, where statistic data is exposed.

The chip layout of the final version is shown in Fig. 5: chip photo is not shown because dies are passivated with dummy layers which prevent us to see the circuit geometry. We can note the large area occupation (~0.28 mm^2) due to large resistors and the large number of BJTs in parallel.

Measurements were performed on 20 packaged samples with the use of an Agilent E3631A DC Power Supply and an HP3478A digital multimeter. The input impedance of this multimeter, in the considered voltage range, is larger than 10 GΩ, and therefore much larger than the output resistance of the voltage generator (~20 MΩ).

The average reference voltage is 240.9 mV (with respect to the 241.7 mV predicted by simulations), with a nominal supply voltage of 1 V at room temperature (27 °C). In these nominal conditions the current consumption is 68.34 nA.

Figs. 6(a)-(b) show that the circuit properly operates for a supply voltage between 0.8 V and 1.4 V, with a mean line sensitivity of 0.12 %/V at room temperature.

Fig. 6(c) shows the reference voltage as a function of supply voltage at different temperatures. The temperature sensitivity of the reference voltage is 97.7 ppm/°C from -25 °C to 80 °C, with the nominal supply voltage of 1 V. This result has been obtained with a simple first-order temperature compensation, and second order effects, especially related to V_{BE} voltage, are not compensated.

The PSRR of the proposed generator, which has been measured with the SR785 Dynamic Signal Analyzer, is of -68 dB at 100 Hz and it is lower than -50 dB at frequencies up to 100 kHz. At higher frequencies, also the pad and the input instrument capacitance contribute to maintain a low PSRR.

Current consumption at room temperature, which has a nominal value of 68.34 nA when the power supply voltage is 1 V, varies between 54.5 nA for a line voltage of 0.8 V, and 155.4 nA for a line voltage of 1.4 V, as shown in Fig. 6(d).

From 1 Hz to 100 kHz, the noise power spectrum is flat and close to $2\mu V/\sqrt{Hz}$.

Since our work is focused on the reduction of process variability, we show extensive statistical analysis of experiments on a single batch and compare them with results from Monte Carlo simulation to assess inter-batch variability. Fig. 7 shows some distributions on the basis of measurements performed on the samples: (a) reference voltage in nominal conditions (a power supply voltage of 1 V at 25 °C), (b) current consumption in nominal conditions, (c) line and (d) temperature sensitivities. The maximum measured reference voltage variation is 0.67%, while the relative standard deviation is 0.18%. The total power consumption of the proposed bandgap has a relative standard deviation of 1.6%.

We have already discussed the intrinsic robustness to process variability of our design: Monte Carlo simulations considering MOSFETs, BJTs and resistors parameters show a reference voltage process sensitivity (in terms of σ/μ) of only 0.48%. As we can see from Fig. 8, the relative standard deviation of the reference voltage is very good also for power supply voltages and temperatures far from the nominal values. In particular, $\sigma/\mu = 0.17\%$ when the line voltage is 0.8 V at room temperature and $\sigma/\mu = 0.19\%$ when the line voltage is 1.4 V at room temperature. With the nominal line voltage (1 V), the σ/μ of the reference voltage value is 0.18% at -25 °C and 0.19% at 80 °C.

Finally, we provide information on inter-batch variability by considering data from the two batches of the preliminary version. The distribution of the reference voltage in the two batches is illustrated in Fig. 9: The relative standard deviation of the reference voltage is of 0.13% for the first batch, 0.19% for the second, and 0.35% in total.

VI.   COMPARISON WITH THE LITERATURE

Table II compares performance figures of the proposed bandgap with those of voltage generators presented in the literature with a power consumption smaller than 1 μW, which can be useful for ultra-low-power applications. Refs [26] and [28] are based on the bipolar bandgap architecture, while the other designs are based on subthreshold MOSFETs. Our solution exhibits - by far - the lowest relative standard deviation of the reference voltage, even if it was obtained considering only one batch.

However, as already said, both Monte Carlo simulations and measurements on two batches on a previous version, based on the same principle, show very low dispersion even considering inter-batch variations. This is because we eliminated in the initial design phase any reliance on quantities - such as V_{th} - too sensitive to process variations.

BJT-based voltage references exhibit a power consumption comparable to our solution, but a higher process sensitivity, which for [28] is due to the use of MOSFET source-coupled pairs. Among the MOSFET-based generators, Ref [25] shows an extremely low power consumption with a very small area occupation. This reference voltage relies on the V_{th} difference of two different MOSFETs (thick oxide and native), and if we can assume some correlation between these threshold voltages, the impact of V_{th} process variability on the reference voltage is reduced with respect to a standard MOSFETs based solution. Results of [25] can be furtherly improved with digital trimming.

The choice of a circuit solution intrinsically less sensitive to process variability allowed us to obtain a manifold suppression of the relative standard deviation. It is more effective than both "internal" process compensation, which provides limited improvement since variability makes cancellation less effective, and "explicit" compensation due to feedback loops, which typically implies larger power consumption [33]. It is also an effective alternative to trimming if we consider applications, such as passive transponders and implantable applications, where trimming can be too costly.

In the literature, there is an example [18] of a BiCMOS reference voltage generator with a relative standard deviation of 0.19%, but with an extremely large current consumption of 20 µA and with comparable area occupation with respect to our solution. Ref. [32] proposes a generator which, by using DTMOSTs, obtains a relative variation of the reference voltage of 0.3% with a power consumption of 2.5 µA. However, this generator is based on a voltage-sum bandgap topology (the reference voltage value is 1.23 V), so it is not suitable for low power and low voltage applications.

Table II also shows the total reference voltage variation considering the contribution of all three variation mechanisms acting simultaneously: process variation, temperature variation (assuming $\Delta T = 20°C$), and supply voltage variation (assuming $\Delta V = 0.5V$). This analysis shows that the contribution of process variation dominates, followed by temperature-induced variations, while the contribution of supply voltage variations is usually much smaller.

It is also useful to compare our solution with voltage references using digitally controlled trimming (Table III). We can note that the standard deviation of V_{ref} in our proposed solution is comparable to that of Refs that have much higher power consumption ([4], [11], [26], [33]) and in one case [4] even larger area occupation. Only [25] obtains a similar process sensitivity of V_{ref} with a much smaller power consumption and area occupation, but this solution is useful if a digital section is easy to implement.

In Fig. 10, for all generators presented in Table II and Table III, we show a scatter plot in which we put on the y axis the cumulative relative variation $\Delta V_{tot}/V_{ref}$, where ΔV_{tot} is the sum of 3 standard deviations due to process variability and the variation generated by a temperature change of 60°C. The x axis is the product of area occupation and power consumption of the voltage generators.

The generators of Table II (no trimming) are represented in pink color, while the ones of Table III (digital trimming) are in blue color; the proposed one is in red. We note that the proposed solution is in a middle position between the graph portions occupied by solutions respectively with and without trimming. It is important to underline that trimming can help us in achieving a stable reference voltage without excessive cost if a digital section is already available in the complete chip and if the trimming procedure does not increase cost too much. The proposed solution is a strong alternative, especially for systems with a very simple digital section (implantable systems, sensor interfaces), for which the implementation of a trimming procedure would be really expensive and not easy.

VII. CONCLUSION

We maintain that a variability-aware approach to circuit design, in which the requirements of low sensitivity to process variations are considered starting from the first design choices, can allow a strong reduction of the statistical dispersion of circuit output quantities, without a significant worsening of other performance parameters. We have demonstrated the effectiveness of such approach in the design of a nanopower reference voltage generator with record-low dispersion due to process variability and with a low power consumption. We have shown that a BJT-based bandgap topology is the most appropriate to the first aim, since the reference voltage is anchored to a silicon physical property such as the energy bandgap, and does not rely on quantities sensitive to process variability as the threshold voltage.

We have derived design criteria that enabled us to obtain low power consumption of 68.3 nW and low relative standard deviation of the reference voltage of 0.18%, which is much smaller than all designs presented in the literature with sub-microwatt power consumption.

The main cost of our choices in the design space is a much higher area occupation, mainly due to the large resistances, needed to reduce the power consumption of the circuit, and the large n. Such cost is particularly acceptable in the case that most interests us, i.e. when one uses aggressively scaled CMOS technologies, which provide abundant margins in terms of die area.

A precise reference voltage generator such as the one proposed here, can be effectively used as a basic building block to provide robustness with respect to process variability to more complex circuits and systems, where one prefers not to use alternative reference circuits (such as quartz oscillators, for example) or expensive trimming procedures.

VIII. ACKNOWLEDGMENT

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TABLE II
COMPARISON BETWEEN THE PROPOSED VOLTAGE GENERATOR AND RESULTS FROM LITERATURE

	This work	[26] BJT	[28] BJT	[20]	[21]	[24]	[25]	[29]	[30]
Tecn. (μm CMOS)	0.18	0.13	0.35	0.35	0.35	0.18	0.13	0.18	0.18
V_{ref} (mV)	240.9	256	553	745	670	263.5	176	275.4	714
V_{dd} (V)	0.8÷1.4	0.75	1.1÷3.3	1.4÷3	0.9÷4	0.45÷1.8	0.5÷3	0.45	0.9
Power or I_{dd}	68 nA	170 nW	110nW	300 nW	40÷55 nA	7÷8 nA	4.4÷81 pA	40 pW	70 nW
V_{dd} sens. (%/V)	0.12	0.005	0.11	0.002	0.27	0.44	0.033	0.46	0.1
Temp. Sens. (ppm/°C) (°C)	97.7 (-25 ÷ 80)	40 (-20 ÷ 85)	394 (-20 ÷ 80)	15 (-20 ÷ 80)	10 (0 ÷ 80)	142 (0 ÷ 125)	62 (-20÷ 80)	105.4	58
Process. sens. Single batch (σ/μ)	0.18% (meas.) 0.48% (MC)	1%	1.63%	0.87%	3.1%	n/a	0.57%-0.85%	0.62%	2.3%
Process. sens. Multi batch (σ/μ)	0.35% (two batches, meas.)	n/a	n/a	n/a	n/a	3.9% (three batches)	0.72% (cumulative on two batches)	n/a	n/a
Total voltage variation (ΔV=0.5V; (ΔT=20°C; process)	0.44%	1.08%	2.47%	0.9%	3.26%	n/a	0.71%	1.06%	2.47%
Area (mm^2)	0.28	0.07	0.22	0.055	0.045	0.043	0.00135	0.018	0.057

TABLE III
COMPARISON BETWEEN THE PROPOSED VOLTAGE GENERATOR AND LITERATURE REFERENCES USING TRIMMING

	This work	[11]	[4]	[33]	[26]	[25]
Tecn.	0.18 um	0.16 um	0.35 um	0.6 um	130 nm	0.13 um
V_{ref} (V)	0.2409	1.0875	0.858	1.14205	0.256	0.1761
V_{dd} (V)	0.8÷1.4	1.8	1.4	2	>0.75	0.5÷3
Power/ Current	68.34 nW	55 µA	162 µW	23 µA	170 nW	59 pA
TC (ppm/°C) (°C)	97.7 (-25÷80)	5÷12 (-40÷125)	12.4 (-20÷100)	5.3 (0÷100)	40 (-20÷85)	5.3÷47.4 (-20÷80)
Process (σ/µ)	0.18%	0.05%	0.3%	0.08%	0.17%	0.16%
Area (mm^2)	0.28	0.12	1.2	0.057	0.07	0.0093
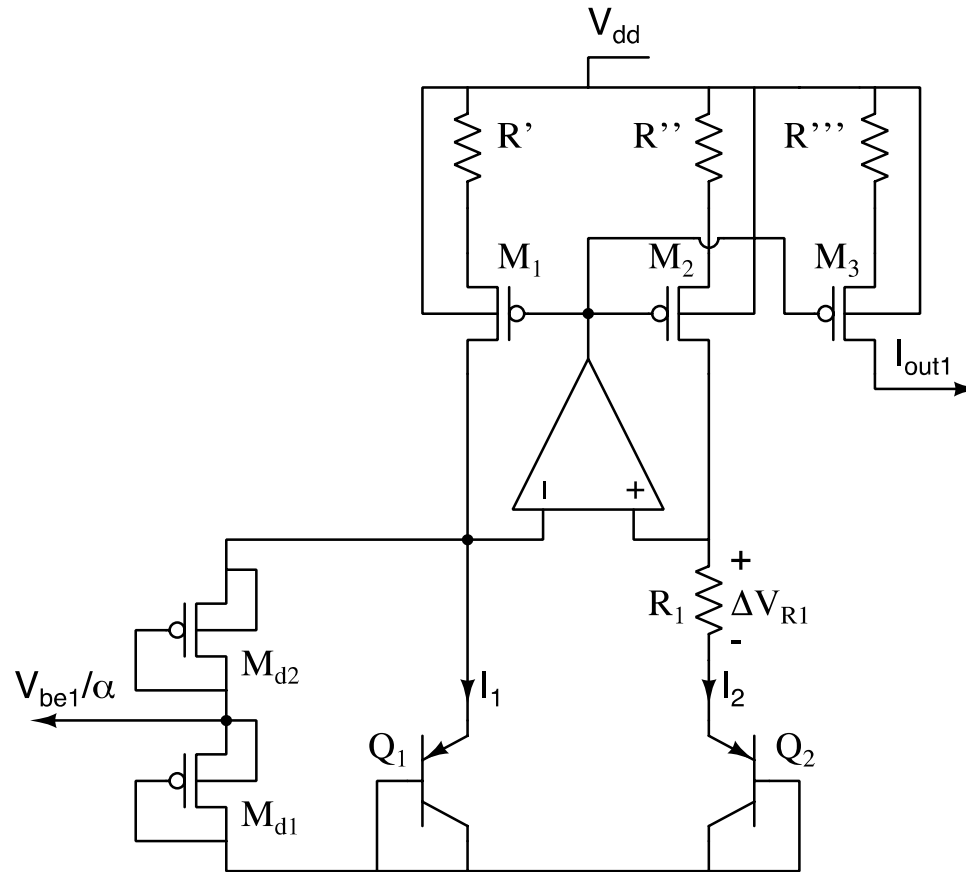
Figure 1. Proposed bandgap core
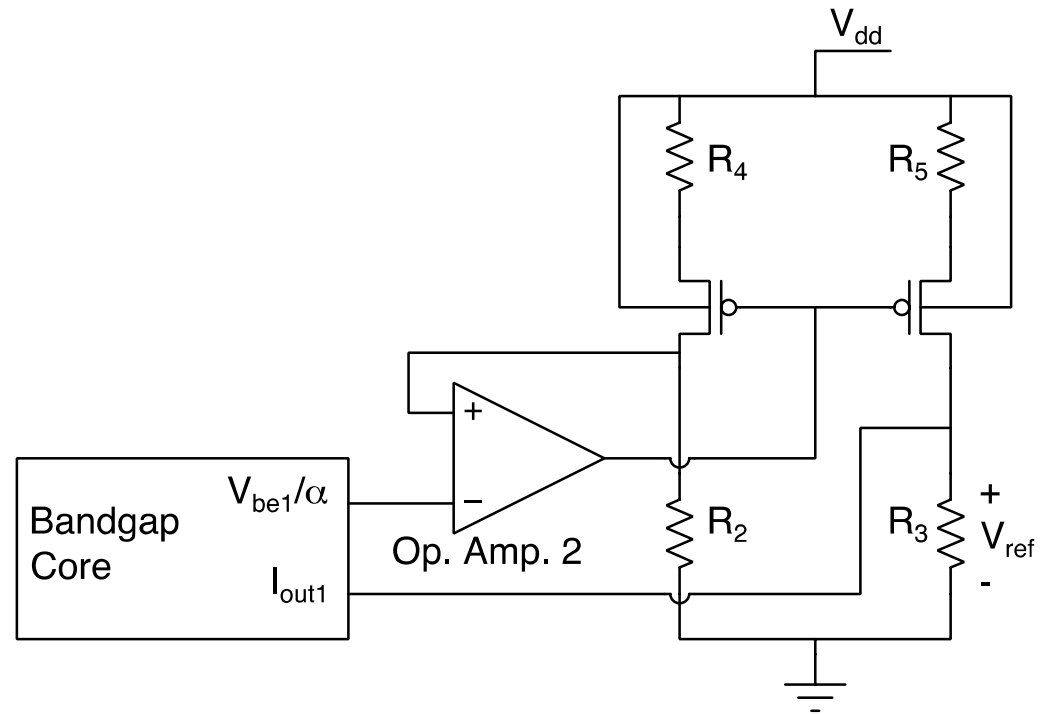
Fig. 2. Bandgap reference voltage generator
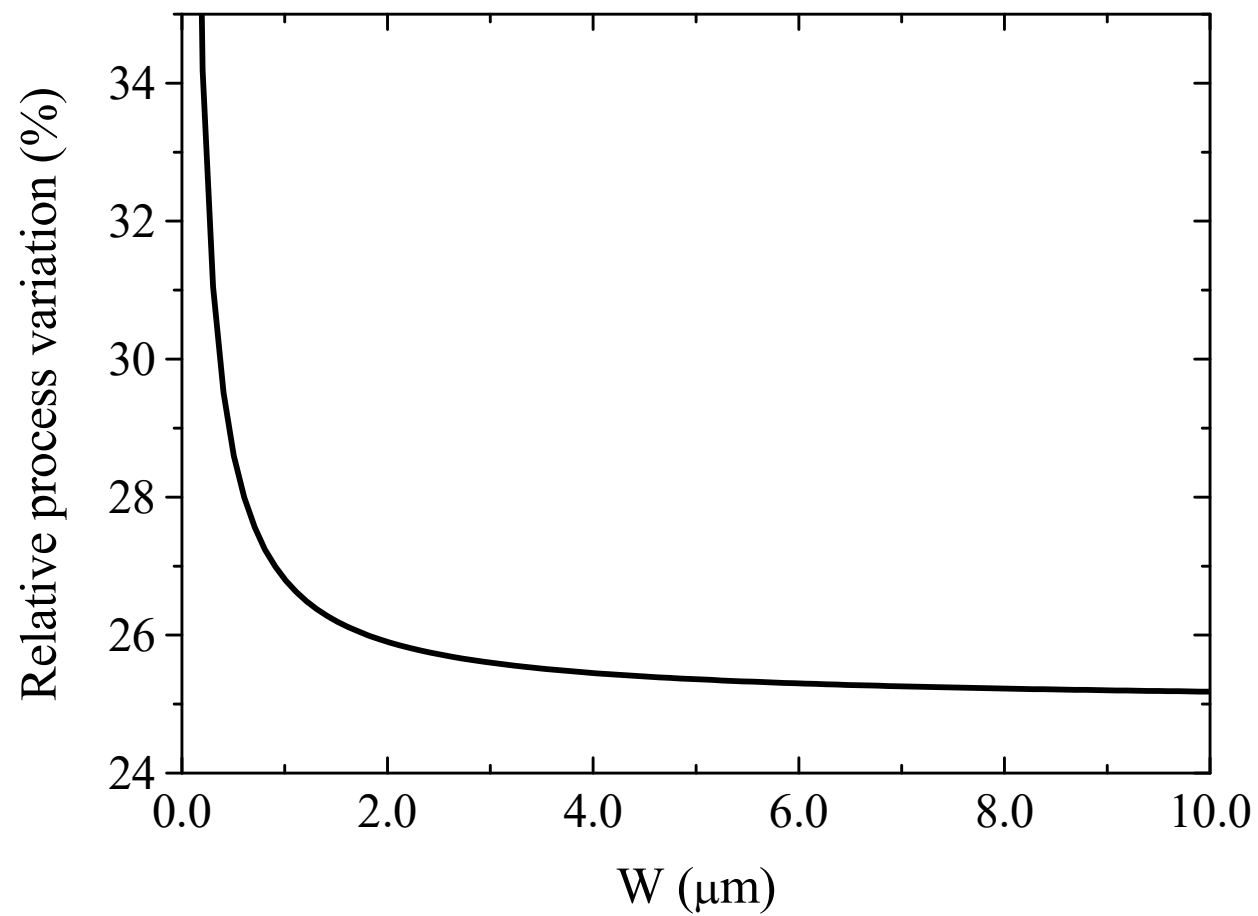
Fig. 3: Relative process variation of resistors as a function of their width *W*
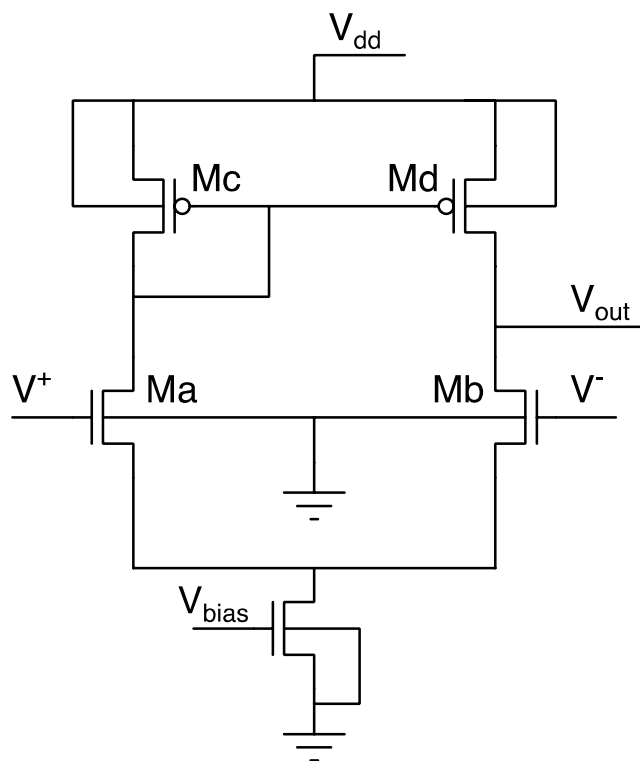
Fig. 4: Single stage operational amplifier
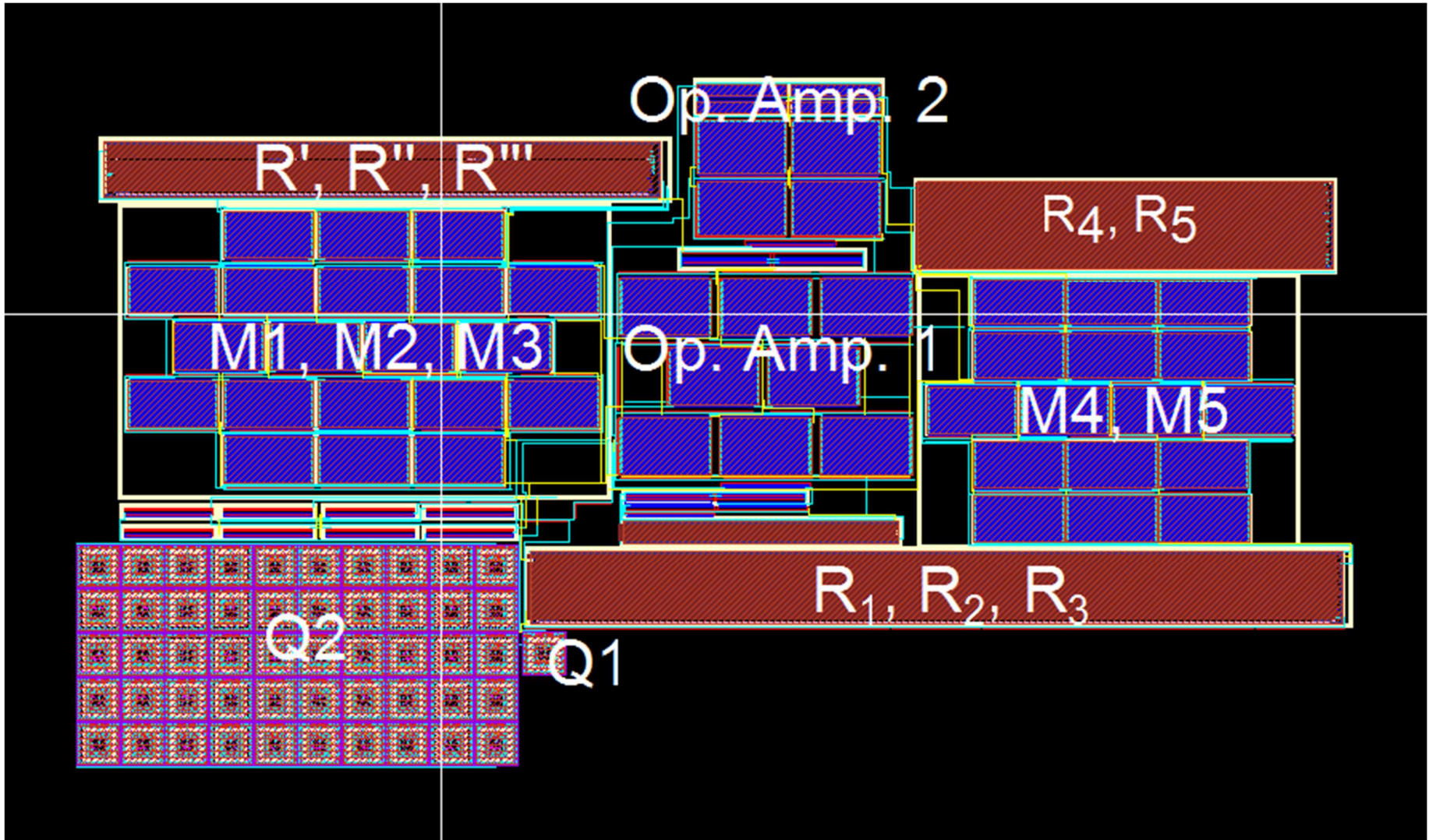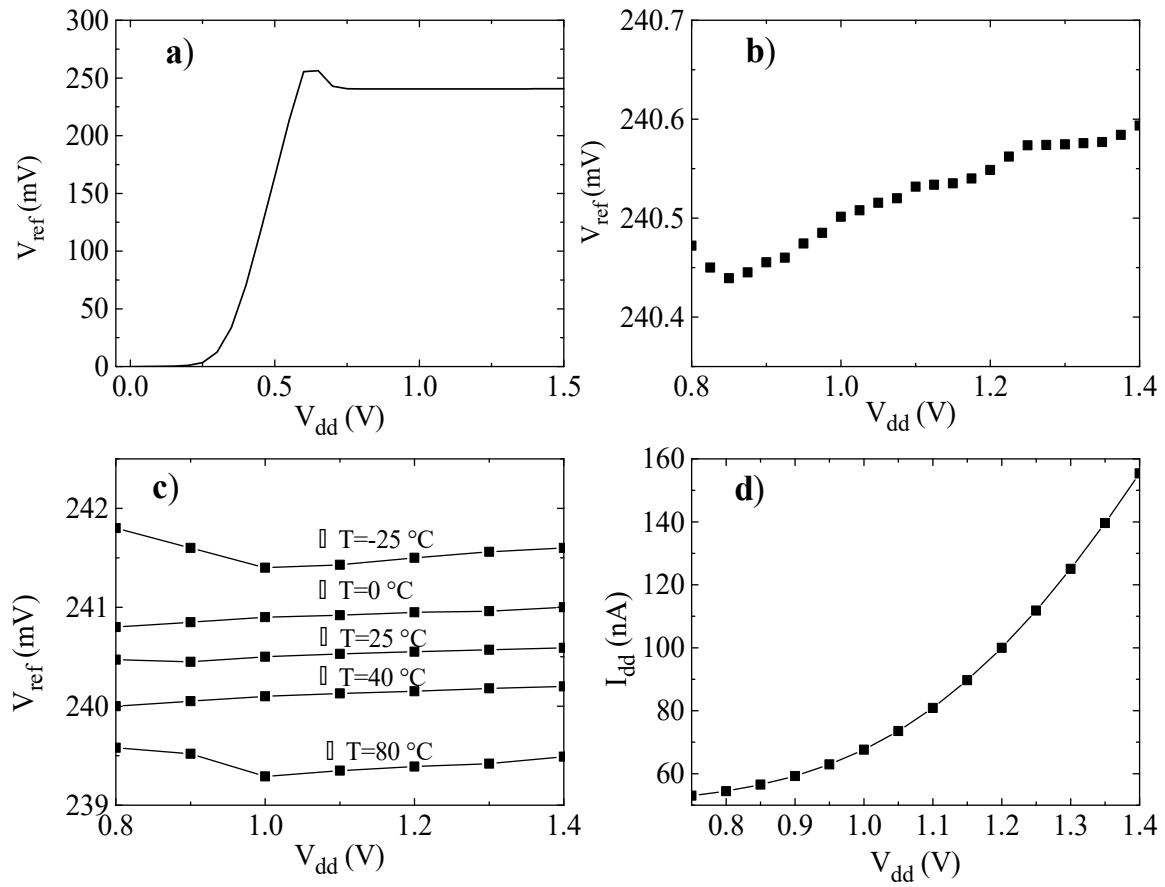
Fig. 5. Chip layout (700 μm x 400 μm)

Fig. 6. a) and b) Reference voltage as a function of supply voltage. c) Reference voltage as a function of supply voltage for five different temperatures. d) Circuit current consumption as a function of supply voltage.
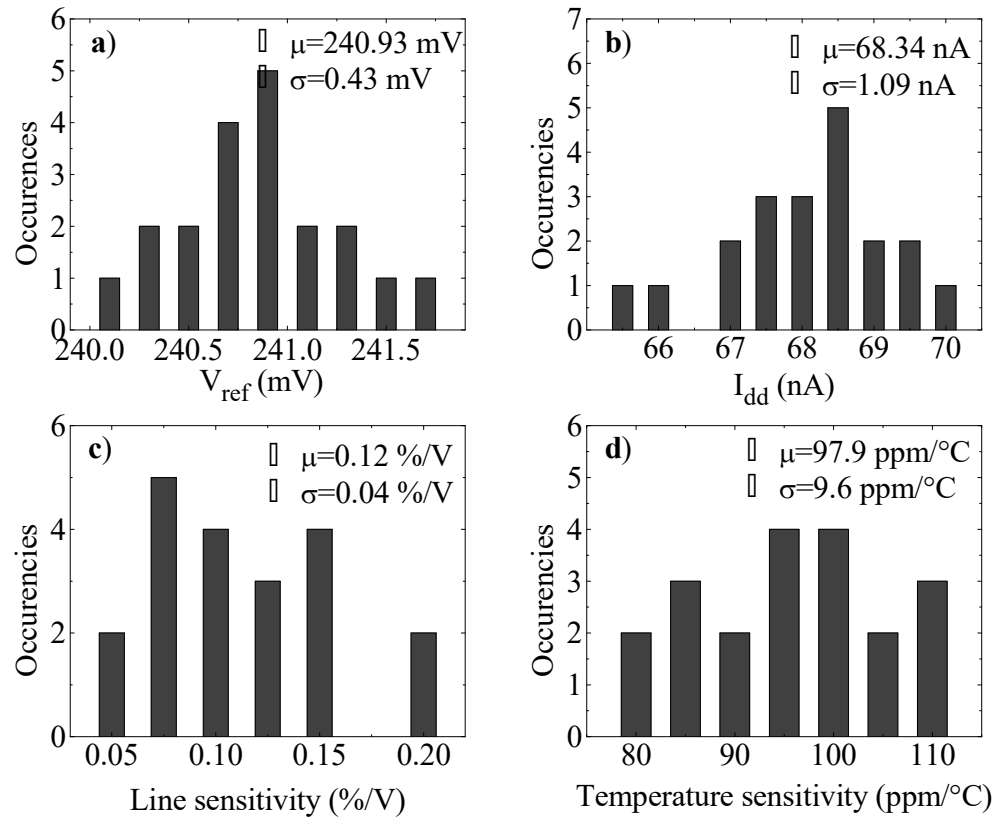
Fig. 7. Distribution over 20 samples at nominal conditions (V_{dd}=1 V, T=25 °C) of: a) Reference voltage. b) Supply current. c) Line sensitivity of the reference voltage. d) Temperature sensitivity of the reference voltage in the interval -25 °C ÷ 80 °C.
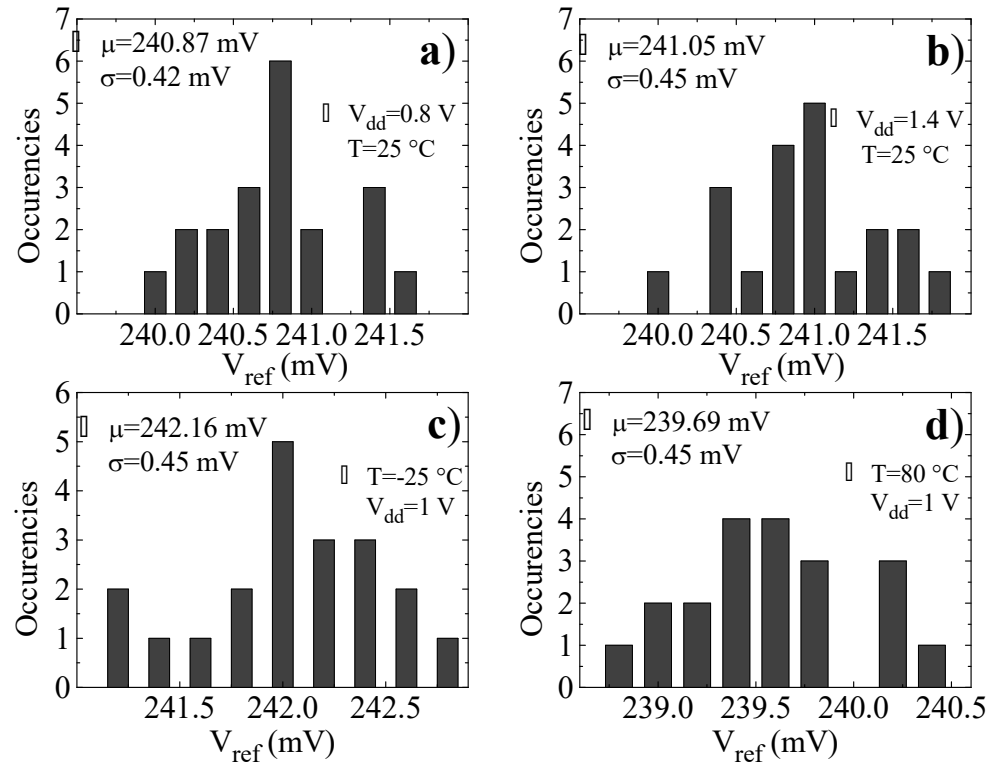
Fig. 8. Distribution of the reference voltage over 20 samples: a) At V_{dd}=0.8 V, T=25 °C. b) At V_{dd}=1.4 V, T=25 °C. c) At T=-25 °C, V_{dd}=1 V. d) at T=80 °C, V_{dd}=1 V.
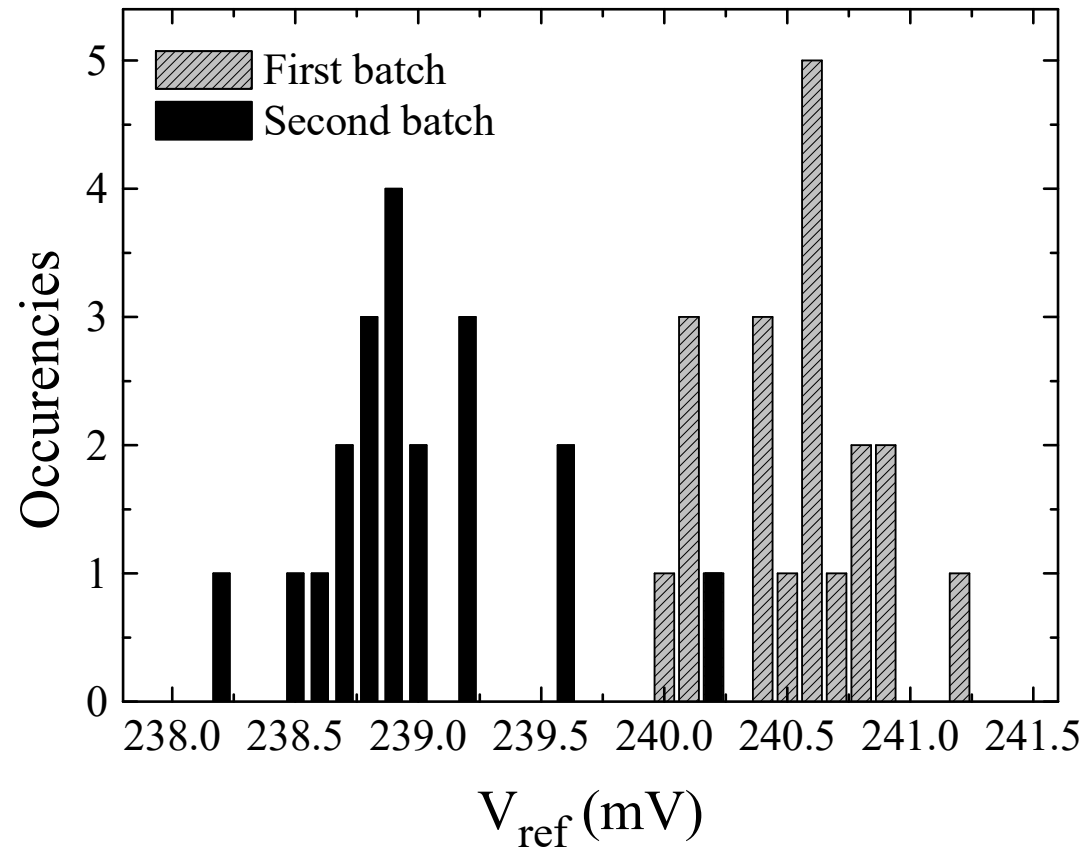
Fig. 9. Distribution over 40 samples from two batches of the reference voltage value in nominal conditions.
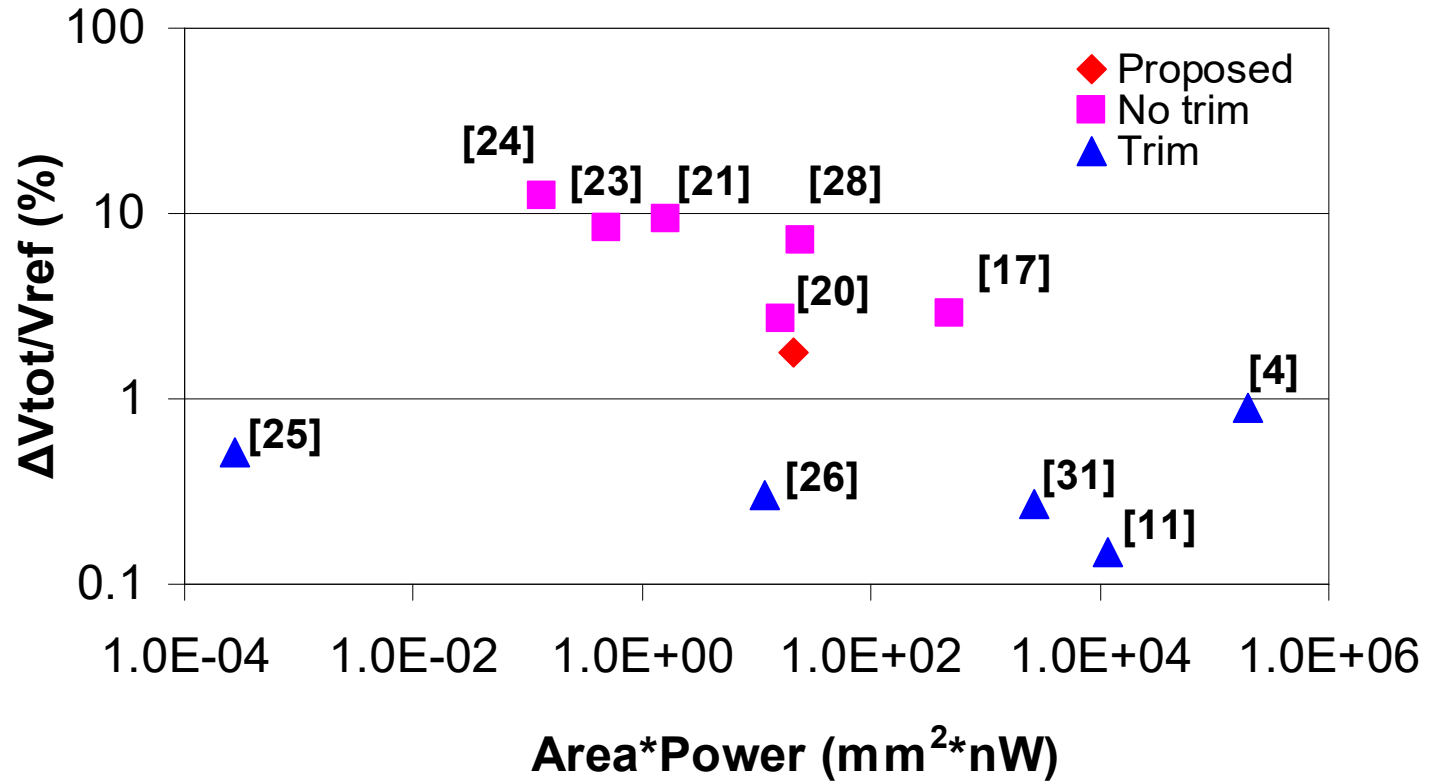
Fig. 10. Reference voltage variation as a function of the product area*power consumption for the generators of Table I (pink ones) and Table II (blue ones) with respect to the proposed one (red one).