Reliability aspects of ferroelectric TiN/Hf_{0.5}Zr_{0.5}O₂/Ge capacitors grown by plasma assisted atomic oxygen deposition

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Abstract

The reliability of Hf_{0.5}Zr_{0.5}O₂ (HZO) metal-ferroelectric-semiconductor capacitors grown by plasma assisted atomic oxygen deposition on Ge substrates is investigated with an emphasis on the influence of crystallization annealing. The capacitors show very weak wake-up and imprint effects allowing reliable operation in excess of 10 years, which is attributed partly to the clean, oxide-free Ge/HZO bottom interface. The weak temperature dependence as well as the observed asymmetries between polarization up and down states and between positive and negative coercive voltage shifts, lead to the conclusion that imprint is controlled by carrier injection at the top electrode interface. The latter mechanism is associated with trapping at interfacial oxygen-vacancy defects. On the other hand, using ultrafast (millisecond) flash annealing improves the leakage current by at least an order of magnitude and the endurance by a factor of 3 compared to conventional rapid thermal annealing, which makes them suitable for low power non-volatile memory applications where (ultra)thin HZO is an essential requirement.

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The discovery of ferroelectricity in Si-compatible, HfO_2 -based oxides¹ and the recent progress² in scaling the ferroelectric (FE) Zr-doped HfO_2 down to 1 nm, has ignited an immense interest of the scientific and engineering community to exploit these materials for the fabrication of low power embedded non-volatile memories (NVM)^{3,4}. Successful integration with CMOS of FeRAM comprising 1C-1T metal-ferroelectric-metal (MFM) capacitors with FE $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$ (HZO) has been demonstrated^{5,6}.

Beyond MFM, the metal-ferroelectric-semiconductor (MFS) structures can be used for the fabrication of FE field effect transistors (FeFET) with applications in neuromorphic technologies⁷⁻¹⁰, negative capacitance FET^{11,12} for low power logic and ferroelectric tunnel junctions (FTJ) NVM¹³ with enhanced tunneling electroresistance.

Germanium (Ge) semiconductor could be a good choice for MFS since it is fully compatible with Si and, according to the recent IRDS update 2020¹⁴, it is considered as one of the channel material technology inflections for future nodes beyond the year 2028. Moreover, the dopant activation in Ge varies between 550 and 700 °C, therefore it is compatible with the HZO crystallization annealing, which also varies in the same temperature range, thus enabling Ge FeFETs processing in the preferred “gate first” flow. The importance of Ge has already been recognized¹⁵ and a number of advanced devices such as Ge nanowire FET¹⁰, NCFET¹² and FTJs¹⁶ have been demonstrated.

An advantage of Ge is that it forms clean interfaces with HZO without an interfacial layer as evidenced in a number of earlier^{17,18} and more recent works¹⁹⁻²¹. This could mitigate²² or totally alleviate some of the reliability problems^{3,23} such as endurance, imprint and wake-up behavior which are associated with the presence of non-ferroelectric (dead) layers at the HZO/semiconductor interface. A big concern is imprint^{3,23}, that is a shift over time of the hysteresis loop along the voltage axis and is already present at room temperature resulting in retention loss. An equally important problem is the constricted (pinched) hysteresis loops^{3,23} typically obtained in pristine devices. Such devices need extensive cycling to open the loop (“wake-up”) which jeopardizes the performance of NVM. The origin and the possible

correlation between imprint and wake-up effects are not known yet in detail²⁴⁻³¹. Here, we deepen our understanding of the mechanism driving imprint and wake-up effects in HZO Ge MFS. Then, we show that depending on the crystallization annealing method, either wake-up and imprint effects can be minimized or leakage current and endurance can be improved, making Ge MFS a prospective candidate for future NVM technologies.

The device layer structure consists of 15 nm HZO/10 nm TiN grown on p-type (0.03-0.07 $\Omega\cdot\text{cm}$) Ge (100) substrate by plasma assisted atomic oxygen deposition²⁰ in a ultra-high vacuum (UHV) system dedicated to molecular beam epitaxy (MBE) of oxides (Fig. S1). HZO is grown amorphous at 120 °C.

The grown structures are cut in two pieces, then crystallization annealing is performed using two different methods (Fig. S2): A two stage rapid thermal annealing (RTA) is performed on one piece with a 550 °C preheating for 30 sec followed by a second RTA step at 750 °C for 20 sec (150 °C/sec), then finished by a rapid cooling (85 °C/sec). The preheating is found to reduce the leakage current and improve the P-V characteristics. A millisecond flash annealing (FLA)³² is performed on the second piece: a preheat at 375 °C (previous study³² shows that the 120 s pre-heat only is not sufficient to crystallize HZO) is followed by an energy flash of 70 J/cm². 50x50 μm^2 capacitors are then processed by optical lithography and lift off using Ti/Pt as the metal electrode, followed by TiN etching using a $\text{NH}_4\text{OH}/\text{H}_2\text{O}_2/\text{H}_2\text{O}$ solution, to define the capacitor areas.

Fig. 1 shows the grazing incidence X-ray diffraction analysis of as-deposited (pink curve) and after FLA (black curve) films. The exponential background is subtracted. The as-deposited films are amorphous, while after FLA the HZO films are polycrystalline, and show a sharp diffraction peak centered at $2\theta-\omega = 30.52^\circ$, characteristic of the pure FE orthorhombic phase or the tetragonal phase. No additional peaks are observed at $\sim 28.3^\circ$ nor at $\sim 31.3^\circ$, indicating that no monoclinic phase has formed.

Typical displacement current density (I-V) and polarization (P-V) hysteresis loops for RTA and FLA-annealed capacitors are shown in Fig. 2 for comparison. It can be inferred that the RTA capacitors have weak or no wake-up effects since the pristine curve does not differ much from the fully open hysteresis loop after 65 cycles (Fig. 2(b), (d)). On the contrary, the FLA samples show a pristine P-V hysteresis curve which is slightly constricted and recovers to a fully open P-V characteristic only after 1000 cycles (Fig. 2(a), (c)). After wake-up, the FLA is comparable to the RTA P-V curve albeit with a slightly lower P_r and slightly larger coercive field E_c . Nevertheless, the FLA capacitors are more robust and show better yield after wake-up. Moreover, the parasitic polarization is smaller for FLA especially in the up state (negative gate bias) as seen from PUND measurements in Fig. S3.

The wake-up effects in the FLA films can be explained by several mechanisms, all related to the presence of oxygen vacancies at the interfaces between HZO and the electrodes, rather than in the bulk. First, the redistribution of oxygen vacancies^{25,28} during cycling can lead to depinning of FE domains²⁸. Second, the vacancies could induce transformation of eventual tetragonal grains to the orthorhombic phase^{23, 26, 27}. Note that a transformation from the monoclinic to the orthorhombic phase, here, is excluded (see the absence of monoclinic grains in the XRD in Fig. 1). Finally, electron trapping into deep states at oxygen vacancies^{29,31}, causing local imprint fields²⁹ which pinch the ferroelectric domains, are considered to be the most probable cause for wake-up. Further, such fields are discussed in more detail below in connection to imprint behavior.

The DC leakage current density and the fatigue/endurance of the RTA and FLA capacitors are presented for comparison in Fig. 3. Before and after wake-up, the FLA capacitors clearly have a lower leakage current compared to RTA capacitors (Fig. 3(a)). After wake up, the leakage of the FLA capacitors increases but it remains an order of magnitude lower than for the RTA ones. It is considered^{33,34} that oxygen vacancies at the grain or domain wall boundaries in the bulk of HZO are the main cause of DC leakage currents. Given that oxygen vacancies are

likely to occur primarily at the top TiN/HZO interface³⁵, it is anticipated that the short (ms) flash annealing time is not sufficient to induce vacancy diffusion in the bulk, thus resulting in less leakage. Nevertheless, the possibility that the observed leakage differences partly originate from the different microstructures likely present in RTA and FLA capacitors cannot be excluded.

It can be inferred from Fig. 3(b) that the FLA capacitors have a better endurance of up to 2×10^5 cycles compared to the RTA ones which break after 6×10^4 cycles. Increased endurance in the FLA sample is probably due to less leakage (Fig. 3(a)) which is known to be the main reason for breakdown²³. It is anticipated that the higher leakage induces more easily conducting paths after some cycling so the ferroelectric in RTA capacitors breaks faster (in less cycles), effectively becoming a resistor. As an alternative explanation it should be noted that the P_r in the FLA samples is lower, favoring a larger endurance. This behavior follows a trend already reported in the literature²³, according to which endurance increases with decreasing P_r .

Retention of programmed (stored) polarization states is mainly affected by depolarization mechanisms (e.g. depolarizing electric fields) and by imprint. The latter is thought to be the main cause of retention loss especially for the opposite state (the state opposite to the programmed one)³.

One of the imprint scenarios^{31, 36} is schematically illustrated in Fig. 4 and a phenomenological description is given below. The imprint is primarily due to the insufficient screening of polarization charges by the free carriers in the metal which creates depolarizing electric fields (E_{dep})³⁷ inside the FE and electric fields E_d at the interfacial dielectric (dead) layer (Fig. 4(a), (c)). Without losing generality in our case, a TiO_xN_y dead layer is formed²⁹ by reaction at the top HZO/TiN interface, associated with a reduction of HZO by Ti, yielding interfacial oxygen vacancy defects. The dead layer acts as a tunneling barrier, regulating the trapping (P_{UP}) and detrapping (P_{DOWN}) of charges at interfacial defects.

It should be noted that in our MFS structure, the bottom electrode is the Ge semiconductor which forms a clean interface with HZO¹⁹⁻²¹, as already mentioned. The absence of an interface dead layer makes the screening of the polarization charges more efficient reducing the depolarization field. Due to finite screening length in Ge semiconductor, the screening of polarization charges by the Ge free carriers is not as efficient as with a TiN metal (in the ideal case of a clean TiN/HZO interface) or with any other metal. However, Ge, unlike other larger gap semiconductors, is benefited from a large concentration of free carriers, thermally excited across the small band gap at room temperature, which facilitates the screening of polarization charges²¹

The built-in fields redistribute mobile charges over time, screen the polarization charges and establish internal imprint fields E_{imp} in the same direction as the polarization vector, thus stabilizing the stored state (Fig. 4(b), (d)). As a consequence, a larger bias is required to first screen E_{imp} before switching the polarization to the opposite state, manifesting imprint as an increase in V_c (or E_c). The charge redistribution mechanisms can be classified in two main categories. First, the bulk limited conduction³⁸ in the FE (Pool-Frenkel (P-F), trap assisted tunneling (TA), ohmic conduction etc.) under the influence of E_{dep} . Second, the electrode-controlled charge injection by direct tunneling through the interfacial potential barrier³⁸, associated with charge trapping/detrapping at the interfacial defects.

Finally, it is noted that most of the bulk conduction methods (P-F, TA) involve electron transport via defect states in the gap of HZO and at energies which are much higher than the Fermi level (Fig.4(b), (d)). Therefore, bulk conduction mechanisms are thermally activated and at relatively low temperatures of the experiment (25-125 °C), the number of thermally excited carriers is small and the generation of imprint field over time is expected to be very slow processes. On the contrary, the electrode-controlled carrier exchange at the electrode/HZO interface is a temperature independent direct tunneling (DT) process and is expected to be very fast and efficient in building up the imprint fields. It should be mentioned that interface dangling bond states at the Ge/HZO interfaces could contribute as any other

bulk state. More specifically, carriers trapped at the interface states could be thermally excited to the conduction band or to other defect levels inside the HZO gap, subsequently following the bulk-limited conduction mechanisms as illustrated in Fig. 4, contributing to imprint in longer time scales.

Alternative mechanisms as a source of imprint, involving oxygen vacancy diffusion^{25, 28} among others, have also been proposed in the past.

Imprint results as well as programming and reading pulses are presented in Fig. 5. The capacitors are programmed in the down (P vector pointing towards Ge) or up polarization state by applying positive or negative pulses on the gate, respectively. Subsequently, the capacitors are baked on the manipulator stage with no bias on the gate and at different temperatures in vacuum for a certain storage/bake time. Then they are measured at the same temperature (no cooling to RT) by applying a positive/negative triangular read pulse sequence (see Fig. 5(a)).

After the storage/bake time of 10^4 sec, in both cases but more notably in the case of RTA, only the coercive voltages corresponding to the polarization-switching from the programmed to the opposite state shows a shift of $\Delta V_c^+ \sim 0.39\text{-}0.47$ V for P_{UP} and $\Delta V_c^- \sim 0.34\text{-}0.39$ V for P_{DOWN} . This is in line with the phenomenological description given above. The other coercive voltage from the opposite state to the initially programmed one shows negligible variation. This is understood as follows³⁹: the first read (switching) pulse is sufficient to partially de-age the HZO, so the second read (switching) pulse reverses the polarization at the expected V_c . The fast de-aging with just one switching pulse is consistent with the notion of fast carrier exchange between TiN and HZO at the top interface (Fig. 4(b), (d)) as the main origin of imprint. At the relatively low experiment temperatures (25-175 °C), slower processes involving bulk charge conduction or possible oxygen vacancy diffusion²⁸, would require a longer de-aging with a larger number of switching pulses (cycling), which is not the case here. Such processes are expected to be thermally activated with a large activation barrier. However, in our case a weak temperature dependence is observed (Fig. 5(b)), further

supporting the suggestion that temperature independent direct tunneling at the top interface controls the formation of imprint fields.

In the case of the FLA capacitors, a larger imprint of $\Delta V_c^+ \sim 0.49\text{-}0.68$ V for P_{UP} and $\Delta V_c^- \sim 0.42\text{-}0.48$ for P_{DOWN} is observed. It is possible that FLA results in larger concentration of oxygen vacancies at the interfaces and/or thinner TiO_xN_y barriers, facilitating the formation of imprint fields due to more efficient trapping/detrapping. To better understand the difference between the RTA and FLA, we consider the following. During RTA, the oxygen vacancies diffuse in the bulk, as opposed to the case of ultrafast (ms) FLA where most of the vacancies remain at the interface thereby enhancing the imprint. It is interesting to note that FLA capacitors also show larger wake-up effects (see Fig. 2), pointing to a possible correlation between the two effects (imprint and wake-up) as previously suggested^{23, 29}. Both have their origin to the inhomogeneous distribution of oxygen vacancies with a preferred accumulation at the top interface.

It is also inferred from Fig. 5 (b) that the P_{UP} imprint is larger compared to P_{DOWN} imprint. This difference between P_{UP} and P_{DOWN} is more pronounced for FLA capacitors. Similar asymmetries have been reported⁴⁰ for Si MFS with poly Si top electrode. This observation of larger P_{UP} imprint is related to the asymmetry between trapping and detrapping efficiency which is, in turn, a consequence of the electrode asymmetry. The bottom Ge electrode has the same screening efficiency in both polarizations (accumulation and inversion) due to a clean interface, hence it plays a minor role. On the other hand, the interface TiO_xN_y dielectric barrier at the top electrode is important since it regulates the trapping (P_{UP}) and detrapping (P_{DOWN}) of charges at interfacial defects. As seen from Fig. 4, trapping (carrier injection) occurs during P_{UP} (Fig. 4(a)) by tunneling through a smaller barrier compared to detrapping during P_{DOWN} (Fig. 4(b)). Thus, in the P_{UP} configuration, the top interface allows for a more efficient screening of polarization charges and thereby helps establishing larger imprint fields. It should be noted that in the case of an MFM structure there is a symmetry between top and bottom interfaces so a symmetric imprint for the P_{UP} and P_{DOWN} polarizations is expected.

The observed imprint, especially for RTA capacitors, is better than that observed in several ALD deposited Al:HfO₂⁴⁰ Si MFS and (La-doped) HZO MFM^{30,31,41}. Our thick (15nm) HZO are also comparable to the best reported²⁹ in the literature for MFM with thin (7nm) ALD HZO. The good imprint results obtained in our films are primarily attributed to the clean Ge/HZO bottom interface. This fact, combined with the abundance of free carriers in the low gap Ge²¹, allow the effective screening of the polarization charges. The rather weak imprint, primarily in the RTA capacitors, may also be due to the particular growth methodology of HZO and TiN. The use of reactive atomic oxygen and nitrogen results in efficient oxidation and nitridation, thus minimizing the oxygen vacancies at the interface.

Setting the criterion for failure to V_c^+/V_c^- not exceeding ± 3.5 V (the write voltage), it is inferred from the projections in Fig. 5(b) that RTA capacitors are not expected to fail before 10 years which is a figure of merit for reliability. Even with a stricter criterion for failure at only ± 3 V, the RTA capacitors comply with the 10-year limit, although marginally. FLA capacitors on the other hand, cannot meet the same standards of reliability (they are predicted to fail before 10 years) due to a slightly larger coercive voltage in the pristine state and a larger imprint.

In summary, reliability measurements of HZO Ge MFS capacitors show that imprint and wake-up effects are correlated and are influenced by the HZO/TiN plasma assisted atomic oxygen growth methodology as well as the crystallization annealing processing. The behavior of the V_c shifting with time and temperature, indicates that the top TiN/HZO electrode-controlled trapping/detrapping at interfacial oxygen-vacancy defects is the primary source of imprint fields. RTA results in MFS capacitors with very weak wake-up effects and small imprint which are very essential for the operation and reliability of Ge FeFET devices. On the other hand, FLA capacitors show better endurance and improved leakage which makes them suitable for low power applications, where ultrathin HZO is an essential requirement.

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Supplementary Material: See supplementary material for details about materials growth and crystallization annealing techniques and PUND measurements of Ge MFS capacitors.

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Data Availability Statement: The data that support the findings of this study are available from the corresponding author upon reasonable request.

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PLEASE CITE THIS ARTICLE AS DOI: 10.1063/5.0029657

References

1. T. S. Böske, J. Müller, D. Bräuhäus, U. Schröder, and U. Böttger, *Appl. Phys. Lett* **99**, 102903 (2011).
2. S. S. Cheema, D. Kwon, N. Shanker, R. d. Reis, S.-L. Hsu, J. Xiao, H. Zhang, R. Wagner, A. Datar, M. R. McCarter, C. R. Serrao, A. K. Yadav, G. Karbasian, C.-H. Hsu, A. J. Tan, L.-C. Wang, V. Thakare, X. Zhang, A. Mehta, E. Karapetrova, R. V. Chopdekar, P. Shafer, E. Arenholz, C. Hu, R. Proksch, R. Ramesh, J. Ciston, and S. Salahuddin, *Nature* **580**, 478 (2020).
3. C.-S. Hwang and T. Mikolajick, *Advances in Non-volatile Memory and Storage Technology*, 2nd ed. (Woodhead Publishing, 2019), Chap. 11-Ferroelectric Memories, p. 393.
4. T. Mikolajick, U. Schroeder, and S. Slesazeck, *IEEE Transactions on Electron Devices* **67**, 1434 (2020).
5. T. Francois, L. Grenouillet, J. Coignus, P. Blaise, C. Carabasse, N. Vaxelaire, T. Magis, F. Aussenac, V. Loup, C. Pellissier, S. Slesazeck, V. Havel, C. Richter, A. Makosiej, B. Giraud, E. Breyer, M. Materano, P. Chiquet, M. Bocquet, E. Nowak, U. Schröder, and F. Gaillard, *IEEE International Electron Devices Meeting* (2019), p. 15.7.1.
6. J. Okuno, T. Kunihiro, K. Konishi, H. Maemura, Y. Shuto, F. Sugaya, M. Materano, T. Ali, K. Kuehnel, K. Seidel, U. Schröder, T. Mikolajick, M. Tsukamoto, T. Umebayashi, in *Symposium on VLSI Technology & Circuits* (2020), TF2.1.
7. H. Mulaosmanovic, J. Ocker, S. Müller, M. Noack, J. Müller, P. Polakowski, T. Mikolajick, and S. Slesazeck, in *Symposium on VLSI Technology* (2017), p. T176.
8. M. Jerry, P. Y. Chen, J. Zhang, P. Sharma, K. Ni, S. Yu, and S. Datta, *IEEE International Electron Devices Meeting* (2017), p. 6.2.1.
9. H. Mulaosmanovic, E. Chicca, M. Bertele, T. Mikolajick, and S. Slesazeck, *Nanoscale* **10**, 21755 (2018).

This is the author's peer reviewed, accepted manuscript. However, the online version of record will be different from this version once it has been copyedited and typeset.

PLEASE CITE THIS ARTICLE AS DOI: 10.1063/5.0029657

10. W. Chung, M. Si, and P. D. Ye, *IEEE International Electron Devices Meeting* (2018), p. 15.2.1.
11. D. Kwon, S. Cheema, N. Shanker, K. Chatterjee, Y.-H. Liao, A. J. Tan, C. Hu, and S. Salahuddin, *IEEE Electron Device Letters* **40**, 993 (2019).
12. J. Li, J. Zhou, G. Han, Y. Liu, Y. Peng, J. Zhang, Q.-Q. Sun, D. W. Zhang, and Y. Hao, *IEEE Transactions on Electron Devices* **65**, 1217 (2018).
13. Z. Wen, and D. Wu, *Adv. Mater.* **32**, 1904123 (2019).
14. See IRDS 2020, <https://irds.ieee.org/editions/2020>, for information about Ge considered as one of the channel material technology inflections for future nodes beyond the year 2028.
15. X. Tian, L. Xu, S. Shibayama, T. Nishimura, T. Yajima, S. Migita, and A. Toriumi, *IEEE International Electron Devices Meeting* (2017), p. 816.
16. Y. Goh, and S. Jeon, *Nanotechnology* **29**, 335201 (2018).
17. A. Dimoulas, G. Mavrou, G. Vellianitis, E. Evangelou, and N. Boukos, *Appl. Phys. Lett.* **86**, 032908 (2005).
18. A. Dimoulas, D. P. Brunco, S. Ferrari, J. W. Seo, Y. Panayiotatos, A. Sotiropoulos, T. Conard, M. Caymax, S. Spiga, M. Fanciulli, C. Dieker, E. K. Evangelou, S. Galata, M. Houssa, and M. M. Heyns, *Thin Solid Films* **515**, 6337 (2007).
19. P. D. Lomenzo, Q. Takmeel, C. M. Fancher, C. Zhou, N. G. Rudawski, S. Moghaddam, J. L. Jones, and T. Nishida, *IEEE Electron Device Lett.* **36**, 766 (2015).
20. C. Zacharaki, P. Tsipas, S. Chaitoglou, S. Fragkos, M. Axiotis, A. Lagoyiannis, R. Negrea, L. Pintilie, and A. Dimoulas, *Appl. Phys. Lett.* **114**, 112901 (2019).
21. C. Zacharaki, P. Tsipas, S. Chaitoglou, E. K. Evangelou, C. M. Istrate, L. Pintilie, and A. Dimoulas, *Appl. Phys. Lett.* **116**, 182904 (2020).
22. K.-Y. Chen, Y.-H. Huang, R.-W. Kao, Y.-X. Lin, K.-Y. Hsieh, and Y.-H. Wu, *IEEE Transactions on Electron Devices* **66**, 3636 (2019).
23. M. H. Park, Y. H. Lee, T. Mikolajick, U. Schröder, and C. S. Hwang, *MRS Commun.* **8**, 795 (2018).

This is the author's peer reviewed, accepted manuscript. However, the online version of record will be different from this version once it has been copyedited and typeset.

PLEASE CITE THIS ARTICLE AS DOI: 10.1063/5.0029657

24. T. Schenk, M. Hoffmann, J. Ocker, M. Pešić, T. Mikolajick, and U. Schroeder, *ACS Appl. Mater. Interfaces* **7**, 20224 (2015).
25. S. Starschich, S. Menzel, and U. Böttger, *Appl. Phys. Lett.* **108**, 032903 (2016)
26. M. Pešić, F. P. Gustav Fengler, L. Larcher, A. Padovani, T. Schenk, E. D. Grimley, X. Sang, J. M. LeBeau, S. Slesazeck, U. Schroeder, and T. Mikolajick, *Adv. Funct. Mater.* **26**, 4601 (2016).
27. E.D. Grimley, T. Schenk, X. Sang, M. Pešić, U. Schröder, T. Mikolajick and J. M. LeBeau, *Adv. Electron. Mater.* **2**, 1600173 (2016).
28. F. P. G. Fengler, M. Pešić, S. Starschich, T. Schneller, C. Küneth, U. Böttger, H. Mulaosmanovic, T. Schenk, M. H. Park, R. Nigon, P. Mural, T. Mikolajick, and U. Schröder, *Adv. Electron. Mater.* **3**, 1600505 (2017).
29. F. P. G. Fengler, M Hoffmann, S Slesazeck, T Mikolajick, and U. Schröder, *J. Appl. Phys.* **123**, 204101 (2018).
30. F. Mehmood, M. Hoffmann, P. D. Lomenzo, C. Richter, M. Materano, T. Mikolajick, and U. Schröder, *Adv. Mater. Interfaces*, **6** 1901180 (2019).
31. P. Buragohain, A. Erickson, P. Kariuki, T. Mittmann, C. Richter, P. D. Lomenzo, H. Lu, T. Schenk, T. Mikolajick, U. Schröder, and A. Gruverman, *ACS Appl. Mater. Interfaces* **11**, 35115 (2019).
32. É. O'Connor, M. Halter, F. Eltes, M. Sousa, A. Kellock, S. Abel, and J. Fompeyrine, *APL Materials* **6**, 121103 (2018).
33. L. Le and D. Vanderbilt, *Phys. Rev B* **68**, 134103 (2003).
34. D. R. Islamov, A. G. Chernikova, M. G. Kozodaev, T. V. Pervalov, V. A. Gritsenko, O. M. Orlov, and A.V. Markeev, *ECS Trans.* **75**, 5 (2016).
35. W. Hamouda, A. Pancotti, C. Lubin, L. Torteck, C. Richter, T. Mikolajick, U. Schröder, and N. Barrett, *J. Appl. Phys.* **127**, 064105 (2020).
36. A. K. Tagantsev, I. Stolichnov, N. Setter, and J. S. Cross, *J. Appl. Phys.* **96**, 6616 (2004).
37. R. R. Mehta, B. D. Silverman, and J. T. Jacobs, *J. Appl. Phys.* **44**, 3379 (1973).

This is the author's peer reviewed, accepted manuscript. However, the online version of record will be different from this version once it has been copyedited and typeset.

PLEASE CITE THIS ARTICLE AS DOI: 10.1063/5.0029657

38. F.-C. Chiu, *Adv. Mater. Sci. Engineer.* **2014**, 578168, 1-18 (2014).
39. C. Peter and H. Kliem, *J. Appl. Phys.* **125**, 174107 (2019).
40. K. Florent, S. Lavizzari, L. D. Piazza, M. Popovici, J. Duan, G. Groeseneken, and J. V. Houdt, *IEEE-TED* **64**, 4091 (2017).
41. F. Mo, T. Saraya, T. Hiramoto, M. Kobayashi, *Appl. Phys. Express* **13**, 074005 (2020).

Figure captions:

Figure 1: GIXRD spectra before (pink) and after (black) FLA. ω is set to 0.37 deg and the exponential background is subtracted.

Figure 2: Pristine and waked up ferroelectric hysteresis loops obtained at 1kHz. Displacement current density (I-V) for FLA (a) and RTA (b) and polarization (P-V) for FLA (c) and RTA (d).

Figure 3: (a) DC leakage current density (I-V) of RTA and FLA before and after the wake-up. (b) Fatigue/endurance measurements of RTA and FLA capacitors.

Figure 4: Schematic illustration of charge redistribution giving rise to imprint field E_{imp} . (a) and (b) correspond to polarization up state immediately after writing and after a finite store time, respectively. (c) and (d) correspond to polarization down state. t denotes the time elapsed after the ferroelectric is poled in the UP or DOWN polarization state. P is the polarization vector and E_{imp} is the imprint electric field. E_{dep} , E_d and E_s are the depolarizing electric field, the electric field across the dielectric dead layer at the top interface, and the surface electric field in the semiconductor, respectively. P-F mark the Pool-Frenkel transport and TA mark conduction in the ferroelectric through trap assisted tunneling. DT denotes direct tunneling through the interfacial barrier.

Figure 5: (a) Hysteresis loops of RTA and FLA capacitors at room temperature (RT) showing the coercive voltage shifts ΔV_c^+ and ΔV_c^- indicated by arrows. The schematic on the right side shows the programming and reading pulses (rise time 1ms). (b) The V_c variation as a function of storage time t for different temperatures. The dashed lines are projections in time of the V_c^+ , V_c^- variations. The schematics on the right side show the P_{UP} and P_{DOWN} configurations.

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