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Published in:

I E E E Journal of Emerging and Selected Topics in Power Electronics

Link to article, DOI:

[10.1109/JESTPE.2020.2966143](https://doi.org/10.1109/JESTPE.2020.2966143)

Publication date:

2020

Document Version

Peer reviewed version

[Link back to DTU Orbit](#)

Citation (APA):

Ammar, A. M., Spliid, F. M., Nour, Y., & Knott, A. (Accepted/In press). Analysis and Design of a Charge-Pump-Based Resonant AC-DC Converter with Inherent PFC Capability. *I E E E Journal of Emerging and Selected Topics in Power Electronics*. <https://doi.org/10.1109/JESTPE.2020.2966143>

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Analysis and Design of a Charge-Pump-Based Resonant AC-DC Converter with Inherent PFC Capability

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Abstract— This paper presents the analysis and design of a resonant power factor correction (PFC) rectifier for the first stage in single-phase front-end offline converters targeting low-power applications (up to 100 W). With the addition of a charge pump circuit comprised of a capacitor and a diode to a class-DE resonant converter, PFC functionality is achieved inherently. The operation is based on soft switching, allowing for increased switching frequencies with reduced switching losses. A 1 MHz prototype employing wide-bandgap (WBG) switching devices is built and tested to validate the analysis and proposed design method. The prototype achieves up to 50 W of output power with a power factor of 0.99, a total harmonic distortion (THD) of 8.6 %, and an efficiency of up to 88 %; with harmonic magnitudes well-within the IEC 61000-3-2 standard class-C device limits, making it suitable for use as the rectifier stage in LED drivers. Despite the additional circuit stresses from the charge pump operation, the proposed converter offers simplicity and low component overhead, with the potential for higher frequency operation towards higher power densities.

Index Terms— AC-DC power conversion, power factor correction, resonant power conversion, charge pump, wide-bandgap semiconductors.

I. INTRODUCTION

WITH the current trend towards smaller and highly portable consumer electronics and other industrial applications, research has been investigating the opportunities for minimizing the weights and sizes of products form factors, while achieving the same performance. The main hinder has been the power supplies due to their bulky passive components, where the passive components sizes are inversely proportional to the switching frequencies of the converters. One such application with a great demand for miniaturization is offline converters.

The typical solution for offline converters is a two-stage architecture, as shown in Fig. 1. The first stage is an AC-DC power factor correction (PFC) rectifier followed by an energy-storage capacitor to filter the double-the-line 100/120 Hz frequency component. The second stage is a DC-DC converter

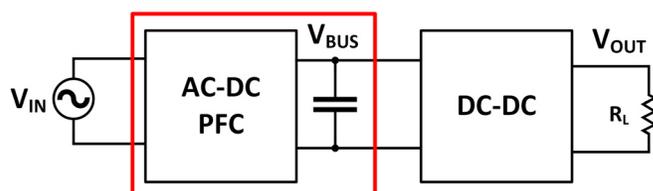


Fig. 1. Offline converter structure. The red box outlines the focus of this work. providing the voltage and current levels that apply to the load electrical characteristics. This conversion has to comply with a number of regulations dictating the shape of the input current to limit the mains voltage distortion [1][2].

Pulse-width-modulated (PWM) converters have been the primary candidate for the AC-DC stage in offline converters, including buck [3]-[6], boost [7][8], buck-boost [9][10], flyback [11], and SEPIC [12][13] converters. They can provide high power factor and are easy to control. However, their operation is based on hard switching. Accordingly, they typically operate at low frequencies in order to limit the switching losses. This in turn results in large sizes for the passive components needed to store and process the energy transferred to the load every switching cycle. On the other hand, high-frequency designs have less efficiency and may incorporate a heat sink for thermal management, which counteracts the gain in power density.

Accordingly, soft-switching resonant converters have been receiving much attention in the recent years [14]-[17]. Resonant converters have substantially lower switching losses than their PWM counterparts. Thanks to their zero-voltage-switching (ZVS) and/or zero-current-switching (ZCS) characteristics, which make them a good candidate for achieving high efficiencies at high frequencies. That in turn results in reduced sizes for the passive components, and thus higher power densities, higher loop-gain bandwidths, and faster transient responses. This has led to the investigation of their adoption into different applications conventionally dominated by PWM converters, including DC-DC [18]-[29] and AC-DC conversion [30]-[35].

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No. 731466. The authors are with the Department of Electrical Engineering, Technical University of Denmark, DK-2800 Kongens Lyngby, Denmark (e-mail:

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Part of this work has been presented at the 2019 IEEE 20th Workshop on Control and Modeling for Power Electronics in Toronto, Canada.

In this paper, the analysis and design flow for a resonant PFC rectifier for single-phase offline converters are presented. The system, shown in Fig. 2, incorporates an input filter and bridge, a charge pump circuit, a DC energy-storage capacitor, and a class-DE converter. The proposed converter can achieve PFC inherently, where the operation is based on soft switching, allowing for high-frequency design with reduced passives sizes, in addition to freedom from the limited bandwidths of the PFC controllers available on the market.

This paper is organized as follows: section II illustrates the principle of operation of the proposed converter. Circuit analysis is presented in section III. Section IV covers the design process of the converter. Prototype implementation and experimental results are shown in section V. Finally, conclusion is provided in section VI.

II. PRINCIPLE OF OPERATION

This section describes the principle of operation of the charge pump PFC converter. A charge pump electronic ballast circuit is reported in [36]. With the addition of an auxiliary circuit comprised of a capacitor and a diode to a conventional high-frequency inverter circuit, the input current can be regulated to follow the input voltage. In this work, the charge pump circuit is incorporated into a class-DE series-resonant converter, as shown in Fig. 3, where the inverter circuit is cascaded by a high-frequency rectifier for enabling use in AC-DC converters [37].

The driving signals to the switches are synchronized with a switching frequency that guarantees operation above resonance, with the same duty cycle and extended dead time. This allows the resonant tank current to charge and discharge the half-bridge switches output capacitances, so that their voltages reach the appropriate rail voltage before switching the gate, thus ensuring ZVS. Additionally, the DC energy-storage capacitor C_{DC} is placed at the inverter input, thus helping to achieve soft-switching operation along the constantly varying AC input line voltage, with no effect on the power factor and input current shape.

Fig. 4 shows a simplified circuit diagram for the power converter, where the input filter is omitted and a diode D_B models the input bridge for simplicity. The figure also shows

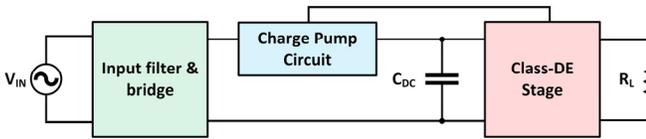


Fig. 2. Proposed PFC stage architecture.

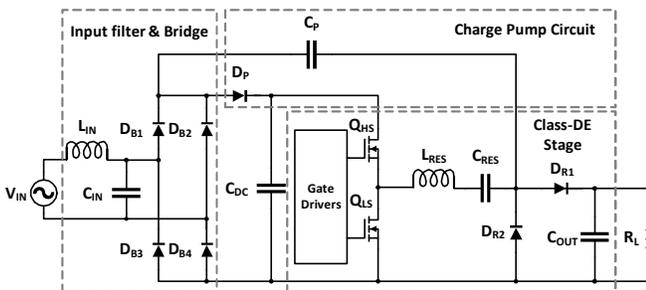


Fig. 3. Proposed PFC converter.

the voltages and currents signs convention used throughout the analysis and rest of figures.

The DC energy-storage capacitor C_{DC} is designed in accordance with the pump capacitor C_P such that the voltage V_{DC} is always higher than the input voltage V_{IN} , and thus the diode bridge D_B and the pump diode D_P do not cross-conduct. As a result, the input current I_{IN} is equal to the charging current of the pump capacitor (positive I_P).

A. Operation across Line Cycle

Fig. 5 shows the behavioral circuit operation across half an input line cycle. As the charge pump capacitor is connected between a low-frequency voltage node V_B and a high-frequency voltage node V_{REC} , charge flows through C_P only during voltage changes on the high-frequency node. This results in voltage changes across C_P , as the other node is relatively constant with respect to high-frequency voltage changes. The pump capacitor charge Q_P is proportional to the capacitor value C_P and the voltage across it, V_P , where the latter varies between a low-frequency high-value V_{P_high} and a constant low-value V_{P_low} . The circuit design ensures that the voltage variation across the pump capacitor V_P follows the input voltage V_{IN} across the line cycle, resulting in a charge variation Q_P , and accordingly an input current, proportional to the input voltage, and a unity power factor can ideally be obtained.

It is noted that the V_{REC} voltage can be any kind of waveform with a constant AC amplitude, and the DC bias of V_{REC} has no effect on the input current shape, which makes the proposed converter architecture, shown in Fig. 2, compatible with different arrangements for the resonant tank, including the parallel-resonant, LCC, and LLC arrangements.

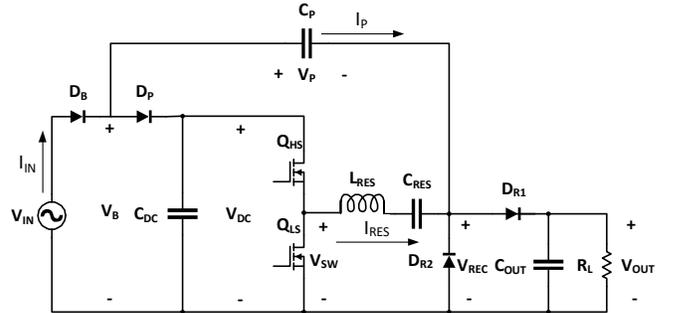


Fig. 4. Simplified circuit diagram for half-line cycle operation.

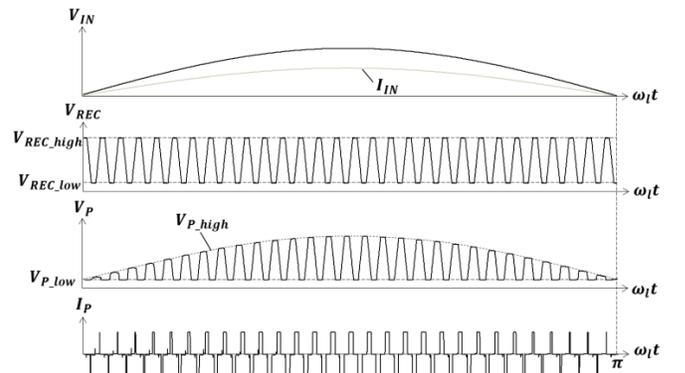


Fig. 5. Behavioral circuit operation across half a line cycle (50 Hz).

B. Operation across Switching Cycle

Fig. 6 shows waveforms for several circuit currents and voltages across two switching cycles, where the circuit and devices parasitics are ignored for simplicity. The circuit operation spans six intervals, where energy is exchanged between the line input, the pump capacitor, the resonant tank, the DC capacitor, and the load. The converter operates in the inductive mode of operation, where the resonant tank current I_{RES} lags the switching node voltage V_{SW} , and thus ZVS can be achieved. Fig. 7 shows the equivalent circuits and resonant tank current paths across the different intervals of operation.

In interval 1 (including 1A and 1B), the voltage V_B is lower than V_{DC} and higher than V_{IN} , so both the diodes D_B and D_P are off, and no current flows through the pump capacitor. Meanwhile, the energy stored in the circuit is transferred to the output through D_{R1} . Fig. 7 (a) shows the resonant inductor current direction in interval 1A, where the high side switch is on and the low side switch is off, and charge flows from the DC capacitor through the resonant tank to the load. In interval 1B, the switching node voltage toggles, and the energy stored in the resonant tank is transferred to the output, as shown in Fig. 7 (b).

Interval 2 takes place across the fall time of V_{REC} . Once V_{REC} starts to decrease, V_B has to decrease along, until D_B is forward biased and V_B is pulled to V_{IN} . While V_{REC} continues to decrease, with V_B almost constant (as the grid frequency is significantly lower than the switching frequency), V_P increases and C_P is charged by the line current I_{IN} , as shown in Fig. 7 (c), until V_{REC} reaches its low value and V_P reaches its high value, where

$$V_{P_high} = V_{IN} - V_{REC_low} \quad (1)$$

Meanwhile, V_{SW} is low, so C_P charges through the resonant tank and low-side switch, and the load is supplied by C_{OUT} .

The third interval (including 3A and 3B) begins once V_{REC} settles at the low-value, when C_P stops charging and while D_P still blocks. Similar to interval 1, no current flows through the pump capacitor and V_P is constant. Fig. 7 (d) shows the resonant tank current direction in interval 3A, where the current

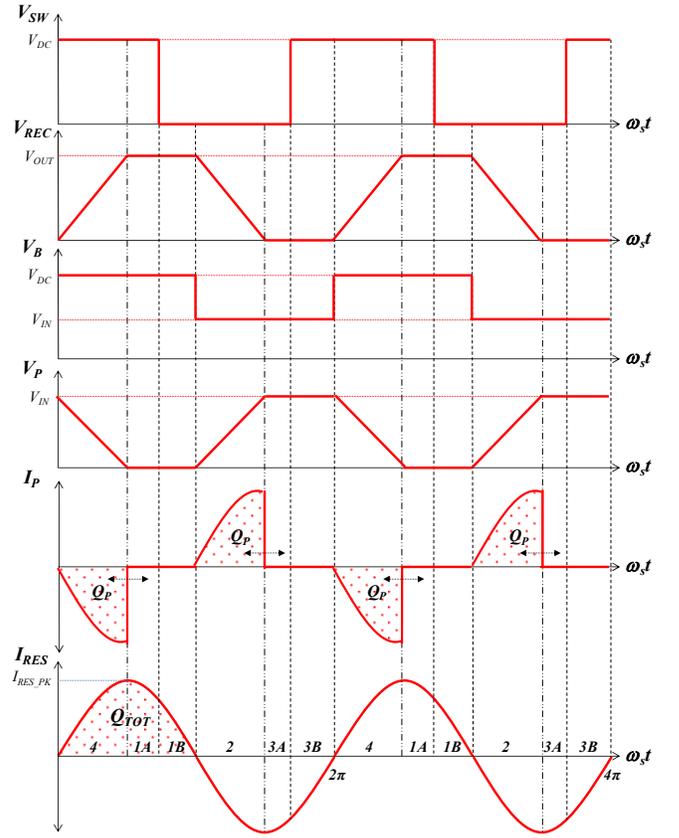


Fig. 6. Circuit operation across two switching cycles (Arrows on the pump capacitor current I_P waveform reflect the variation of the capacitor charge Q_P across line cycle).

freewheels in D_{R2} and Q_{LS} . In interval 3B, the switching node voltage toggles, and energy is transferred from the resonant tank to the DC capacitor through Q_{HS} and D_{R2} , as shown in Fig. 7 (e). Throughout the interval, the load is supplied by C_{OUT} .

Interval 4 takes place across the rise time of V_{REC} . Once V_{REC} starts to increase, V_B has to increase along until D_P is forward biased and V_B is pulled to V_{DC} . While V_{REC} continues

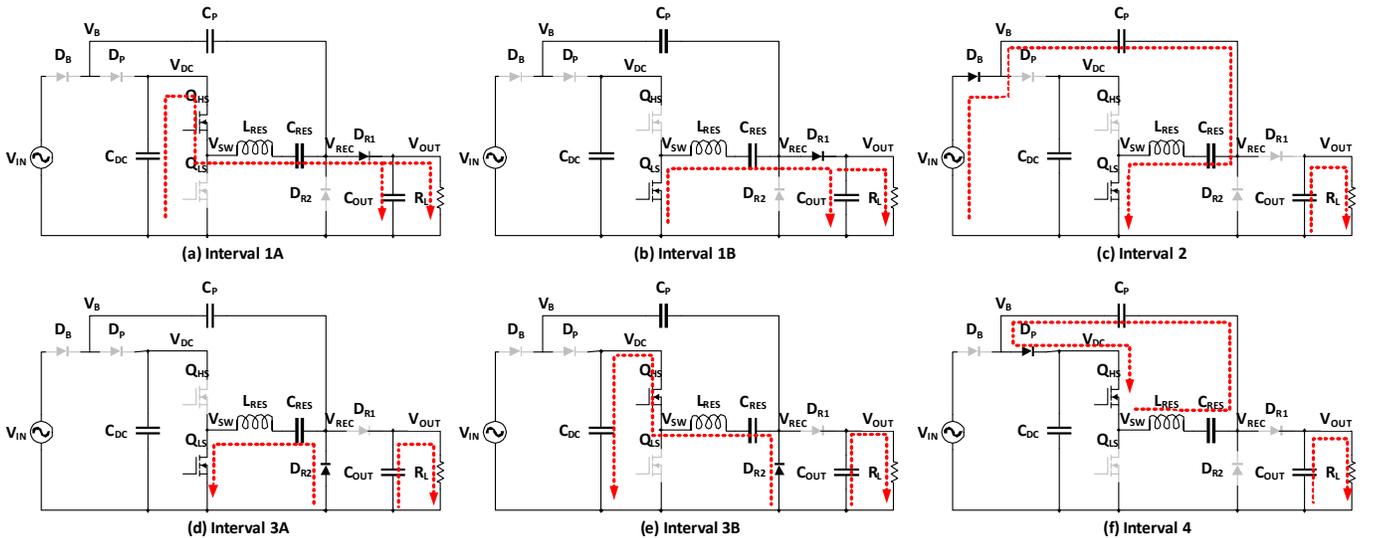


Fig. 7. Equivalent circuits with resonant tank current paths (dashed arrows) across different intervals of operation.

decreasing, with V_{DC} almost constant, V_P decreases and energy transfers from C_P to resonant tank, as shown in Fig. 7 (f), until V_{REC} reaches its high value, and V_P reaches its low value, where

$$V_{P_low} = V_{DC} - V_{REC_high} \quad (2)$$

Meanwhile, the load is supplied by C_{OUT} . By the end of the fourth interval, operation enters interval 1 again and the cycle repeats.

The analysis shows that the input current is discontinuous, only flows into the circuit during the second interval, and is equal to the charging pump capacitor current (positive I_P shown in Fig. 6), where the charge Q_P is equal to the charge taken from the line input Q_{IN} .

Depending on the value for the input line voltage V_{IN} across the line cycle, the length of intervals 2 and 4 gets extended or narrowed with respect to the amount of charge taken from the input AC mains, which is shown by the arrows on the I_P waveform in Fig. 6. When V_{IN} is high, the majority of the load energy comes from the line, thus Q_{IN} increases, extending the lengths of intervals 2 and 4, which reach their maximum at the peak input AC mains voltage ($\omega t = \pi/2, 3\pi/4$). On the other hand, when the V_{IN} is low, the majority of the load energy comes from the DC capacitor C_{DC} , with reduced charge taken from the input AC mains. That, in turn, narrows the lengths for intervals 2 and 4, which reach zero value at the zero crossings of the input AC mains voltage ($\omega t = \pi, 2\pi$), then the charge Q_P equals zero, as shown in Fig. 5, and all of load energy then comes from C_{DC} . Therefore, at the zero-crossings of the input voltage, the class-DE stage operates in a conventional nature, with no effect from the charge-pump circuit. While at the peaks of V_{IN} , the charge-pump capacitor is at full capacity, loading the resonant tank and DC capacitor with the peak charge taken from the line, resulting in additional circuit stresses that are analyzed as follows.

III. CIRCUIT ANALYSIS

In this section, the circuit analysis is presented. The analysis is based on the First Harmonic Approximation (FHA) approach for modelling resonant converters, which assumes the resonant tank current to be sinusoidal. That is ensured through the design for a high loaded quality factor in the resonant tank. With that assumption, a simple analysis and design flow is presented, sparing the need for an accurate model that takes into account the high-order harmonics in the resonant tank and pump circuit, thus simplifying the design process.

Two conditions for proper functionality of the circuit are illustrated. These conditions set the basis for the design process covered in the following section. In addition, the different circuit stresses that result from the incorporation of the charge-pump circuit into the class-DE resonant stage are analyzed. The stresses include the resonant tank peaking current and the DC capacitor peaking voltage. The section starts with finding the first condition for achieving high power factor based on the principle of operation illustrated in section II, which sets the basis for the class-DE stage design. That is followed by two analyses for the voltage across the DC capacitor, including the average voltage value, which is a function of the pump capacitor C_P size, and the low-frequency voltage ripple, which is a function of the C_{DC} size. Another condition for ensuring full

control over the input current is then illustrated, which sets the requirement for the design of the two capacitors. Eventually, an analysis of the maximum resonant tank peak current across line cycle is presented, which defines the specifications for the resonant inductor design.

A. First Condition for Obtaining High Power Factor

From the circuit operation covered in section II-B, and considering that for a series-resonant tank the rectifier input voltage V_{REC} swings between zero volts and the output voltage, as shown in Fig. 6, (1) and (2) can be re-evaluated as follows

$$V_{P_high} = V_{IN} - V_{REC_low} = V_{IN} - 0 = V_{IN} \quad (3)$$

$$V_{P_low} = V_{DC} - V_{REC_high} = V_{DC} - V_{OUT} \quad (4)$$

The equations show that the envelope of the high values for the voltage across the pump capacitor takes the shape of the input voltage, while the low-values envelope takes the value of the difference between the resonant converter's input and output voltages, which is almost constant in high frequency. Across one switching cycle, the variation of charge in the pump capacitor is equal to

$$Q_P = C_P(V_{P_high} - V_{P_low}) = C_P(V_{IN} - V_{DC} + V_{OUT}) \quad (5)$$

The pump capacitor charging current, which is equal to the input current, averaged over one switching cycle is equal to

$$I_{IN} = \frac{Q_P}{T_s} = f_s \cdot Q_P = f_s \cdot C_P(V_{IN} - V_{DC} + V_{OUT}) \quad (6)$$

where f_s is the converter switching frequency. Considering the class-DE stage is designed to operate near resonance, with a high gain close to unity, the difference between V_{DC} and V_{OUT} gets to be very small. Assuming $V_{DC} \approx V_{OUT}$, (6) is re-evaluated to

$$I_{IN} \approx f_s \cdot C_P \cdot V_{IN} \quad (7)$$

Therefore, in steady state, the input current becomes proportional to the input voltage, resulting in a high power factor and low total harmonic distortion (THD). Accordingly, this condition sets the specification for the class-DE stage design.

B. Energy-Storage Capacitor Average Voltage Analysis

From (6), the input power averaged over a switching cycle is obtained by

$$P_{IN} = V_{IN} \cdot I_{IN} = f_s \cdot C_P \cdot V_{IN}(V_{IN} + V_{OUT} - V_{DC}) \quad (8)$$

And knowing that

$$V_{IN} = V_{IN_pk} \sin(\omega t) \quad (9)$$

The input power averaged over a line cycle is found by

$$P_{IN_avg} = \frac{1}{T_l} \int_0^{T_l} P_{IN} dt = \frac{2}{T_l} \int_0^{\frac{T_l}{2}} P_{IN} dt \quad (10)$$

Substituting (8) in (10), the integral is evaluated to

$$P_{IN_avg} = f_s \cdot C_P \cdot V_{IN_pk} \left[\frac{V_{IN_pk}}{2} + \frac{2}{\pi} (V_{OUT} - V_{DC_avg}) \right] \quad (11)$$

Equating to P_{OUT}/η and rearranging to find V_{DC_avg}

$$V_{DC_avg} = V_{OUT} + \frac{\pi}{2} \left(\frac{V_{IN_pk}}{2} - \frac{P_{OUT}}{\eta \cdot f_s \cdot C_P \cdot V_{IN_pk}} \right) \quad (12)$$

where η is the converter efficiency. Therefore, the charge-pump circuit results in a stress on the DC capacitor voltage, where a larger pump capacitor results in a higher voltage stress across the DC capacitor.

C. Energy-Storage Capacitor Voltage Ripple Analysis

For an AC-DC rectifier, the difference between the instantaneous input power and the constant output power needs to be stored within a circuit element. In case of the proposed converter, that element is the DC energy-storage capacitor C_{DC} . As discussed in section II-B, when the input voltage is high, so is the input power, and the majority of the energy comes from the line and gets stored in the pump capacitor C_P , which then charges the DC bus capacitor C_{DC} , increasing the voltage across it. On the other hand, when the input voltage is low, C_{DC} expends more energy to the load than what it stores from the line, decreasing the voltage V_{DC} . Further, when the input voltage is zero, all energy comes from the DC capacitor and it does not store any charge. This results in a double-the-line-frequency voltage ripple across the DC capacitor, as shown in Fig. 8, which is evaluated from the energy of the DC capacitor as follows. The power flowing into the DC capacitor is

$$P_{DC} = P_{IN} - P_{OUT} \quad (13)$$

Assuming a power factor of one, where the input voltage and current are sinusoids and in phase, and rewriting (8), the input power is calculated to

$$\begin{aligned} P_{IN} &= V_{IN_pk} \cdot I_{IN_pk} \sin^2(\omega t) \\ &= \frac{V_{IN_pk} \cdot I_{IN_pk}}{2} [1 - \cos(2\omega t)] \end{aligned} \quad (14)$$

For simplicity, assuming 100 % efficiency

$$P_{OUT} = P_{IN_avg} = \frac{V_{IN_pk} \cdot I_{IN_pk}}{2} \quad (15)$$

Substituting (14) and (15) in (13) gives

$$P_{DC} = -P_{OUT} \cos(2\omega t) \quad (16)$$

Finding the energy

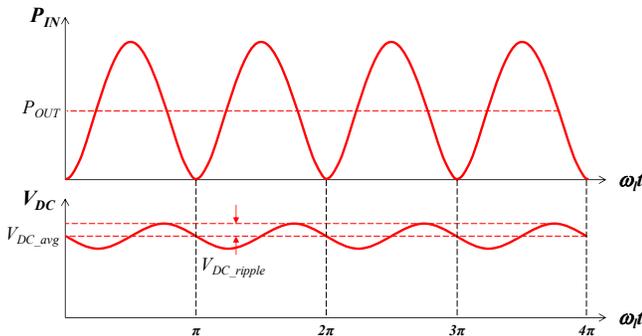


Fig. 8. The input power and DC capacitor voltage waveforms.

$$\begin{aligned} E_{DC} &= \int_0^{T_l} P_{DC} dt = E_{DC}(0) - \frac{P_{OUT} \sin(2\omega t)}{2\omega_l} \\ &= \frac{1}{2} C_{DC} \cdot V_{DC}^2 \end{aligned} \quad (17)$$

Rearranging for V_{DC} and knowing that $V_{DC}(0)$ is equal to the rms voltage [38]

$$V_{DC} = V_{DC_rms} \sqrt{1 - \frac{P_{OUT}}{\omega_l \cdot C_{DC} \cdot V_{DC_rms}^2} \sin(2\omega_l t)} \quad (18)$$

With the AC ripple being sufficiently smaller than V_{DC_rms} , the ripple amplitude can be evaluated by

$$V_{DC_ripple} \approx \frac{P_{OUT}}{2\omega_l \cdot C_{DC} \cdot V_{DC_rms}} \quad (19)$$

Therefore, the low-frequency ripple on the DC capacitor voltage is a function of the output power and the DC capacitor C_{DC} size.

D. Second Condition for Obtaining High Power Factor

From the analyses for the average DC capacitor voltage and its low frequency ripple, the pump and DC capacitors should be designed such that the minimum DC capacitor voltage is higher than the peak input voltage. That guarantees no cross-conduction occurs through the diode bridge and the pump diode, the case allowing current to flow directly from the line input to the DC capacitor, which reduces the power factor. Therefore, for a high power factor, the following condition needs to be satisfied

$$V_{DC_ripple} < V_{DC_avg} - V_{IN_pk} \quad (20)$$

Therefore, equation (20) sets a design specification for the maximum ripple on the DC capacitor voltage, and accordingly the minimum size of the DC capacitor for a given average voltage across it, where the latter is a function of the pump capacitor size.

E. Resonant Tank Maximum Current Amplitude Analysis

From the circuit operation illustrated in section II-B, it is shown that the resonant tank carries both the charge pump circuit current as well as the current to the output load. The input charge Q_{IN} stored in the charge pump capacitor is transferred to the resonant tank in interval 4, while the output charge Q_{OUT} is supplied to the load by the DC capacitor and the resonant tank in intervals 1A and 1B respectively. Accordingly, a total charge of Q_{TOT} gets stored then depleted from the resonant tank within one half of a switching cycle, as shown in Fig. 6 (shaded area), where

$$Q_{TOT} = Q_{IN} + Q_{OUT} = \int_0^{\frac{T_s}{2}} I_{RES}(t) dt \quad (21)$$

With the assumption that the resonant tank has a high-enough loaded quality factor Q_L with near-resonance operation, the resonant tank current is a sinusoidal waveform that can be described by

$$I_{RES}(t) = I_{RES_pk} \sin(\omega_s t) \quad (22)$$

Accordingly, (21) is evaluated to

$$Q_{IN} + Q_{OUT} = \frac{T_s}{\pi} I_{RES_pk} \quad (23)$$

Dividing both sides of (23) by T_s gives the average currents across the switching cycle

$$I_{IN} + I_{OUT} = \frac{I_{RES_pk}}{\pi} \quad (24)$$

Assuming I_{OUT} is constant and I_{IN} is a sinusoid in phase with the input voltage V_{IN} (unity power factor), the maximum values for both currents are evaluated to

$$I_{OUT} = \frac{P_{OUT}}{V_{OUT}} \quad (25)$$

$$I_{IN_pk} = \frac{P_{IN_pk}}{V_{IN_pk}} = \frac{2P_{IN_avg}}{V_{IN_pk}} = \frac{2P_{OUT}}{\eta \cdot V_{IN_pk}} \quad (26)$$

The maximum value for the resonant tank current amplitude across a line cycle, which occurs at the peak input voltage, is then evaluated to be

$$I_{RES_max} = \pi P_{OUT} \left(\frac{2}{\eta \cdot V_{IN_pk}} + \frac{1}{V_{OUT}} \right) \quad (27)$$

Accordingly, the charge pump circuit results in a stress in the resonant tank current, which is a function of the input voltage and output power of the converter.

IV. DESIGN

This section illustrates the design process for the proposed converter based on the analyses and design conditions covered in section III. The design criteria covers the design for a given set of specifications while satisfying the conditions for obtaining a high power factor. First, the pump capacitor needs to be large enough to store the maximum input charge from the AC mains, which is function of the output power, the peak input voltage, and the switching frequency. Second, the energy-storage DC capacitor needs to be designed such that the voltage across it, V_{DC} , is always higher than the input voltage V_{IN} across the line cycle in steady state. That ensures the diode bridge and the pump diode cannot conduct at the same time, and no direct current flow from the line input to the DC capacitor, thus providing full control on the input current, which has to flow through the pump capacitor. Lastly, the class-DE stage is designed based on the analysis in section III-A, which sets a condition for the stage voltage gain to be high (close to unity). That ideally eliminates the dependence of the input current on the DC capacitor voltage V_{DC} and the output voltage V_{OUT} , and makes it function of only the input voltage in steady state, as shown by (7).

A. Charge Pump Capacitor Design

The maximum current through the pump capacitor (averaged over a switching cycle) is equal to the peak input current, which takes place at the peak input voltage and is calculated from (26). Substituting in (7) and rearranging for C_P

$$C_P \geq \frac{2P_{OUT}}{\eta \cdot f_s \cdot V_{IN_pk}^2} \quad (28)$$

To account for the power stage gain not being one ($V_{DC} - V_{OUT} \neq 0$), the value for C_P can be adjusted to be marginally larger than that obtained from (28), while keeping in mind that a larger C_P results in higher voltage stress across C_{DC} .

B. Energy-Storage DC Capacitor Design

From (12) and (20), a specification is found for the maximum allowed ripple on the DC capacitor voltage in order to guarantee proper operation and high power factor. From (19), rearranging for C_{DC} , and considering a conservative substitution of V_{DC_avg} for V_{DC_rms} , the sizing for the DC capacitor for a given ripple is found from

$$C_{DC} \geq \frac{P_{OUT}}{2\omega_l \cdot V_{DC_ripple} \cdot V_{DC_avg}} \quad (29)$$

For applications with relaxed requirements for power factor and THD, some cross-conduction can be allowed to occur without violating the specifications, where some charge will flow directly from the input line to the DC capacitor, resulting in a short notch in the input current waveform. Thus, the sizing for both capacitors constitutes a design trade-off between circuit stresses, power quality and power density.

C. Class-DE Stage Design

The design procedure given in [14] is used for the class-DE stage design. The procedure starts by calculating the rectifier input resistance R_{REC} from the load resistance R_L through impedance transformation via the resonant rectifier as follows

$$R_{REC} = \frac{2R_L}{\pi^2} = \frac{2V_{OUT}^2}{\pi^2 \cdot P_{OUT}} \quad (30)$$

The voltage conversion ratio is equal to

$$M_V = \frac{V_{OUT}}{V_{DC_avg}} \quad (31)$$

Considering a half bridge for the inverter switching network and a class-D rectifier, the overall converter gain becomes approximately equal to the resonant tank gain. The converter loaded quality factor is then calculated using the following equation

$$Q_L = \frac{\sqrt{\frac{1}{M_V^2} - 1}}{f_n - \frac{1}{f_n}} \quad (32)$$

where f_n is the normalized switching frequency, equal to f_s/f_o , with f_o being the resonant frequency. In order to ensure the validity of the above analysis based on the FHA approach, the loaded quality factor Q_L of the resonant circuit needs to be high enough so that the current through the resonant circuit is sinusoidal. A loaded quality factor of ~ 2.5 is sufficient [14]. The normalized switching frequency is then obtained from (32). Following, and for a specified switching frequency f_s , the resonant tank component values are calculated

$$f_o = \frac{f_s}{f_n} \quad (33)$$

$$L_{RES} = \frac{Q_L \cdot R_{REC}}{\omega_o} \quad (34)$$

$$C_{RES} = \frac{1}{\omega_o \cdot Q_L \cdot R_{REC}} \quad (35)$$

It is worth mentioning that a higher Q_L value would not affect the power factor, as it guarantees a more sinusoidal resonant tank current with lower harmonic content. However, it can complicate the magnetic devices design, see (34), which is a challenge for this topology with the high current stress in the inductor, as shown by (27), and can result in low efficiency. On the other hand, a lower value for Q_L can result in mismatch between the proposed design flow and the realized values, as the current in the tank is no longer sinusoidal, and an accurate model taking into account the high-order harmonics in the resonant tank and the pump circuit is then needed, which complicates the design.

The rectifier devices stresses are calculated as follows

$$V_{D_{max}} = V_{OUT} + V_{OUT_{ripple}} \quad (36)$$

$$I_{D_{max}} = \pi I_{OUT} \quad (37)$$

while the voltage stress for the half-bridge switches is the same as the DC and pump capacitors voltage stresses, and is equal to

$$V_{S_{max}} = V_{DC_{avg}} + V_{DC_{ripple}} \quad (38)$$

and the current stress in the half bridge is equal to that of the resonant tank obtained from (27).

V. 1 MHz 50 W PROTOTYPE

This section covers the design and implementation of a 1 MHz 50 W prototype based on the analysis and design conditions obtained from sections III and IV. Starting from the design specifications, the design procedure for the presented specifications is illustrated, followed by a presentation of the simulation results used for functional verification. The resonant inductor design process is then covered, followed by a description of the implementation of the overall prototype. Eventually, experimental results are presented and compared against the analysis and circuit simulation results.

A. Design Specifications

Table I lists the specifications for the designed prototype, which is proposed for PFC rectifiers supplied from European mains for low-power range applications. A switching frequency of 1 MHz is specified for the design, as it constitutes a good trade-off between converter size and efficiency, with respect to the range of frequencies that the state-of-the-art magnetic materials allow for. As discussed in section IV-A, the gain of the class-DE stage has to be high to allow for a high power factor and low THD. A good approximation is to design for 300 V output voltage for a peak input voltage of 325 V. It is,

TABLE I. DESIGN SPECIFICATIONS.

Specifications	Input Voltage	230 V _{rms}
	Line Frequency	50 Hz
	Output Power	50 W
Design Considerations	Switching Frequency	1 MHz
	Output Voltage	300 V

however, possible to design for lower output voltages through the insertion of a high-frequency transformer in the rectifier circuit. As long as the pump capacitor is coupled to a high-frequency node with high voltage gain, inherent PFC functionality is achieved.

B. Prototype Design Procedure

From the design specifications, the design process starts by sizing the pump capacitor according to the output power, the input voltage, and switching frequency. Finding the minimum value for C_P from (28), a marginally higher value is chosen to account for the non-unity gain of the class-DE stage. The DC capacitor voltage stress is then calculated from (12). Following, the specification for the double-the-line-frequency ripple on the DC capacitor voltage is evaluated from (20) in order to guarantee high power factor. The DC capacitor is then designed for the specified low-frequency ripple according to (29). Eventually, the class-DE stage design takes place according to the procedure given in section IV-C, using (30-38), where the resonant tank current stress is calculated from (27).

It is worth noting that this design procedure is a first pass approach, as numerous issues have been neglected for simplicity, including parasitics and other non-idealities. A design decision is made for power quality, where a design iteration with respect to a larger pump capacitor and/or a larger DC capacitor can be needed. Another decision is then made on whether the design specifications with respect to power density and efficiency are met. If not, a design iteration with respect to class-DE stage design is conducted for a different output voltage and/or resonant tank quality factor.

Table II lists the obtained design values according to the specifications given in Table I, with a resonant tank quality factor of 2.4 and assuming 90 % efficiency.

C. Simulation Results

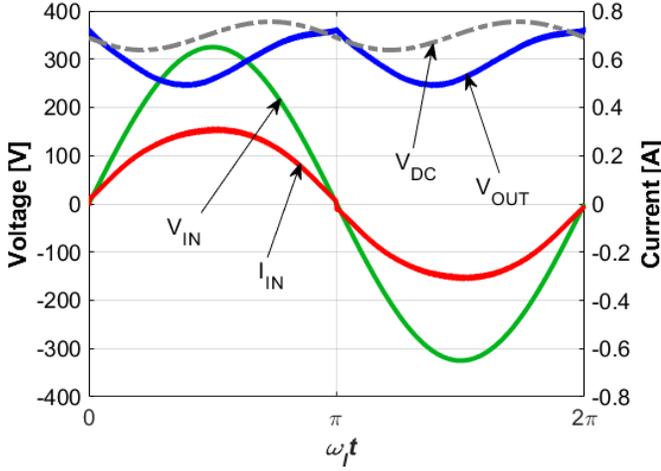
Based on the analysis and calculated values, the circuit is simulated in LTspice for functional verification. Fig. 9 shows the simulation results at full-load operation. Fig. 9 (a) shows the line-frequency waveforms at an output power of 50.6 W and an average output voltage of 300 V, with a power factor of 0.99 and a THD of 5.5 %. Fig. 9 (b) shows the switching-frequency waveforms at the peak input power ($\omega t = \pi/2, 3\pi/4$), where ZVS operation is observed on the V_{SW} waveform, which peaks to ~ 370 V, while a sinusoidal resonant tank current with a peak value of 1.6 A is observed. Thus, the results go in accordance with the analysis in section IV and the calculated values in section V-B.

D. Resonant Inductor Design

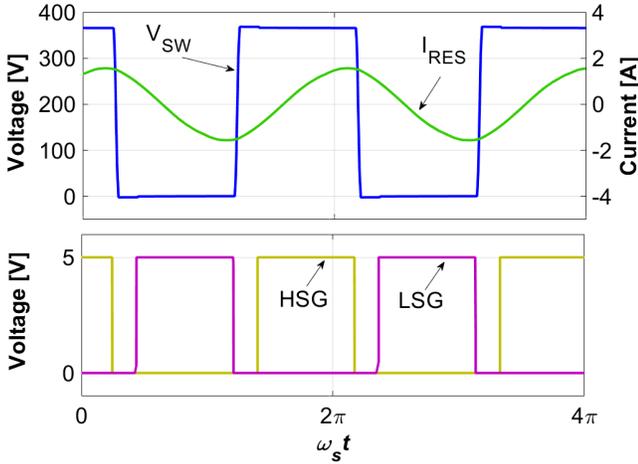
Table III summarizes the specifications for the resonant inductor design, which are obtained from the circuit analysis

TABLE II. DESIGN VALUES CALCULATED FROM CIRCUIT ANALYSIS.

Parameter	Calculated
C_P (min.)	1.05 nF
$V_{DC_{avg}}$	349 V
C_{DC} (min.)	9.6 μ F
L_{RES}	158 μ H
C_{RES}	206 pF
$I_{RES_{max}}$	1.6 A



(a) Line-frequency waveforms.



(b) Switching-frequency waveforms.

Fig. 9. Simulation results at full-load operation.

and verified with simulation results, where the peak current amplitude and the inductance specifications are obtained from (27) and (34) respectively.

When handling high-frequency AC currents, a key factor to the inductor design is choosing the right core material. Several magnetic materials [39][40] are investigated and compared in terms of core losses at 1 MHz, as shown in Fig. 10, where the 3F46 material is chosen, as it shows the lowest core losses at the design operating conditions. The following equation is used to estimate the inductor core losses. The peak flux density in the core can be calculated from [38]

$$B_{max} = \frac{1}{N} \cdot \frac{I_{RES_max} \cdot L}{A_e} \quad (39)$$

where N is the number of turns, L is the inductance, and A_e is the effective core cross-sectional area. Considering that the core

TABLE III. RESONANT INDUCTOR DESIGN SPECIFICATIONS.

Parameter	Specification
Inductance	158 μ H
Current Frequency	1 MHz sinusoid
Current Peak Amplitude	1.6 A

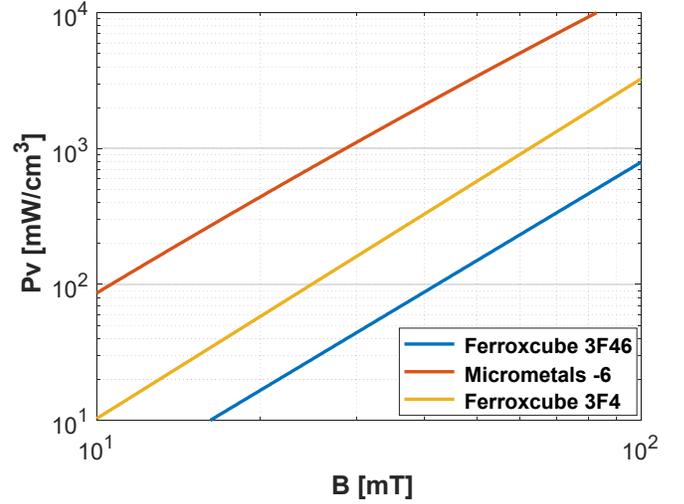


Fig. 10. Core power-loss density (P_v) vs. magnetic flux density (B) for different magnetic materials at 1 MHz.

losses are a function of the peak flux density for a chosen material, the losses for a given number of turns and core size can be estimated. The following calculation of the DC resistance of the windings gives an estimate of the winding losses. The total cross-sectional area of the windings A_c is calculated from

$$A_c = n_{wires} \cdot \pi \cdot r_{wire}^2 \quad (40)$$

where n_{wires} is the number of strands of Litz wire and r_{wire} is the wire radius. The DC resistance is then calculated from

$$R_{dc} = \rho_{cu} \cdot \frac{MLT \cdot N}{A_c} \quad (41)$$

where ρ_{cu} is the copper resistivity and MLT is the mean length of turn. For an EFD 25/13/9 core size, with two parallel layers of 20 x 0.05 mm Litz wire, the DC resistance is calculated to 8.6 m Ω · N.

Next, the AC resistance of the windings is calculated. The skin effect is negligible when using Litz wire at 1 MHz, but the proximity effect can have a significant influence on the closely wound wires. Modelling the AC resistance to be three times larger than the DC resistance (based on empirical tuning), the winding losses are estimated to

$$P_{cu} = R_{ac} \cdot I_{rms}^2 = 3 \cdot R_{dc} \cdot \frac{I_{RES_max}^2}{2} = 33 \text{ mW} \cdot N \quad (42)$$

Fig. 11 shows the inductor losses vs. number of turns. Based on these estimates, the inductor is designed with 52 turns, which helps to distribute the losses evenly between the core and the winding, and results in acceptable total losses. An airgap of 1.2 mm, distributed across the three legs of the core, adjusted the desired inductance. Fig. 12 shows the small signal characteristics of the implemented inductor measured using a 40 Hz – 110 MHz precision impedance analyzer (Agilent Technologies 4294A). At 1 MHz, an inductance of 152.3 μ H and an ESR of 2.5 Ω are obtained, corresponding to a Q -value of 380 and 3.2 W of losses when excited with a 1.6 A sinusoidal current. This is a first-pass approach for the resonant inductor design, which assumes room temperature for inductor core and

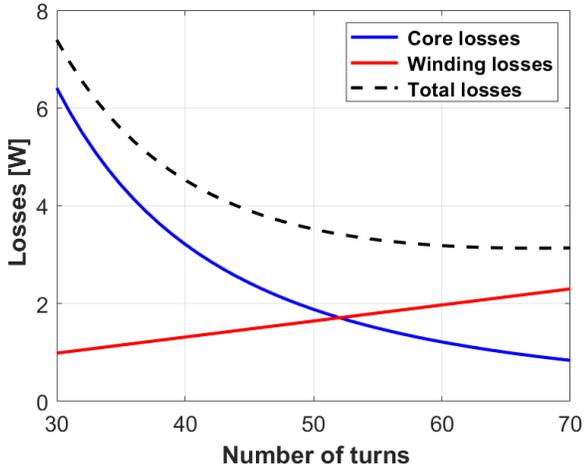


Fig. 11. Inductor losses vs. number of turns.

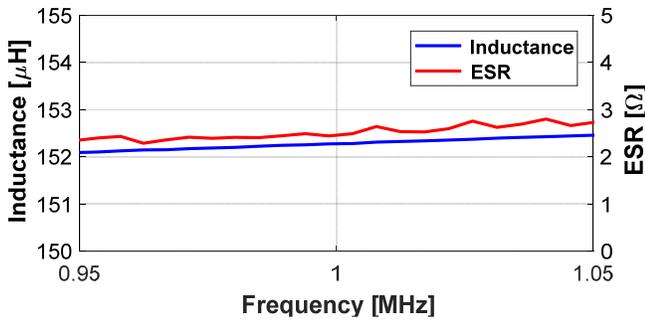


Fig. 12. Resonant inductor inductance and ESR measurements.

windings, and does not take into account the impact of the non-ideal field distribution in the core and the windings self-heating.

E. Implementation

Fig. 13 shows a photograph of the implemented prototype power stage. The converter is implemented and assembled on a two-layer printed circuit board (PCB). Because of the charge-pump circuit operation, a high-frequency AC current runs through the input bridge, which is implemented using four fast-recovery diodes. With respect to selection of switches, Fig. 14 shows a comparison based on datasheet parameters between the best in-class switches figures of merit [41]-[44], where gallium nitride (GaN) FETs show superior performance compared to the silicon superjunction and silicon carbide (SiC) counterparts.

Device 6 in Fig. 14 is used for the inverter design. The switches gate-driving circuit is comprised of a digital isolator (Si8610BC by Silicon Labs) and a gate driver (UCC27611 by Texas Instruments) for each of the high-side and low-side switches. For the high-side driver supply, a bootstrap network of a diode (GB01SLT06-214, SiC Schottky) and a capacitor (1 μ F, ceramic X7R) is used, in addition to a peripheral solution comprised of isolated power supplies (MTE1S0506MC by Murata), and both circuits are equally operational.

In order to control noise coupling from the power loop to gate-drive loop, the gate driver packages are placed as close as possible to the devices gate terminals to minimize the gate parasitic inductance. Another layout consideration taken is the separation of the source terminal to the driving and power loops

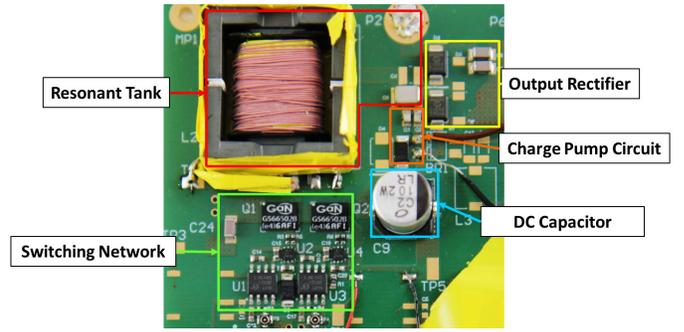


Fig. 13. Prototype power stage.

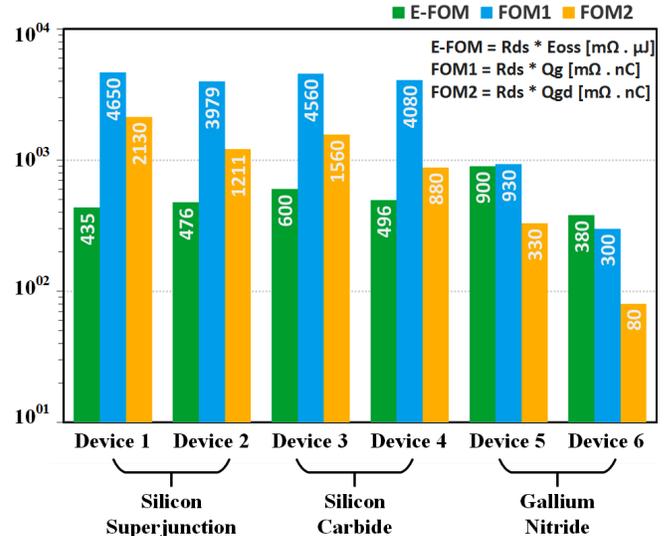


Fig. 14. Summary of best in-class switches' figures of merit.

in a star-connected fashion. That helps alleviate the gate ringing resulting from the common-source inductance. As the selected gate driver offers separate source/sink outputs, a separate 0402 SMD gate resistor is added to each path to control the miller effect. A source gate resistor of 30 Ω is chosen to reduce the turn-on dv/dt slew rate and limit gate oscillation. On the other hand, a sink gate resistor of 4 Ω is chosen to provide a strong pull-down during turn-off, hence preventing the false turn-on events with the low threshold voltage of GaN FETs.

For the rectifier side, SiC Schottky diodes are employed, as they show higher efficiency compared to the silicon high-

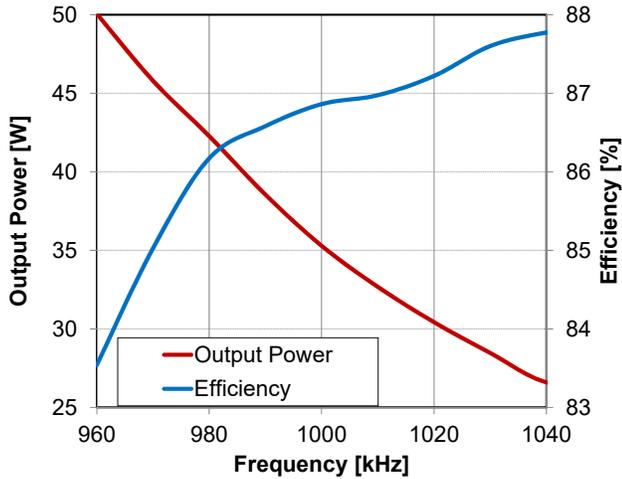
TABLE IV. PROTOTYPE POWER-STAGE BOM.

Component	Calculated	Simulated	Prototype	Type
L_{IN}		100 μ H	100 μ H / 0.5 A	Inductor
C_{IN}		30 nF	2 * 15 nF / 450 V	Ceramic (C0G)
Diode Bridge			4 * ESH1GM RSG	Si Fast Recovery
C_{DC}	9.6 μ F	10 μ F	1 * 10 μ F / 450 V 3 * 0.1 μ F / 450 V	Electrolytic Ceramic (C0G)
D_P			RF201LAM4S	Si Fast Recovery
C_P	1.05 nF	1.3 nF	2 * 680 pF / 500 V	Ceramic (C0G)
Q_{HS}, Q_{LS}			GS66502B	GaN Switches
L_{RES}	158 μ H	158 μ H	152 μ H / 1.6 A	Custom design
C_{RES}	206 pF	200 pF	220 pF / 3 kV	Ceramic (C0G)
D_{R1}, D_{R2}			GB01SLT06-214	SiC Schottky
C_{OUT}		30 nF	2 * 15 nF / 450 V	Ceramic (C0G)

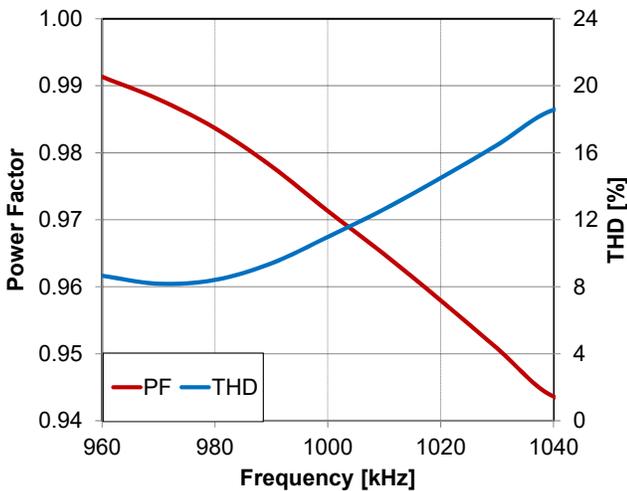
voltage counterparts. Table IV shows a breakdown of the incorporated power stage bill-of-materials (BoM) for the proposed design.

F. Experimental Results

The converter is tested for operation from 230 V_{rms} at switching frequencies between 0.96 MHz and 1.04 MHz, which are within the inductive mode of operation for the resonant converter, and accordingly, soft-switching operation can be achieved. Fig. 15 (a) shows the output power and efficiency across the operational frequency range for the proposed converter. Results illustrate that an output power ranging from 26.6 to 50 W is obtained through frequency modulation, while achieving a peak efficiency of 87.8 %. Fig. 15 (b) shows the power quality results. The converter achieves a peak power factor of 0.99 and minimum THD of 8.6 %, at an output power of 50 W and switching frequency of 0.96 MHz. Results show that operation at lower frequencies, close to resonance with higher gain, achieves higher power factor and lower THD, which goes in accordance with the analysis given in section III.



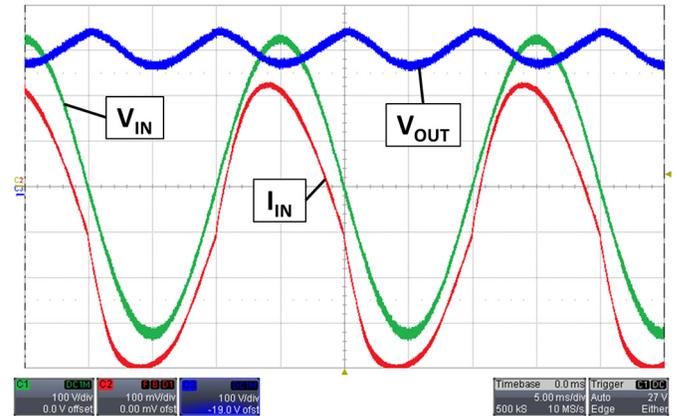
(a) Output power and efficiency.



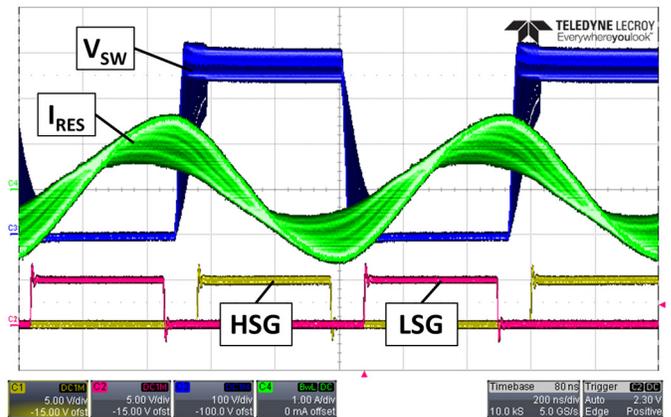
(b) Power factor and THD.

Fig. 15. Obtained prototype measurements across operational frequency range.

Fig. 16 shows scope captures for the implemented prototype waveforms at full-load operation. Fig. 16 (a) shows the low frequency waveforms, including the input voltage and current as well as the output voltage. The input voltage is displayed using a high-voltage differential probe (Testec SI 9001), while the input current is measured using a 50 MHz current probe (Hioki CT6700), and the output voltage is measured using a 500 MHz 10x voltage probe with 9 pF capacitance. The figure shows an almost-sinusoidal input current with a phase difference of 5.7° with the input voltage, and an average output voltage of 300 V, which matches the circuit analysis and the simulation results shown in Fig. 9 (a). A 100 Hz ripple of 40 V is measured on the output voltage, which is about 13 % of the DC voltage and can be reduced through the incorporation of a larger DC capacitor. Fig. 16 (b) shows a scope capture for the high-frequency signals at full-load operation. The capture is taken with infinite persistence to visualize the variations across the input voltage range, which is the low-frequency ripple on the DC capacitor voltage. The resonant circuit current I_{RES} is measured using a 50 MHz current probe (LeCroy AP015). The current is seen to be sinusoidal, thus ensuring the validity of the design process given in section IV-C, which is based on the FHA approach. The resonant tank current peaking effect matches the 1.6 A value obtained from the analysis in section III-E and the simulations results shown in Fig. 9 (b). The



(a) Line-frequency waveforms (V_{IN} 100 V/div, I_{IN} 100 mA/div, V_{OUT} 100 V/div with 5 ms/div).



(b) Switching-frequency waveforms in infinite-persistence mode (V_{SW} 100 V/div, I_{RES} 1 A/div, HSG/LSG 5 V/div with 200 ns/div).

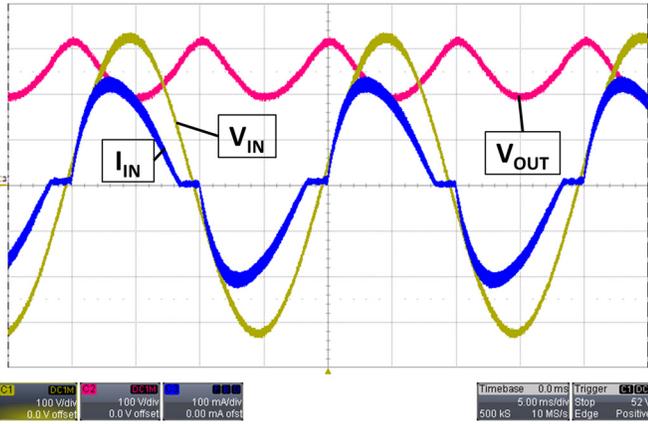
Fig. 16. Scope images for the implemented prototype waveforms at full-load operation.

switching node voltage waveform V_{SW} is measured using a 500 MHz 10x voltage probe with 9 pF capacitance and shows that soft switching is obtained across the input voltage range.

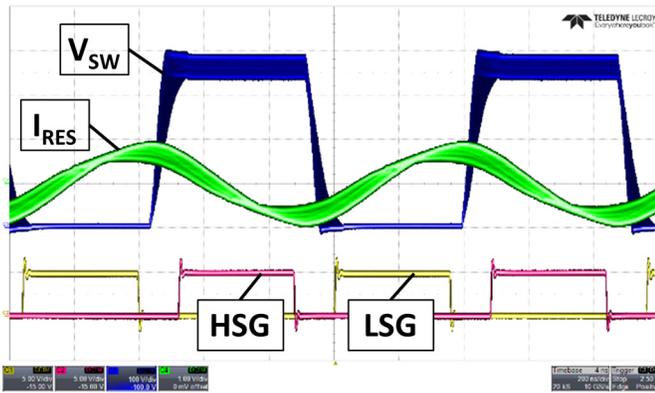
Fig. 17 shows scope captures for the implemented prototype waveforms at half-load operation. As expected, operation at higher frequencies, away from resonance, results in lower power factor and higher THD, as observed from Fig. 17 (a), which are quantified in Fig. 15 (b). On the other hand, Fig. 17 (b) shows a reduced resonant tank current stress, resulting in higher efficiency at lower loads, as shown by Fig. 15 (a).

The driving signals to the switches are synchronized with the same duty cycle and extended dead time. For the full-load operation shown in Fig. 16 (b), the driving signals duty cycle is adjusted and fixed at 37 %, where ZVS is achieved and the average devices temperature is minimal, resulting in a dead time of 135 ns. Considering that the input voltage for the half-bridge is not dc, where it has the double-the-line-frequency ripple on top of the average DC capacitor voltage, see (38), full ZVS is achieved for the mid-range of V_{DC} . Whereas partial soft switching is observed at the lower end of that range, as longer dead time is needed. On the other hand, a short interval with GaN-FETs reverse conduction is noticed at the higher end of the range, for which a shorter dead time can achieve full ZVS.

Considering that the GaN device has zero reverse recovery charge (Q_{RR}), the worst-case power loss due to reverse



(a) Line-frequency waveforms (V_{IN} 100 V/div, I_{IN} 100 mA/div, V_{OUT} 100 V/div with 5 ms/div).



(b) Switching-frequency waveforms in infinite-persistence mode (V_{SW} 100 V/div, I_{RES} 1 A/div, HSG/LSG 5 V/div with 200 ns/div).

Fig. 17. Scope images for the implemented prototype waveforms at half-load operation.

conduction can be estimated as follows. Fig. 18 shows measurement results for the reverse conduction characteristics of the employed GaN device across different temperatures with zero gate-source voltage (obtained using a Keysight B1505A curve tracer). Assuming an average reverse current I_{rev} equal to the maximum resonant tank current, 1.6 A, a voltage drop of about 2.2 V is developed across the GaN device (V_{rev}). From Fig. 16 (b), a reverse conduction interval T_{rev} of 80 ns is observed for each device. The power loss due to reverse conduction P_{rev} is then calculated to

$$P_{rev} = 2 \cdot I_{rev} \cdot V_{rev} \cdot T_{rev} \cdot f_s = 0.54 W \quad (43)$$

Considering that reverse conduction occurs only for the high end of the voltage range across the half-bridge, the value obtained from (43) represents a pessimistic case that assumes that reverse conduction occurs across the entirety of the line-cycle, with the same reverse current. Accordingly, the actual contribution of the reverse conduction loss to the total power loss is of less concern.

For achieving the best efficiency across line and load ranges, an adaptive dead-time adjustment circuit can be incorporated [45]. A less-effective but lower-cost method to alleviate that effect is through the incorporation of a larger capacitor C_{DC} , which results in reduced ripple across the DC capacitor and half-bridge, see (19).

Fig. 19 shows the input current harmonics distribution at full and half-load operations, where THD figures of 8.6 % and 17.4 % are measured respectively. Since one of the potential applications for the proposed converter is the rectifier stage in LED drivers, the figure illustrates the harmonics magnitudes against IEC 61000-3-2 standard class-C device limits [1][2], where it is shown that the measured harmonics magnitudes are well-within the limits set by the standard.

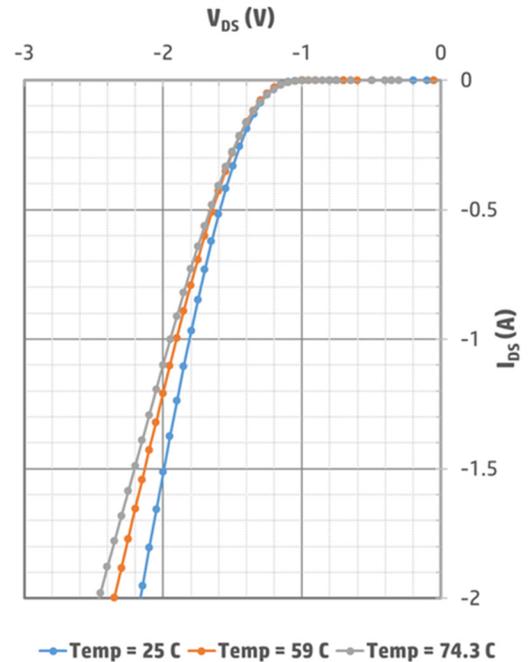


Fig. 18. Measured GaN device reverse characteristics across different temperatures for $V_{GS} = 0$ V.

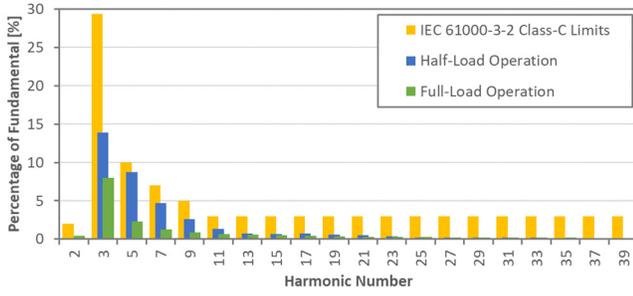


Fig. 19. Input Current harmonics distribution.

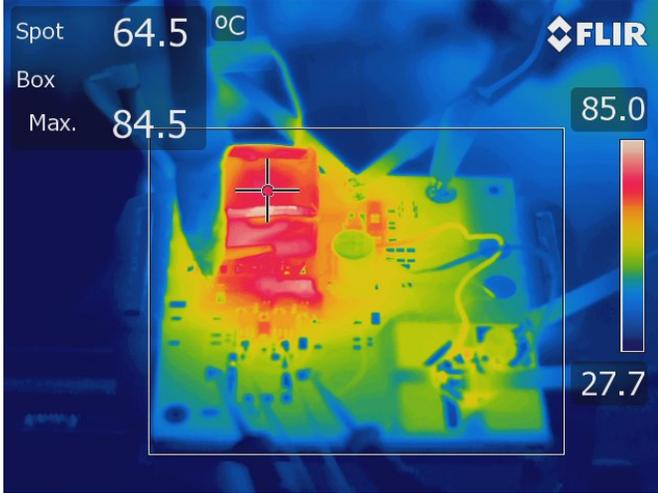


Fig. 20. Thermal image for converter at full-load.

Fig. 20 shows a thermal photograph for the prototype under full-load operation, where the inductor windings are the hottest element in the circuit, with a maximum temperature of 84.5 °C (with airflow).

Table V shows a comparison of the proposed work with several reported solutions for the PFC front-end in single-phase offline converters for low-power applications. While the majority of the reported converters operate at low frequencies to limit the switching losses, the proposed converter operates at 1 MHz with soft switching. The proposed converter also has the

potential for operation at higher frequencies, as all of the circuit components scale with frequency (other than the DC energy-storage capacitor size, which is dictated by the 50/60 Hz standard line frequency). In addition, different PFC control techniques are employed in the reported solutions, while the proposed converter achieves PFC inherently, where the circuit overhead is only an extra diode and a capacitor. That simplifies the design and provides freedom from the limited frequency range for available PFC controllers, which is another factor allowing for high-frequency operation. The output-voltage control can be achieved with switching frequency modulation and/or burst-mode operation, depending on the requirements of the following DC-DC stage, where results has shown that high power factor and low THD are achieved across the load range.

Similar to most of the reported solutions, the proposed structure is compatible with universal input mains, as the charge pump circuit is able to achieve inherent PFC regulation, regardless of the input voltage, where the analysis and principle of operation of the pump circuit is the same across any input voltage that can range between 85 – 265 V_{rms} . However, in order to achieve the same output power across both ends of the input voltage range, two aspects need to be taken into consideration. First, the resonant tank needs to be designed for the worst-case conditions, with respect to the input rms voltage and output power. More specifically, the resonant tank inductor needs to be designed to handle the worst-case current, which comes with the minimum input rms voltage and maximum output power, as can be seen from (27). Second, in order to satisfy the first condition for obtaining high power factor, given in section III-A, which entitles the class-DE stage to operate near resonance with a near-unity gain, the output voltage will change across the range of the input rms voltage. That in turn will require the following DC-DC stage to have a wide-input line regulation capability. Fig. 21 shows a scope capture for the implemented prototype line-frequency waveforms with 120 V_{rms} input, delivering an output power of 12.8 W, a power factor of 0.99, and a THD of 9.1 % for an average output voltage of 179 V with 20 V low-frequency ripple. Fig. 22 shows the input current harmonics magnitudes for 120 and 230 V_{rms} inputs. The figures show that high power factor and low THD are achieved with different input voltages, as the charge pump circuit works in the same manner. Yet, to achieve the full-load operation for the low

TABLE V. COMPARISON WITH REPORTED LITERATURE.

Reference	[4]	[5]	[8]	[10]	[11]	[12]	[13]	This Work
Year	2011	2013	2016	2013	2017	2011	2016	2019
Topology	Buck	Buck	Boost	Buck-Boost	Flyback	SEPIC	SEPIC	Resonant
Aux. Circuits	None	Switch and 2 diodes	None	None	None	None	None	Capacitor and diode
Mains Compatibility	Universal	Universal	Universal	Universal	Universal	100 V_{rms}	220 V_{rms}	Universal
Output Power [W]	100	100	150	12	60	65	21	50
Output voltage [V]	90	80	250 / 450	112 / 350	24	48	30	300
Power Factor	0.98	0.96	---	0.98	0.99	---	0.99	0.99
THD [%]	---	18	5	8.7	8	1.6	12.6	8.6
Efficiency [%]	96.5	95.5	95	88	90.8	92.8	91.6	88
Semiconductors	(switches)	Si	Si	Si	Si	Si	Si	GaN
	(diodes)	Si	Si	SiC	Si	Si	Si	SiC
Switching freq. [kHz]	25 – 425	---	125 – 1000	65	45 – 300	50	50	1000
PFC Control	Constant ON-time	Constant ON-time	PWM / PFM	PWM	Variable ON-time	PWM	PWM	Inherent
Output Voltage Control	Constant ON-time	Constant ON-time	PWM / PFM	PWM	Variable ON-time	PWM	PWM	PFM

line voltage, the resonant tank needs to be redesigned for the high current that will result from (27), while the current prototype was designed for the 230 V_{rms} mains input as given in the design specifications in Table I.

Even though the inherently achieved power factor and THD figures fall within the reported ranges, it is noted that the proposed solution has lower efficiency compared to several reported ones. This comes from two main factors. The first being the added stress on the resonant-tank, as the pump circuit operation entitles the resonant tank to store the energy from the input line as well as the energy to the load every switching cycle, which is the main reason for the current peaking effect analyzed in section III-E and evaluated by (27). With the employed high-frequency magnetic material for the given operation frequency range, the core losses scale with $\sim f_s^{2.5} \cdot I_{RES}^{2.34}$ [39], while the winding losses scale with $\sim f_s \cdot I_{RES}^2$. Accordingly, in addition to the high frequency design, the current stress in the resonant tank results in high losses in the resonant inductor. A way to alleviate that effect is through the incorporation of a larger core or a better-suited magnetic material. The second factor is the partial soft switching of the converter with the implemented fixed dead time, which can be alleviated through the incorporation of an adaptive dead-time adjustment technique and/or a larger energy-storage capacitor C_{DC} . On the other hand, a lower frequency design would mitigate both effects while sacrificing the power density. These factors together constitute a trade-off between efficiency, power density and power quality (power factor and THD).

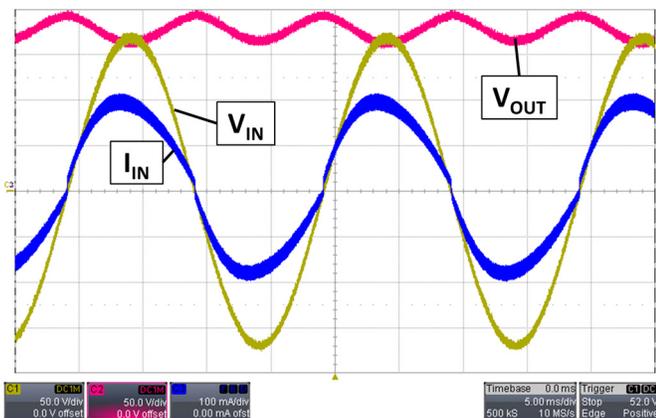


Fig. 21. Line-frequency waveforms for 120 V_{rms} input (V_{IN} 50 V/div, I_{IN} 100 mA/div, V_{OUT} 50 V/div with 5 ms/div).

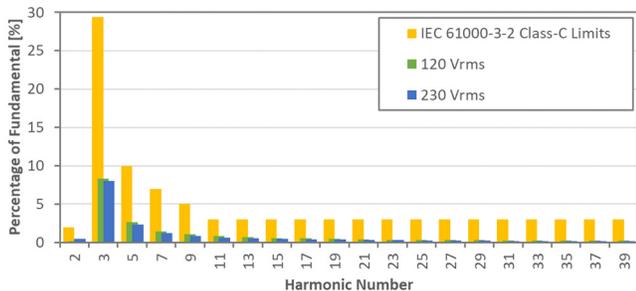


Fig. 22. Input current harmonics distribution for different line voltages against the standard.

It is worth mentioning that while the proposed architecture is tested and implemented with a series-resonant tank, the charge-pump circuit is functional with other arrangements for the resonant tank, including the parallel-resonant, LLC, and LCC circuits. In addition, resonant converters allow for galvanic isolation through the addition of a high-frequency transformer to the resonant tank. These features allow for different output voltages that can be higher or lower than the input voltage, which gives additional flexibility for the following DC-DC stage design based on the application and system requirements.

VI. CONCLUSION

The analysis and design flow of a charge-pump-based resonant PFC rectifier for low-power single-phase offline converters is presented. The system incorporates an input bridge, a charge-pump circuit, a DC energy-storage capacitor, and a class-DE resonant converter. Although the circuit is subject for additional stresses from the incorporation of the charge pump circuit, which result in added losses in the resonant tank, the converter achieves PFC functionality inherently. At the same time, the operation is based on soft switching, allowing for increased switching frequencies with reduced switching losses. A prototype is built and tested to validate the presented analysis and design procedure. The prototype achieves up to 50 W of power, with a power factor of 0.99, a THD of 8.6 %, and an efficiency of up to 88 %, with harmonic magnitudes well-within the IEC 61000-3-2 standard class-C device limits, making it suitable for use as the rectifier stage in LED drivers.

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