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A Time-Based Control Scheme for Power Factor Correction Boost Converter

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Abstract—A time-based control scheme for the power factor correction (PFC) boost rectifier is presented. Average-current-mode control in time is achieved using time-based compensators performing a proportional-integral control action. The controller is fully CMOS compatible, which allows for monolithic integration with the power switching elements. The time-based controller also eliminates the need for the pulse-width-modulation (PWM) generator required in the conventional analog and digital controllers. The proposed controller draws a sinusoidal input current in phase with the input mains voltage and delivers a dc output voltage. The control scheme model is verified on a 600 W PFC boost converter, achieving a power factor of 0.99 and a 400 V dc output from a 230 V_{rms} 50 Hz input voltage.

Index Terms—AC-DC converter, time-based control, power factor correction, voltage-controlled oscillator, boost converter

I. INTRODUCTION

With the recent advancements in industrial electronics that aim for added performance, reliability and portability, a great demand for new technologies in power supplies becomes persistent. Research is taking steps towards highly integrated systems in the form of the Power-System-in-Package (PSiP) and the more compact Power-Supply-on-Chip (PwrSoC), where application-specific integrated circuits (ASICs) are combined with power devices to produce highly integrated power supplies with high power densities and reduced physical dimensions [1]. While different technologies advanced the power stage miniaturization with the design of power converters switching in the very-high frequency (VHF) range [2][3], new technologies in controller designs are needed to cope with the miniaturization trend. One application with such potential is the power factor correction (PFC) controllers.

A high power factor is generally required in a power supply system connected to the grid. In case the power grid is loaded by a nonlinear load, e.g. switching converter, the current drawn by the load is interrupted by the switching action, which introduces harmonics in the current waveform with frequencies that are multiples of the input line frequency (in

addition to the switching frequency harmonics). That harmonic distortion reduces the average power transferred to the load, as the average power is the product of the fundamental components of the input current and voltage. In addition, the current harmonics contaminate the grid, affecting the power quality for other grid-connected loads. Accordingly, international standards such as the IEEE/ANSI 519 [4] and the IEC 61000-3-2 [5] set limits on the power factor and input current harmonic magnitudes to reduce the mains voltage distortion. PFC converters bring the power factor of a power circuit closer to unity by making the load appearing more resistive to the grid, thus achieving a close-to-sinusoidal input current that is proportional to and in phase with the sinusoidal input voltage. As a result, PFC rectifiers and their controllers are incorporated in most offline (grid-interfacing) power converters.

Over the past few years, signal processing in the time domain was introduced for several applications [6][7]. Time-based signal processing utilizes the voltage-to-time properties of ring oscillators and delay lines to synthesize gain blocks, integrators, and differentiators. It is finding new applications to improve performance and reduce die area and power consumption, as it copes better with the technology scaling that comes with increased speeds and reduced power supplies. One application reported in prior art is time-based controllers for DC-DC buck converters [8]–[10], where a time-based control loop compares the output voltage with a reference, and provides regulation across line and load disturbances.

This work investigates the incorporation of time-based control in an AC-DC PFC boost converter, where an additional control loop is included to regulate the input current to follow the input voltage. A time-based control scheme is proposed where two time-based control loops are combined, with a similar function to the conventional average-current-mode controller (ACMC). The presented scheme model is verified on a 600 W PFC boost converter and achieves a power factor of 0.99 with a constant output voltage of 400 V.

This paper is organized as follows. Section II describes the ACMC controller using traditional analog signal processing techniques. The proposed time-based controller is introduced in section III. Section IV covers the design process of the presented controller. Model results are then illustrated in

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section V. Eventually, conclusion is provided in section VI.

II. AVERAGE-CURRENT-MODE CONTROLLER

To ensure that a power supply appears resistive to the grid, a controlled rectifier is implemented to ensure both a stable dc output voltage and a sinusoidal input current in phase with the grid voltage. There are several ways of controlling a power circuit to ensure a resistive grid-load. PFC controllers operating at a fixed frequency and varying duty-cycle are the most commonly employed controllers, thanks to their simple design and high power factor. One such control method is the Average Current Mode Control (ACMC) [11]. Fig. 1 shows a block diagram of the ACMC controller incorporated in a boost converter, one of the most common topologies for PFC applications.

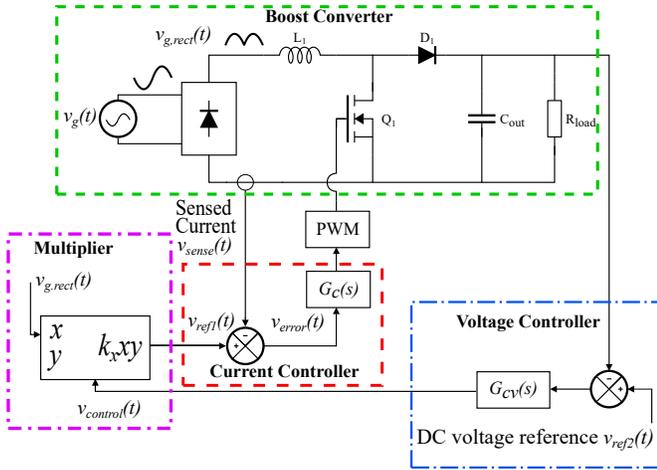


Fig. 1: Average-current-mode control of a boost PFC converter [11].

The grid voltage, $v_g(t)$, is rectified using a full wave bridge rectifier, then fed to a switch-mode power supply (SMPS), in this case a boost converter. The boost converter has a conversion ratio, $M(t)$, ranging from one to infinity, ideally, which is essential to perform PFC. For the input current to follow the input voltage, the conversion ratio of the converter moves from a minimum level, M_{min} , to infinity, as illustrated in fig. 2.

The controller seen in fig. 1 is comprised of two control loops. A current controller, $G_C(s)$, which controls the shape of the input current, and a voltage controller, $G_{CV}(s)$, controlling the output voltage. The current controller takes a scaled version of the input voltage as a reference and compares it with the sensed input current. The voltage controller compares the output voltage with a reference voltage and generates a control signal, $v_{control}(t)$. This control signal is fed into a multiplier which multiplies the control signal by the input voltage and divides the quantity by the peak voltage squared of the input voltage, $V_{g,peak}^2$, to ensure correct power delivery. This is shown in (1), where K_v is a factor which is dimensioned to the operating ranges of the input and output voltages to ensure

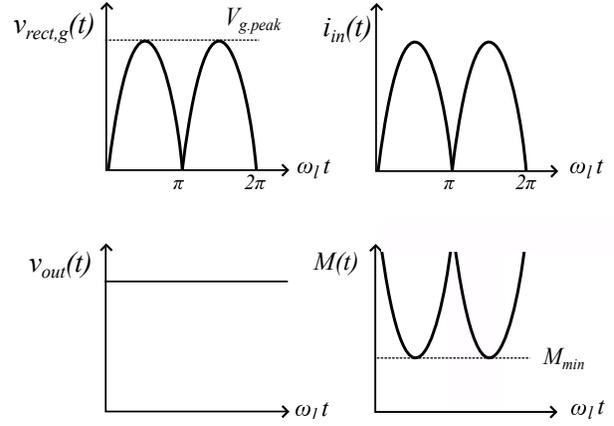


Fig. 2: Voltage and current waveforms of the boost PFC as well as conversion ratio $M(t)$ [11].

proper operation in the case of the minimum input ac voltage at the max output power.

$$v_{ref1}(t) = \frac{K_v \cdot v_{g,rect}(t) \cdot v_{control}(t)}{V_{g,peak}^2} \quad (1)$$

The two controllers together set a control voltage to a pulse width modulation (PWM) generator that then controls the switch Q_1 , such that the load seen by the grid is ideally resistive. These controllers are traditionally implemented using analog compensators. An analog proportional-integrating (PI) controller is shown in fig. 3. While well-known and easy to implement, analog controllers constitute a challenge for integration on an integrated circuit, due to the need for large passives, which increases the total area and price of the circuit. In many cases, they are employed as discrete passives, thus increasing the cost and bill of materials, as well as consuming area on the board. Furthermore, the generation of a PWM signal consumes a large die area if implemented monolithically. Additionally, analog compensators use voltage as the reference, whereas the trend of scaling transistor feature sizes continues, and so decreases the voltage supplies. This in turns results in less resolution on the controller, as the available reference range is reduced.

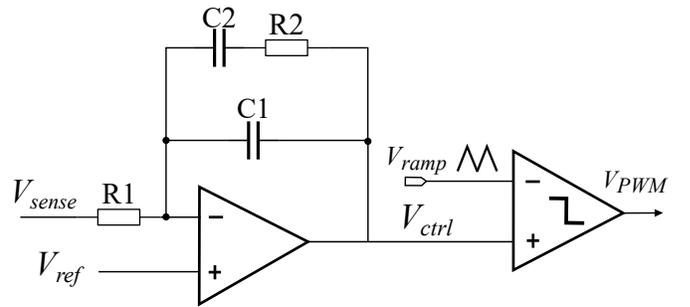


Fig. 3: Traditional analog PI controller.

On the other hand, digital controllers are incorporated in some cases. Fig. 4 shows the block diagram of a digital PI

controller. The error voltage is converted from analog to digital using an analog-to-digital converter (ADC). This digitized voltage is processed through digital compensation, where the proportional and integral control portions of the analog compensator are implemented using a gain scaler and a digital accumulator. A digital PWM (DPWM) then conducts the digital-to-time conversion and generates a duty-cycle signal proportional to the error voltage. While digital controllers can operate at a high switching frequency and eliminate the need for large passives, they produce additional ripples on the output voltage, which result from the quantization error introduced by the ADC and DPWM blocks. Reducing the ripple requires high precision ADC and DPWM blocks, thus adding complexity and increasing power consumption.

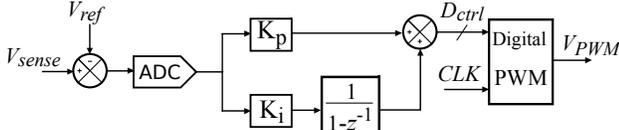


Fig. 4: Block diagram of a digital PI controller.

III. TIME-BASED CONTROLLER

Time-based control is based on signal processing in the time domain [6] [7], where the error voltage is converted to a time signal using a voltage-to-time converter and the output is processed by a time-based compensator. The output of the compensator is a pulse-width modulated signal. Compared to the digital controller, time-based control eliminates the quantization error introduced by the ADC and DPWM blocks, thus behaving like a linear system in steady state, and achieving a small voltage ripple similar to the analog controller. Compared to both analog and digital controllers, the time-based controller eliminates the need for a PWM generator, as the PWM signal is inherently generated in time-based signal processing. Furthermore, the needs for large passives, high gain-bandwidth (GBW) error amplifiers, high-speed comparators, and ADC are obviated. Time-based control also enables converters operation at the VHF range (30–300 MHz), which is a main trend in switch-mode power converters design, in addition to being fully CMOS compatible, where it takes advantage of technology scaling and low feature-size devices, which allows for monolithic integration with the power switching devices. That makes it a main candidate for controller design towards the highly integrated PSiP and PwrSoC converters.

A time-based PI controller is shown in fig. 5. A voltage-controlled oscillator (VCO) converts the error voltage into frequency, and as phase is the integral of frequency, the VCO acts as a voltage-to-phase integrator, thus providing both voltage-to-time conversion and integration functions. The proportional portion is implemented using a voltage-controlled delay line (VCDL) that incorporates a chain of tunable delay cells, providing voltage-to-time conversion with proportional function, as a time delay corresponds to a voltage gain in the voltage domain. A phase detector (PD) compares the phase of

the VCDL output signal with that of a reference clock that is generated from a replica VCO with an input bias voltage that sets the free-running frequency of the PWM signal. That frequency is designed to be equal to the switching frequency of the converter. The output of the PD is a PWM signal equivalent to the control signal in time domain.

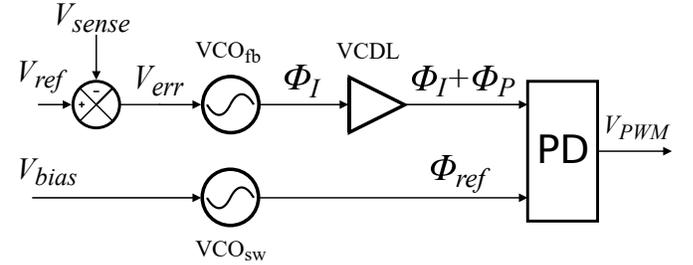


Fig. 5: Block diagram of a time based PI controller.

While prior art reported time-based controllers for DC-DC buck converters with a single control loop to regulate the output voltage [8]–[10], this work investigates the employment of time-based controllers for an AC-DC boost PFC converter, where an additional control loop is added to control the input current, and the two time-based loops are combined to achieve a sinusoidal input current in phase with the input voltage, as well as a dc output voltage.

A. Proposed Time-Based Control Scheme

Fig. 6 shows a block diagram of the proposed time-based ACMC PFC rectifier, with the two control loops synthesized in the time-domain, and combined using the multiplier circuit shown. By comparing this control scheme with the conventional controller shown in fig. 1, it is seen that each control loop is replaced by a time-based equivalent comprised of two VCOs, a VCDL, and a PD. It is also observed that the time-based controller eliminates the need for the PWM generator block, thanks to the inherent PWM generation capability.

B. Voltage-Frequency and Gain-Delay Conversions

Fig. 7 shows a schematic for the VCO and VCDL circuits, which is functionally identical to the blocks shown in fig. 6. It is possible to design the transfer functions using conventional methods and then find the corresponding parameters for a time-based controller. Within the linear operation range of the VCO, the relationship between voltage and frequency is

$$\omega_{out}(t) = \omega_{fr} + K_{vco} \cdot V_{vco}(t) \quad (2)$$

where K_{vco} is the voltage-to-frequency gain, $V_{vco}(t)$ is the control voltage of the oscillator, ω_{fr} is the free running frequency of the reference VCO, and $\omega_{out}(t)$ is the output frequency of the VCO. The integral gain K_i of a conventional PID controller is identical with K_{vco} (Hz/V) [9].

$$K_i = K_{vco} \quad (3)$$

The switching frequency of the power converter is set by ω_{fr} .

$$f_{sw} = \frac{\omega_{fr}}{2\pi} \quad (4)$$

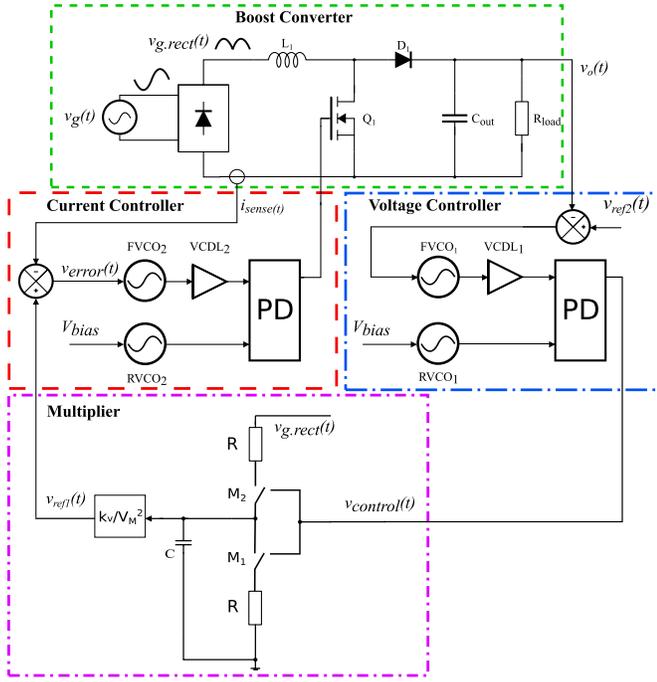


Fig. 6: Time-based average-current-mode control for a PFC boost converter.

The proportional gain K_p is realized as the control gain of the VCDL, $K_{vc dl}$ (s/V).

$$K_p = K_{vc dl} \cdot 2\pi \cdot f_{sw} \quad (5)$$

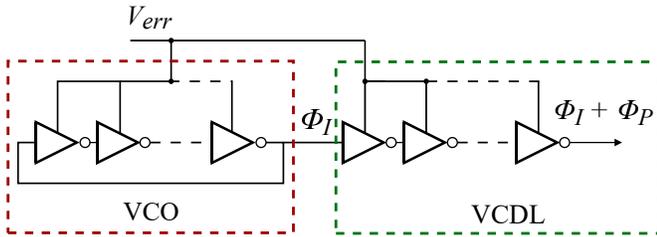


Fig. 7: Schematic for the VCO and VCDL blocks.

In order to ensure linearity, the gains of the VCOs and VCDLs must be operating in their linear region. In previous work [12], a low gain, linear oscillator and delay line is implemented by varying the bias on a varactor at the output of the inverter cells.

C. Phase Detector

Several varieties of phase detectors can be used for time-based controllers. The most common ones include the exclusive-OR phase detector (XOR PD), the two-state PD, and the tri-state PD. The XOR PD has a linear range which is equal to only π and an output frequency of twice the input frequency. This would complicate the controller design dramatically and increase the impact of a parasitic pole [6] [7]. The two-state PD has a linear range of 2π . Thus, the two phases can not be more than π apart, thereby limiting

the duty cycle to 50%. This constitutes an issue for boost-converter-based PFC applications, as the controller utilizes the fact that the converter's voltage transfer ratio tends towards infinity when the duty cycle approaches 100%. By using the tri-state PD, which has a linear range of 4π , it is possible to produce duty cycles up to 100% [12]. Fig. 8 shows a plot of the input-output relationship of the tri-state PD [7].

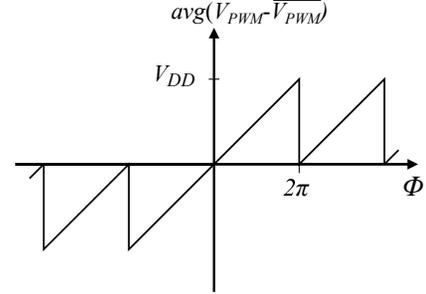


Fig. 8: Relationship between a phase difference at the input and the average output of a tri-state PD.

One persisting issue with the tri-state PD is the fact that when the duty cycle goes beyond 100%, the signal flips over to 0%, rather than decreasing linearly. The flipping of the signal beyond 2π corresponds to a major non-linearity seen at the controller output. A solution to this problem was proposed and implemented in a buck converter in [9] [13] but for the two-state PD. The tri-state PD is recommended for time-based controllers in a PFC boost converter. However, it requires cautiousness during the design stage to ensure stability. Fig. 9 shows a conventional tri-state PD, which is functionally identical to the PD block shown in fig. 6.

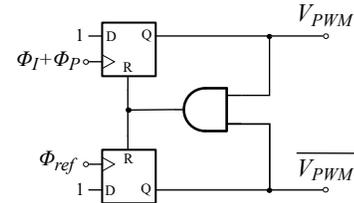


Fig. 9: Tri-state phase detector.

D. Combining the Two Loops

The proposed circuit for combining the two control loops necessary for PFC is shown in fig. 6. The circuit is able to multiply the rectified input voltage $v_{g,rect}(t)$ and the output of the time-based voltage controller $v_{control}(t)$. The circuit works by having the control signal operate two switches which connect the output to either $v_{g,rect}(t)$ or ground, depending on whether the control signal is high or low. The control signal is a PWM signal and the output voltage becomes a chopped version of $v_{g,rect}(t)$. The passives R and C filter this signal and provide the mean value of the chopped version of $v_{g,rect}(t)$. The value K_v/V_M^2 ensures that the multiplier provides the correct gain which yields the desired output

power. This gain is achieved with accurate scaling of the sensed current and voltages. The output voltage of the circuit can be expressed as

$$V_{ref1}(t) = \frac{\text{mean}(v_{control}(t) \cdot v_{g,rect}(t)) \cdot K_v}{V_M^2} \quad (6)$$

It is seen that (6) provides the same expression as the conventional multiplier in (1), where $V_M = V_{g,peak}$. The bandwidth of the RC filter needs to be higher than the input rectified-voltage frequency of 100Hz while still below the oscillation frequencies of the VCOs, i.e. the converter switching frequency.

IV. DESIGN

The proposed time-based control scheme is simulated for a boost PFC with the specifications listed in table I. The system functionality is verified using the system simulator CppSim [14], which is a behavioral simulation tool used for the design of phase-locked loops (PLLs) and other systems.

TABLE I: Design specifications for the boost PFC converter

Input voltage V_{in}	230 V_{rms} 50 Hz
Output voltage V_{out}	400 V
Output Power P	600 W
Operating frequency f_{sw}	50 kHz

A. Controller Gains

Controller gains are evaluated for each of the control loops. First, the current controller gains are obtained using the boost converter's duty-cycle-to-input-current transfer function. The boost PFC duty-cycle-to-input-current response, controller response and the corresponding loop gain for the current controller are shown in fig. 10. The current controller is shown to have a crossover frequency of 18 kHz and a phase margin of 100° . Second, the voltage controller gains are evaluated using the transfer function from the input of the multiplier, with the current controller, to the output voltage of the boost PFC. The boost PFC $V_{control}$ -to- V_{out} response, controller response and the corresponding loop gain for the voltage controller are shown in fig. 11. The voltage controller is shown to have a crossover frequency of 1.3 Hz and a phase margin of 90° . The time-based circuit parameters are then obtained using the conversion of the K_i and K_p to K_{vco} and K_{vcdl} presented in the previous section. The values are shown in table II.

TABLE II: Time-based control circuit parameters

	Current Controller	Voltage Controller
K_{vco}	377 Hz/V	62.84 Hz/V
K_{vcdl}	3.18 μ s/V	15.92 μ s/V

B. Multiplier Circuit Parameters

As mentioned in section III, the multiplier circuit proposed in this work has to have a bandwidth which is above the 100 Hz of the rectified input voltage and below the converter switching frequency, i.e. 50 kHz. Since the phase detector is by nature a sample system, the bandwidth of the multiplier must be kept

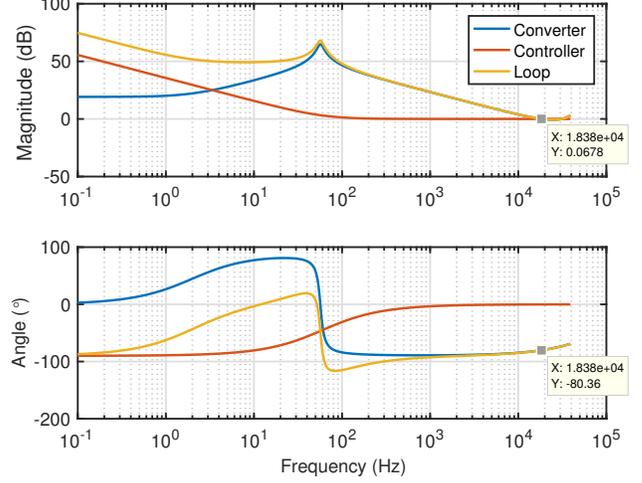


Fig. 10: Bode plot of the current controller $G_c(s)$.

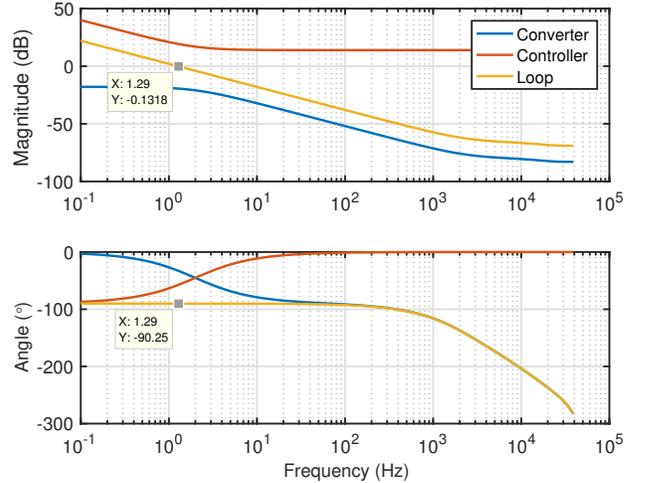


Fig. 11: Bode plot of the voltage controller $G_{cv}(s)$.

a decade lower than the switching frequency, to ensure the validity of the linear models for the transfer functions. The bandwidth is set to

$$f_{3dB,mult} = \frac{1}{2\pi RC} \approx 4.5 \text{ kHz} \quad (7)$$

where the values of the passives R and C are chosen accordingly. It is noted that these passives sizes are indirectly proportional to the switching frequency of the converter, where the higher the switching frequency is, the smaller the sizes for R and C will be, which aids with the passives integration on the same die for high switching frequency designs, and that can result in full monolithic integration of the converter. Table III lists the values for the passive components bill-of-materials (BoM) shown in fig. 6.

TABLE III: Passive components BoM

Component	Value
L_1	4.34 mH
C_{out}	600 μ F
R_{load}	266.7 Ω
C	3.5 pF
R	10 M Ω

V. MODEL RESULTS

This section shows the results of the boost PFC time-based control scheme model simulated in CppSim. Fig. 12 shows the moving average (low-frequency envelope of 50 kHz signal) of the control signals from the voltage and current controllers respectively. It can be seen that in steady-state operation, the voltage control signal is almost constant, with minimal variation around the dc value for achieving a low 100 Hz ripple on the output voltage. On the other hand, the current control signal is varying with the input voltage, regulating the input current, and going in accordance with the conversion ratio waveform shown in fig. 2.

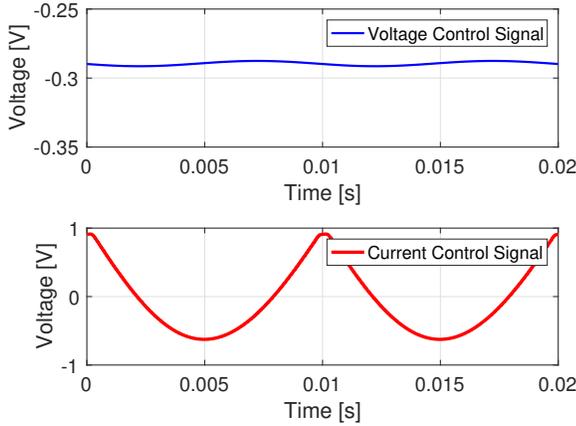


Fig. 12: Moving average of voltage and current controllers outputs from the model results.

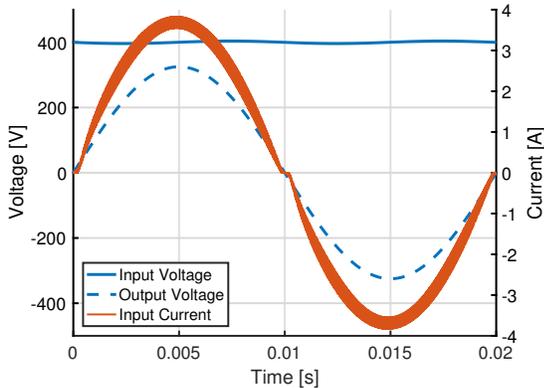


Fig. 13: Input voltage, input current and output voltage from the model results.

Fig. 13 shows the converter input voltage, input current and output voltage. It can be seen that the PFC boost converter is able to maintain a low ripple dc output voltage whilst having an in-phase sinusoidal input current and voltage. The power factor is evaluated to 0.99 at 600 W of output power.

VI. CONCLUSION

A time-based control scheme for a boost PFC converter is presented. The controller is based on the average current mode control, with the PI control loops implemented in time-domain using VCOs, VCDLs and tri-state phase detectors. A multiplier circuit is proposed for combining the two time-based control loops. The system functionality is verified on the system simulator CppSim for a 600 W PFC boost converter with a 400 V dc output and 230 V_{rms} 50 Hz input voltages. Results show a stable output voltage with a small ripple, and a low-harmonic-content input current in phase with the input voltage, achieving a power factor of 0.99.

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