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# Design of 1ϕ 63 Level Inverter Using 9 Switches for Harmonics Mitigation

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***ABSTRACT***

*This project proposes a 1ϕ 63 level inverter with 9 switches only, with a novel pulse width-modulated (PWM) control scheme. In this 63 Level inverter output voltage level increasing by using nine numbers of switches driven by the switch ON/OFF modulation techniques. The inverter is capable of producing sixty three levels of output-voltage (During half positive cycle voltage increase from 0V to +Vdc & decreases to 0V. During negative half cycle voltage decreases from 0V to -Vdc & increases to 0V) from the dc supply voltage. This topology reduces the THD with less number of switches. The H bridge circuit with multiplier cell produces the sixty three level output voltage waveform. The proposed system was verified through MATLAB simulation and the hardware is implemented by using DSPIC30F2010 controller.*

***Keywords****: 63 level inverter, pulse width modulated control, total harmonic distortion*

## INTRODUCTION

Large inverters have traditionally satisfied the ever-increasing demand of high power industrial applications, which currently extends from the tens to hundreds of megawatts. Some examples of this fact are the medium voltage range (2.3 to 13.8 KV) AC motor drives. Nowadays, it is problematic to connect only one power semiconductor switch directly to the grid due to the high voltage range. In order to solve this difficulty, a new type linking them directly to the grid by connecting single devices among multiple DC levels. Multilevel Converters are found in many applications; industrial motor drives, of power converter have been introduced as a solution in high power applications. Multilevel Converters use high speed switching components, avoiding the problem of utility interfaces for renewable energy systems (Photovoltaic, wind energy and fuel cells), flexible AC transmission systems (FACTS), high voltage direct current transmission (HVDC), and traction drives systems.[6-9]

A nine level inverter generates a 9voltage levels in the output with only ten power switches, one auxiliary capacitor (CA) and two input DC capacitors (C1, C2). It has joint features of diode-clamped, flying capacitor and coupled inductor based MLIs.[5,11] The H9LI has a single DC source at the input which is divided into two halves with the support of C1 and C2. The three-level neutral point clamped voltages are divided into five voltage levels by using auxiliary capacitor, CA which is regulated at a voltage of VDC 4. A coupled inductor is incorporated in the H9LI, whose two ends experience five voltage levels (±4VDC/8, ±2VDC/8 and 0) and three voltage levels (±4VDC/8 and 0) respectively due to which the H9LI generates nine different voltage levels at the midpoint "c" of the coupled inductor as listed in Table I. The nine voltage levels produced by H9LI are ± 4VDC/8, ±

  

3VDC/8, ± 2VDC/8, ± VDC/8 and 0 as shown in Figure 2. Each switch used in H9LI is a combination of a fully controlled switch and an antiparallel diode, which allows the current to freewheel through the switches.[10,11]

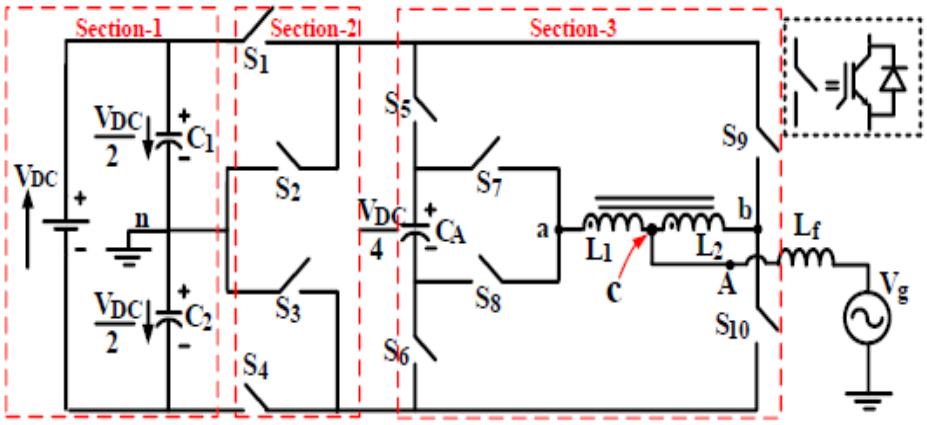


***Fig.1:*** *1-ϕ H9LI Topology.*

The disadvantages in the conventional system is as follows,

1. High THD.
2. Switching losses high.
3. Input capacitors induces voltage stability problem.

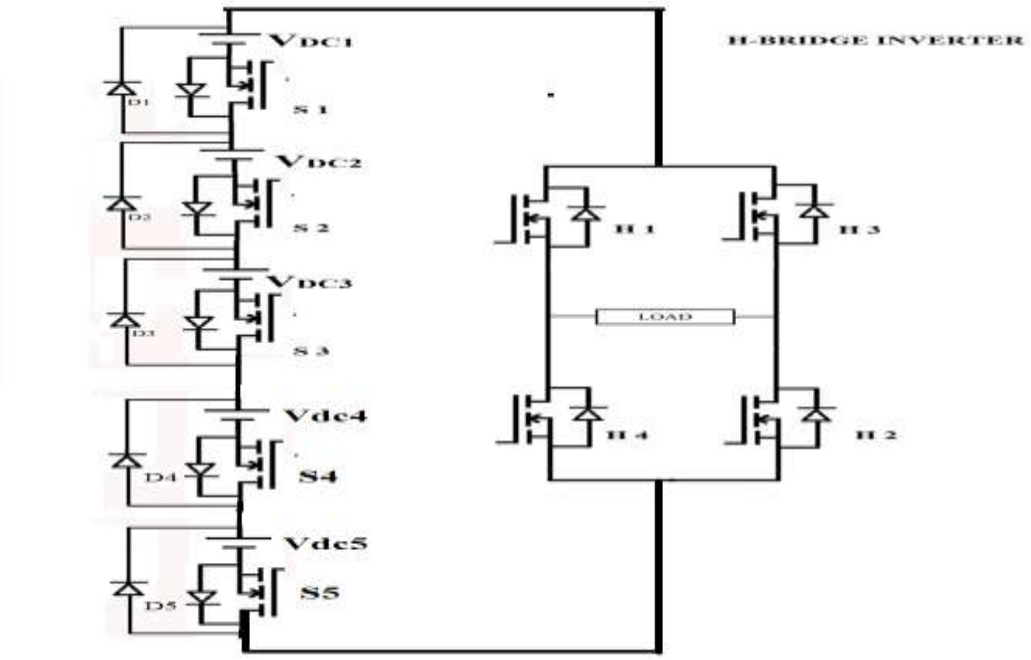


***Fig. 2:*** *Proposed 63 Level Inverter with 9 Switches.*

**63 LEVEL INVERTER**

The proposed single-phase sixty three-level inverter is developed from the existing system. It comprises a Single phase conventional H-bridge inverter, nine switches, and five voltage sources. The switching devices used here is MOSFET. [1-3]

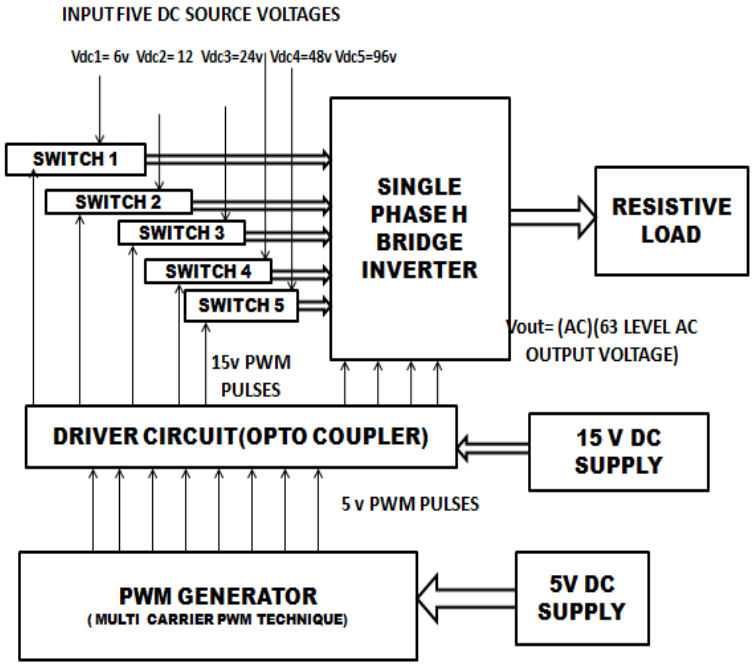


***Fig. 3:*** *Block Diagram of Proposed 63 Level Inverter with 9 Switches.*

The proposed inverter's operation can be divided into sixty three switching states; the required sixty three levels of output voltage were generated as follows.

- Maximum positive output (*V*dc): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input
- 31/31 Positive output (31*V*dc/31): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input supply. The switches S1, S2, S3, S4, S5 are ON. The voltage applied to the load terminals is 31*V*dc/31.
- 30/31 positive output (30*V*dc/31): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input supply. The switches S2, S3, S4, S5 are ON the voltage applied to the load terminals is 30*V*dc/31.
- 29/31 Positive output (29*V*dc/31): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input supply. The switches S1, S3, S4, S5 are ON the voltage applied to the load terminals is 29*V*dc/31.
- 28/31 Positive output (28*V*dc/31): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input supply. The switches S3, S4, S5 are ON. The voltage applied to the load terminals is 28*V*dc/31.
- 27/31Positive output (27*V*dc/31): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input supply The switches S5, S4, S2, S1 are ON. The voltage applied to the load terminals is 27*V*dc/31.
- 26/31 Positive output (26*V*dc/31): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input supply. The switches S2, S4, S5 are ON. The voltage applied to the load terminals is 26*V*dc/31.
- 25/31 Positive output (25*V*dc/31): *H*1

is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input supply. The switches S1, S4,S5 are ON. The voltage applied to the load terminals is 25*V*dc/31.

- 24/31 Positive output (24*V*dc/31): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input supply. The switches S4, S5 are ON. The voltage applied to the load terminals is 24*V*dc/31.
- 23/31 Positive output (23*V*dc/31): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input supply. The switches S5, S3, S2, S1 are ON. The voltage applied to the load terminals is 23*V*dc/31.
- 22/31 Positive output (22*V*dc/31): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input supply. The switches S5, S3, S2 are ON. The voltage applied to the load terminals is 22*V*dc/31.
- 21/31 Positive output (21*V*dc/31): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input supply. The switches S5, S3, S1 are ON. The voltage applied to the load terminals is 21*V*dc/31.
- 20/31 Positive output (20*V*dc/31): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input supply. The switches S5, S3 are ON. The voltage applied to the load terminals is 20*V*dc/31.
- 19/31 Positive output (19*V*dc/31): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input supply. The switches S5, S2, S1 are ON. The voltage applied to the load terminals is 19*V*dc/31.
- 18/31 Positive output (18*V*dc/31): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input supply. The switches S5, S2, are ON. The voltage applied to the load terminals is 18*V*dc/31.
- 17/31 Positive output (17*V*dc/31): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input supply. The switches S5,S1 are ON. The voltage applied to the load terminals is 17*V*dc/31.
- 16/31 Positive output (16*V*dc/31): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input supply. The switches S5 only ON. The voltage applied to the load terminals is 16*V*dc/31.
- 15/31 Positive output (15*V*dc/31): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input supply. The switches S1, S2,S3, S4 are ON. The voltage applied to the load terminals is 15*V*dc/31.
- 14/31 Positive output (14*V*dc/31): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input supply. The switches S2, S3, S4 are ON. The voltage applied to the load terminals is 14*V*dc/31.
- 13/31 Positive output (13*V*dc/31): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input supply. The switches S1, S3, S4 are ON. The voltage applied to the load terminals is 13*V*dc/31.

- 12/31 Positive output (12*V*dc/31): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON,
- load terminals is 12*V*dc/31.
- 11/31 Positive output (11*V*dc/31): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input supply. The switches S1, S2, S4 are ON. The voltage applied to the load terminals is 11*V*dc/31.
- 10/31 Positive output (10*V*dc/31): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input supply. The switches S4, S2 are ON. The voltage applied to the load terminals is 10*V*dc/31.
- 9/31 Positive output (9*V*dc/31): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input supply. The switches S4, S1 are ON. The voltage applied to the load terminals is 9*V*dc/31.
- 8/31 Positive output (8*V*dc/31): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input supply. The switches S4 only ON. The voltage applied to the load terminals is 8*V*dc/31.
- 7/31 Positive output (7*V*dc/31): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input supply. The switches S1, S2, S3 are ON. The voltage applied to the load terminals is 7*V*dc/31.
- 6/31 Positive output (6*V*dc/31): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input supply. The switches S2, S3 are ON. The voltage applied to the load connecting the load negative terminal of input supply. The switches S2, S4 are ON. The voltage applied to the terminals is 6*V*dc/31.
- 5/31 Positive output (5*V*dc/31): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input supply. The switches S1, S3 are ON. The voltage applied to the load terminals is 5*V*dc/31.
- 4/31 Positive output (4*V*dc/31): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input supply. The switches S3 only ON. The voltage applied to the load terminals is 4*V*dc/31.
- 3/31 Positive output (3*V*dc/31): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input supply. The switches S1, S2 are ON. The voltage applied to the load terminals is 3*V*dc/31.
- 2/31 Positive output (2*V*dc/31): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input supply. The switches S2 are ON. The voltage applied to the load terminals is 2*V*dc/31.
- 1/31 Positive output (1*V*dc/31): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal of input supply. The switches S1 only ON. The voltage applied to the load terminals is 1*V*dc/31.
- Zero output: All the switches S1, S2, S3, H1, H2, H3, and H4 are in OFF position.

***Table.1:*** *Positive Cycle Modes of Operation.*

**MODES OF OPERATION (POSITIVE LEVEL)**

| MODES | | SWITCHING SEQUENCE | | | | | | | | | CURRENT PATH | OUTPUT VOLTAGE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | S5 | S4 | S3 | S2 | S1 | H1 | H2 | H3 | H4 | | |
| Positive Level | 1 | 0 | 0 | 0 | 0 | 1 | ON | ON | OFF | OFF | DC1(+)-D2-D3-D4-H1-LOAD-H2-S1-DC1(-) | 6 |
| | 2 | 0 | 0 | 0 | 1 | 0 | ON | ON | OFF | OFF | DC2(+)-D3-D4-D5-H1-LOAD-H2-S1-S2-DC2(-) | 12 |
| | 3 | 0 | 0 | 0 | 1 | 1 | ON | ON | OFF | OFF | DC2(+)-D3-D4-D5-H1-LOAD-H2-S1-DC1(-)-S2-DC2(-) | 18 |
| | 4 | 0 | 0 | 1 | 0 | 0 | ON | ON | OFF | OFF | DC3(+)-D4-D5-H1-LOAD-H2-S1-DC1(-)-DC1-S2-DC2-DC3(-) | 24 |
| | 5 | 0 | 0 | 1 | 0 | 1 | ON | ON | OFF | OFF | DC3(+)-D4-D5-H1-LOAD-H2-S1-DC1-D2-S3-DC3(-) | 30 |
| | 6 | 0 | 0 | 1 | 1 | 0 | ON | ON | OFF | OFF | DC3(+)-D4-D5-H1-LOAD-H2-D1-S2-DC2-S3-DC3(-) | 36 |
| | 7 | 0 | 0 | 1 | 1 | 1 | ON | ON | OFF | OFF | DC3(+)-D4-D5-H1-LOAD-H2-S1-DC1-S2-DC2-S3-DC3(-) | 42 |
| | 8 | 0 | 1 | 0 | 0 | 0 | ON | ON | OFF | OFF | DC4(+)-D4-D5-H1-LOAD-H2-D1-D2-D3-DC4(-) | 48 |
| | 9 | 0 | 1 | 0 | 0 | 1 | ON | ON | OFF | OFF | DC4(+)-D5-H1-LOAD-H2-S1-DC1-D2-D3-DC4(-) | 54 |
| | 10 | 0 | 1 | 0 | 1 | 0 | ON | ON | OFF | OFF | DC4(+)-D5-H1-LOAD-H2-D1-S2-DC2-D3-DC4(-) | 60 |
| | 11 | 0 | 1 | 0 | 1 | 1 | ON | ON | OFF | OFF | DC4(+)-D5-H1-LOAD-H2-S1-DC1-S2-DC2-D3-DC4(-) | 66 |
| | 12 | 0 | 1 | 1 | 0 | 0 | ON | ON | OFF | OFF | DC4(+)-D5-H1-LADD-H2-D1-D2-S3-DC3-DC4(-) | 72 |
| | 13 | 0 | 1 | 1 | 0 | 1 | ON | ON | OFF | OFF | DC4(+)-D5-H1-LOAD-H2-S1-DC1-D2-S3-DC3-S4-DC4(-) | 78 |
| | 14 | 0 | 1 | 1 | 1 | 0 | ON | ON | OFF | OFF | DC4(+)-D5-H1-LOAD-H2-D1-S2-DC2-S3-DC3-S4-DC4(-) | 84 |
| | 15 | 0 | 1 | 1 | 1 | 1 | ON | ON | OFF | OFF | DC4(+)-D5-H1-LOAD-H2-S1-DC1-S2-DC2-S3-DC3-S4-DC4(-) | 90 |
| | 16 | 1 | 0 | 0 | 0 | 0 | ON | ON | OFF | OFF | DC(+)-H1-LOAD-H2-D1-D2-D3-D4-DC5(-) | 96 |
| | 17 | 1 | 0 | 0 | 0 | 1 | ON | ON | OFF | OFF | DC5(+)-H1-LOAD-H2-S1-DC1-D2-D3-D4-DC5(-) | 102 |
| | 18 | 1 | 0 | 0 | 1 | 0 | ON | ON | OFF | OFF | DC5(+)-H1-LOAD-H1-D1-S2-DC2-D3-D4-DC5(-) | 108 |
| | 19 | 1 | 0 | 0 | 1 | 1 | ON | ON | OFF | OFF | DC5(+)-H1-LOAD-H2-S1-DC1-S2-DC2-D3-D4-DC5(-) | 114 |
| | 20 | 1 | 0 | 0 | 0 | 0 | ON | ON | OFF | OFF | DC5(+)-H1-LOAD-H2-S1-DC1-D2-S3-DC3-D4-DC5(-) | 120 |
| | 21 | 1 | 0 | 0 | 0 | 1 | ON | ON | OFF | OFF | DC5(+)-H1-LOAD-H2-D1-S2-DC2-S3-DC3-D4-DC5(-) | 126 |
| | 22 | 1 | 0 | 0 | 1 | 0 | ON | ON | OFF | OFF | DC5(+)-H1-LOAD-H2-D1-S2-DC2-S3-DC3-D4-DC5(-) | 132 |
| | 23 | 1 | 0 | 0 | 1 | 1 | ON | ON | OFF | OFF | DC5(+)-H1-LOAD-H2-S1-DC1-S2-DC2-S3-DC3-D4-DC5(-) | 138 |
| | 24 | 1 | 1 | 1 | 0 | 0 | ON | ON | OFF | OFF | DC5(+)-H1-LOAD-H2-D1-D2-D3-S4-DC4-DC5(-) | 144 |
| | 25 | 1 | 1 | 1 | 0 | 1 | ON | ON | OFF | OFF | DC5(+)-H1-LOAD-H2-S1-DC1-D2-D3-S4-DC3-DC5(-) | 150 |
| | 26 | 1 | 1 | 1 | 1 | 0 | ON | ON | OFF | OFF | DC5(+)-H1-LOAD-H2-D1-S2-DC2-D3-S4-DC4-DC5(-) | 156 |
| | 27 | 1 | 1 | 1 | 1 | 1 | ON | ON | OFF | OFF | DC5(+)-H1-LOAD-H2-S1-DC1-S2-DC2-D3-S4-DC4-DC5(-) | 162 |
| | 28 | 1 | 1 | 1 | 0 | 0 | ON | ON | OFF | OFF | DC5(+)-H1-LOAD-H2-D1-D2-S3-DC3-S4-DC4-DC5(-) | 168 |
| | 29 | 1 | 1 | 1 | 0 | 1 | ON | ON | OFF | OFF | DC5(+)-H1-LOAD-H2-S1-DC1-D2-S3-DC3-S4-DC4-DC5(-) | 174 |
| | 30 | 1 | 1 | 1 | 1 | 0 | ON | ON | OFF | OFF | DC5(+)-H1-LOAD-H2-D1-S2-DC2-S3-DC3-S4-DC4-DC5(-) | 180 |
| | 31 | 1 | 1 | 1 | 1 | 1 | ON | ON | OFF | OFF | DC5(+)-H1-LOAD-H2-S1-DC1-S2-DC2-S3-DC3-S4-DC4-DC5(-) | 186 |
| Zero Level | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

During negative half cycle voltage decreases from 0V to -Vdc & increases to 0V.

***Table. 2:*** *Negative Cycle Modes of Operation.*

**MODES OF OPERATION (NEGATIVE LEVEL)**

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Negative Level | 1 | 0 | 0 | 0 | 0 | 1 | OFF | OFF | ON | ON | DC1(+)-D2-D3-D4-H3-LOAD-H4-S1-DC1(-) | -6 |
| | 2 | 0 | 0 | 0 | 1 | 0 | OFF | OFF | ON | ON | DC2(+)-D3-D4-D5-H3-LOAD-H4-S1-S2-DC2(-) | -12 |
| | 3 | 0 | 0 | 0 | 1 | 1 | OFF | OFF | ON | ON | DC2(+)-D3-D4-D5-H3-LOAD-H4-S1-DC1(-)-S2-DC2(-) | -18 |
| | 4 | 0 | 0 | 1 | 0 | 0 | OFF | OFF | ON | ON | DC3(+)-D4-D5-H3-LOAD-H4-S1-DC1(-)-DC1-S2-DC2-DC3(-) | -24 |
| | 5 | 0 | 0 | 1 | 0 | 1 | OFF | OFF | ON | ON | DC3(+)-D4-D5-H3-LOAD-H4-S1-DC1-D2-S3-DC3(-) | -30 |
| | 6 | 0 | 0 | 1 | 1 | 0 | OFF | OFF | ON | ON | DC3(+)-D4-D5-H3-LOAD-H4-D1-S2-DC2-S3-DC3(-) | -36 |
| | 7 | 0 | 0 | 1 | 1 | 1 | OFF | OFF | ON | ON | DC3(+)-D4-D5-H3-LOAD-H4-S1-DC1-S2-DC2-S3-DC3(-) | -42 |
| | 8 | 0 | 1 | 0 | 0 | 0 | OFF | OFF | ON | ON | DC4(+)-D4-D5-H3-LOAD-H4-D1-D2-D3-DC4(-) | -48 |
| | 9 | 0 | 1 | 0 | 0 | 1 | OFF | OFF | ON | ON | DC4(+)-D5-H3-LOAD-H4-S1-DC1-D2-D3-DC4(-) | -54 |
| | 10 | 0 | 1 | 0 | 1 | 0 | OFF | OFF | ON | ON | DC4(+)-D5-H3-LOAD-H4-D1-S2-DC2-D3-DC4(-) | -60 |
| | 11 | 0 | 1 | 0 | 1 | 1 | OFF | OFF | ON | ON | DC4(+)-D5-H3-LOAD-H4-S1-DC1-S2-DC2-D3-DC4(-) | -66 |
| | 12 | 0 | 1 | 1 | 0 | 0 | OFF | OFF | ON | ON | DC4(+)-D5-H3-LADD-H4-D1-D2-S3-DC3-DC4(-) | -72 |
| | 13 | 0 | 1 | 1 | 0 | 1 | OFF | OFF | ON | ON | DC4(+)-D5-H3-LOAD-H4-S1-DC1-D2-S3-DC3-S4-DC4(-) | -78 |
| | 14 | 0 | 1 | 1 | 1 | 0 | OFF | OFF | ON | ON | DC4(+)-D5-H3-LOAD-H4-D1-S2-DC2-S3-DC3-S4-DC4(-) | -84 |
| | 15 | 0 | 1 | 1 | 1 | 1 | OFF | OFF | ON | ON | DC4(+)-D5-H3-LOAD-H4-S1-DC1-S2-DC2-S3-DC3-S4-DC4(-) | -90 |
| | 16 | 1 | 0 | 0 | 0 | 0 | OFF | OFF | ON | ON | DC(+)-H3-LOAD-H4-D1-D2-D3-D4-DC5(-) | -96 |
| | 17 | 1 | 0 | 0 | 0 | 1 | OFF | OFF | ON | ON | DC5(+)-H3-LOAD-H4-S1-DC1-D2-D3-D4-DC5(-) | -102 |
| | 18 | 1 | 0 | 0 | 1 | 0 | OFF | OFF | ON | ON | DC5(+)-H3-LOAD-H4-D1-S2-DC2-D3-D4-DC5(-) | -108 |
| | 19 | 1 | 0 | 0 | 1 | 1 | OFF | OFF | ON | ON | DC5(+)-H3-LOAD-H4-S1-DC1-S2-DC2-D3-D4-DC5(-) | -114 |
| | 20 | 1 | 0 | 0 | 0 | 0 | OFF | OFF | ON | ON | DC5(+)-H3-LOAD-H4-S1-DC1-D2-S3-DC3-D4-DC5(-) | -120 |
| | 21 | 1 | 0 | 0 | 0 | 1 | OFF | OFF | ON | ON | DC5(+)-H3-LOAD-H4-D1-S2-DC2-S3-DC3-D4-DC5(-) | -126 |
| | 22 | 1 | 0 | 0 | 1 | 0 | OFF | OFF | ON | ON | DC5(+)-H3-LOAD-H4-D1-S2-DC2-S3-DC3-D4-DC5(-) | -132 |
| | 23 | 1 | 0 | 0 | 1 | 1 | OFF | OFF | ON | ON | DC5(+)-H3-LOAD-H4-S1-DC1-S2-DC2-S3-DC3-D4-DC5(-) | -138 |
| | 24 | 1 | 1 | 1 | 0 | 0 | OFF | OFF | ON | ON | DC5(+)-H3-LOAD-H4-D1-D2-D3-S4-DC4-DC5(-) | -144 |
| | 25 | 1 | 1 | 1 | 0 | 1 | OFF | OFF | ON | ON | DC5(+)-H3-LOAD-H4-S1-DC1-D2-D3-S4-DC3-DC5(-) | -150 |
| | 26 | 1 | 1 | 1 | 1 | 0 | OFF | OFF | ON | ON | DC5(+)-H3-LOAD-H4-D1-S2-DC2-D3-S4-DC4-DC5(-) | -156 |
| | 27 | 1 | 1 | 1 | 1 | 1 | OFF | OFF | ON | ON | DC5(+)-H3-LOAD-H4-S1-DC1-S2-DC2-D3-S4-DC4-DC5(-) | -162 |
| | 28 | 1 | 1 | 1 | 0 | 0 | OFF | OFF | ON | ON | DC5(+)-H3-LOAD-H4-D1-D2-S3-DC3-S4-DC4-DC5(-) | -168 |
| | 29 | 1 | 1 | 1 | 0 | 1 | OFF | OFF | ON | ON | DC5(+)-H3-LOAD-H4-S1-DC1-D2-S3-DC3-S4-DC4-DC5(-) | -174 |
| | 30 | 1 | 1 | 1 | 1 | 0 | OFF | OFF | ON | ON | DC5(+)-H3-LOAD-H4-D1-S2-DC2-S3-DC3-S4-DC4-DC5(-) | -180 |
| | 31 | 1 | 1 | 1 | 1 | 1 | OFF | OFF | ON | ON | DC5(+)-H3-LOAD-H4-S1-DC1-S2-DC2-S3-DC3-S4-DC4-DC5(-) | -186 |

## WORKING OPERATION OF 63 LEVEL INVERTER

In this project multi carrier pulse width modulation technique is used to generate the sixty three level output voltage. Seven equal amplitude carrier triangular signals with offset are compared with the sinusoidal reference signal. These PWM signals are given to the switches S1, S2, S3, S4. Then the two sinusoidal signals having 180 degree displacement signals are compared with the carrier triangular signal, these PWM pulses are having dead band, it will avoid the shoot through problem between two devices. These PWM pulses are given to the single phase inverter circuit switches H1, H2, H3 and H4. Here the switching device is MOSFET; as compared to IGBT the cost is low. The processor used here is PIC (peripheral interface controller). It's under the category of Very large scale integration system. In PIC many of the pins are multiplexed pins. So we can use it as either input or output pins. The operating speed of the DSPIC controller operating speed is much greater than Digital signal processors. These controllers are used to generate the PWM pulses to the sixty three level inverter. [4]

## SIMULATION RESULTS

Simulation of power electronic converters can be done by MATLAB software.

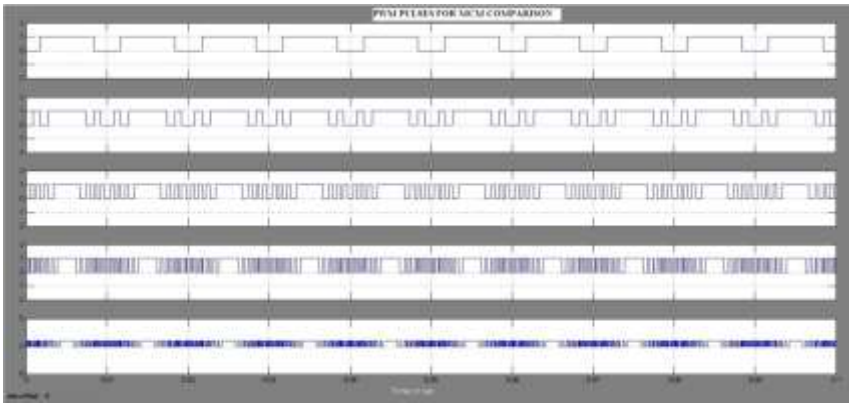

***Fig. 4:*** *PWM Pulses to the 63 Level Inverter Switches.*

The above figure shows the PWM pulses applied to the switches S1, S2, S3, S4, S5. This pulse having 5 KhZ switching frequency to control the additional switches. These PWM pulses are the main reason to control the output voltage of the inverter.

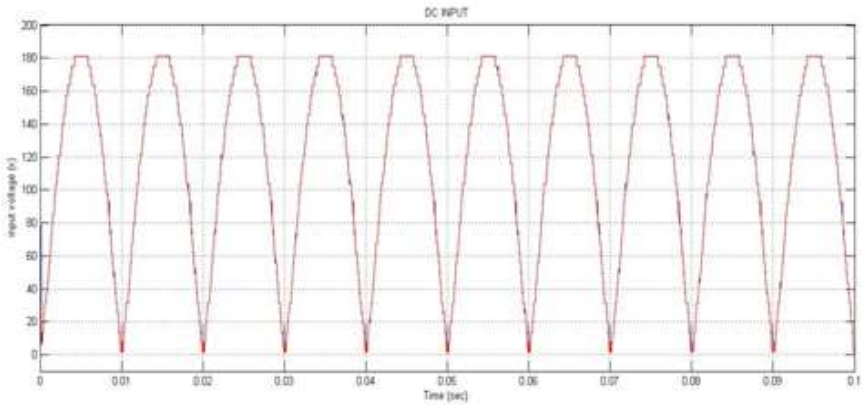


***Fig. 5:*** *DC Output Voltage Waveform before Inverter.*

The above figure shows the output of the sixty three levels before going to the single phase inverter. This level output voltage is given to the inverter. It wills separate the positive and negative output levels.

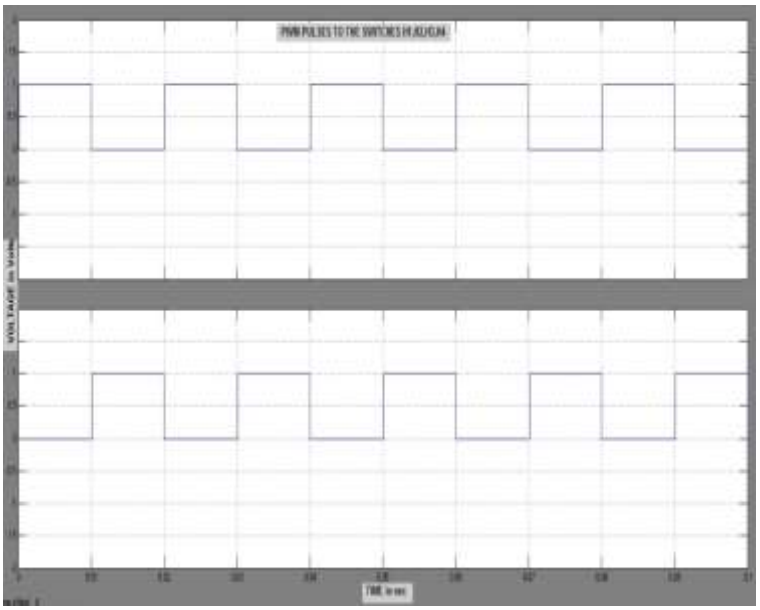

***Fig. 6:*** *PWM Pulses to the H Bridge Inverter.*

The above figure shows the PWM pulses applied to the single phase inverter. This has 180 degree displacement. The fundamental frequency of the reference signal is 50Hz.

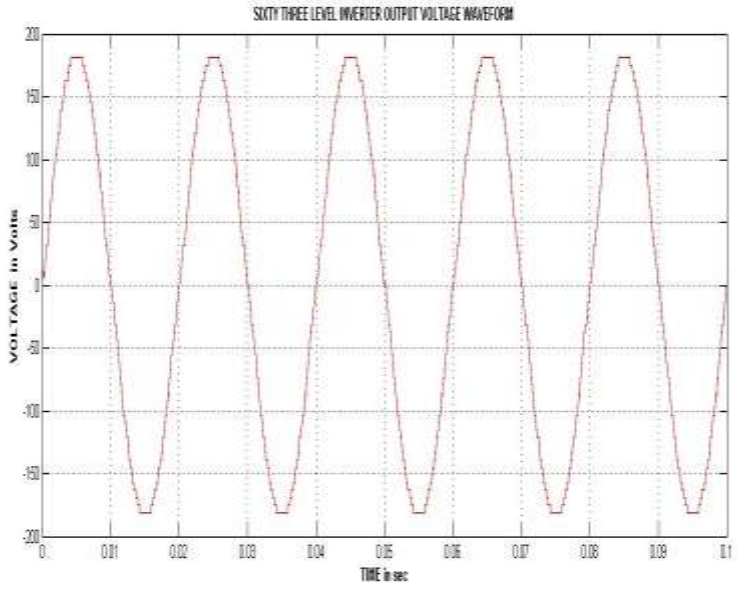


***Fig. 7:*** *Level Inverter Output Voltage.*

The above figure shows the output voltage level of the proposed inverter topology. The output voltage is near sinusoidal wave. This means we can expect very less amount of THD. The output voltage is 183 Volt. This voltage is given to the load.

Here the resistive load is 100 Ohms. And the load current is 1.83 Amps.

The below figure shows the THD results of the proposed sixty three level inverter with resistive load. Here the THD result is only 2.74%.

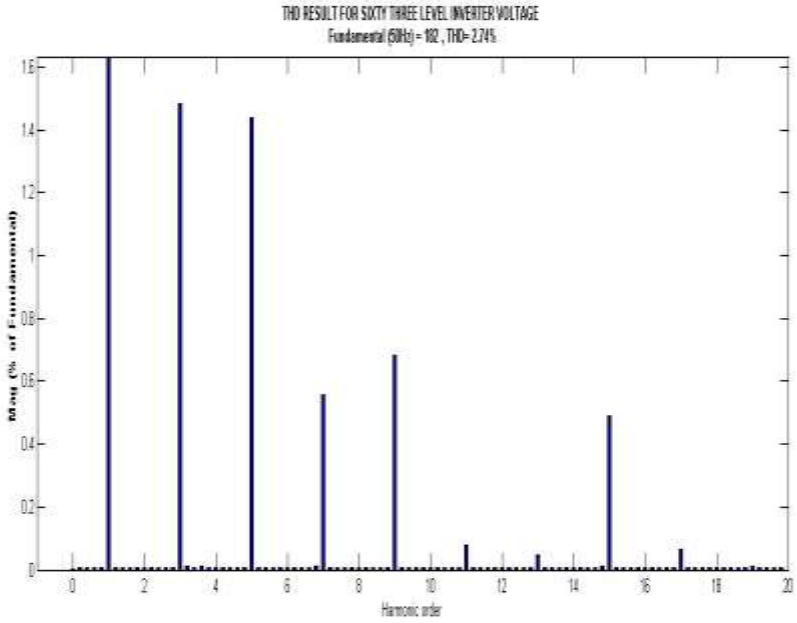


***Fig. 8:*** *THD Result.*

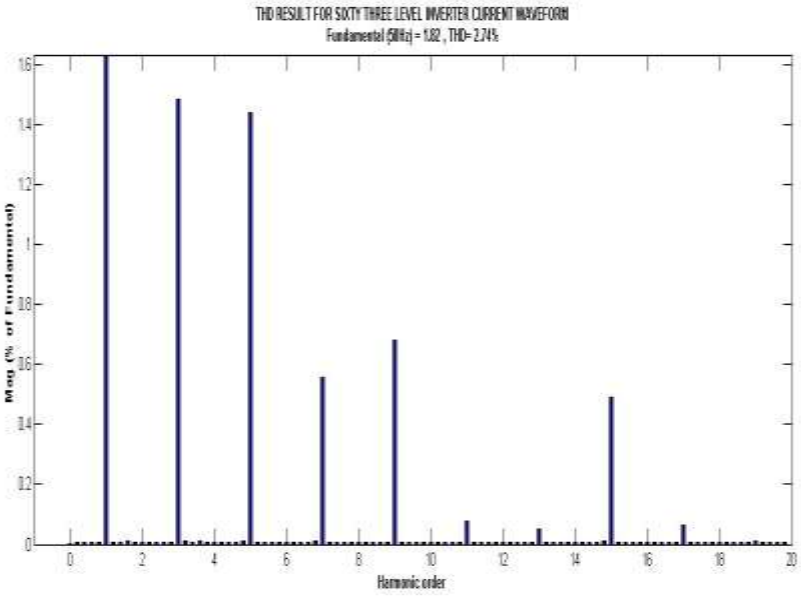


***Fig. 9:*** *63 Level Inverter Current THD.*

The above figure shows the THD results of the proposed sixty three level inverter current waveform with resistive load. Here the THD result is only 2.74%.

**HARDWARE RESULTS**

The Hardware kit consists of Power supply unit, DSPIC30F2010 controller kit, Driver circuit, Opto-isolator kit, H bridge inverter kit, input DC supply with 9 switches.

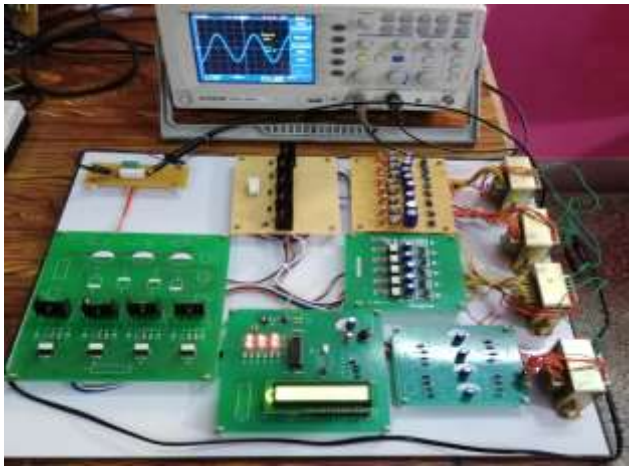

***Fig. 10:*** *Hardware Kit.*

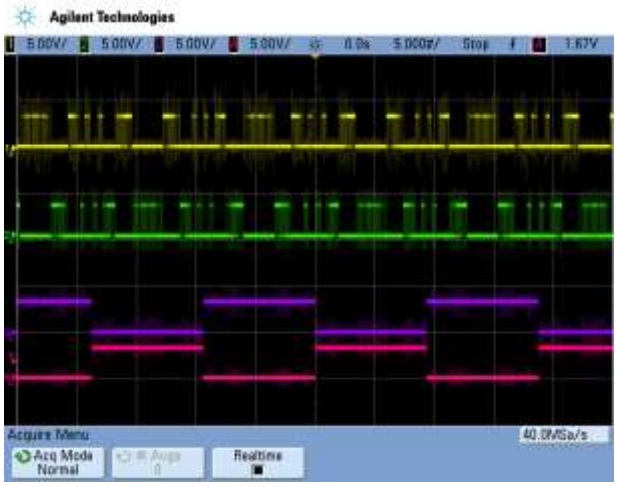


***Fig. 11:*** *PWM Pulses to the Inverter Switches.*

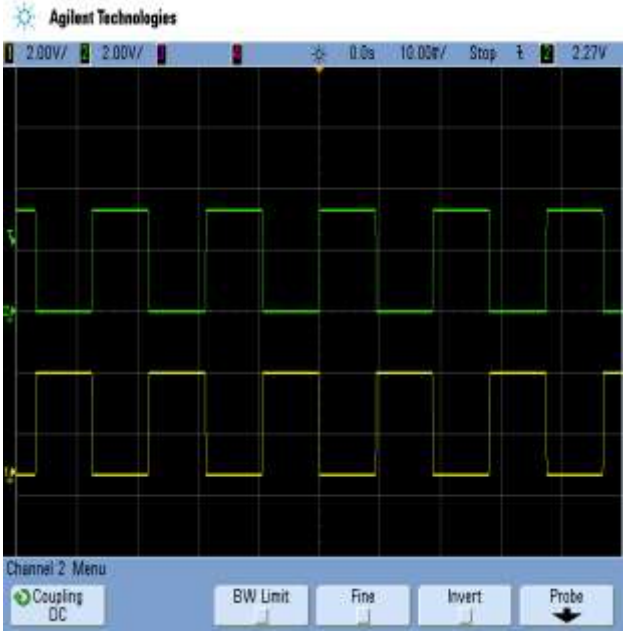


***Fig. 12:*** *PWM Pulses to the Inverter.*

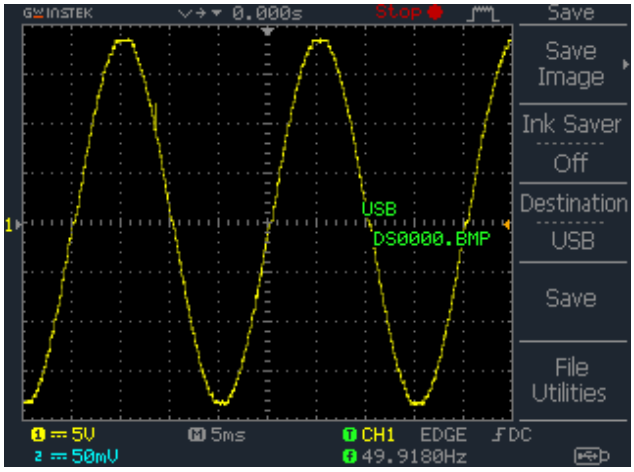


***Fig. 13:*** *63 Level Inverter Output Voltage Waveform.*

## CONCLUSION

Multilevel inverters offer improved output waveforms and lower THD. This paper has presented a novel PWM switching scheme for the proposed multilevel inverter. Here there are five different DC voltage levels are used in this multi-level inverters. So this method of configuration is known as asymmetrical cascaded inverter. By controlling the modulation index and different levels of DC voltages the sixty three levels of the output voltage's achieved.

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