



VILLAS4ERIGrid

Geographically Distributed Real-time Simulation and PHIL between TU Delft, DTU Risø, Lyngby and RWTH Aachen

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Speaker / User Group



■ Guests:

- ≡ Steffen Vogel (RWTH)
- ≡ Marija Stevic (RWTH)

■ Hosts:

- ≡ Kai Heussen (DTU)
- ≡ Ha Thi Ngyuen (DTU)
- ≡ Vetrivel Subramaniam Rajkuma (TUD)
- ≡ Rishabh Bhandia (TUD)



Transnational Access Exchanges

■ ERIGrid Transnational Access Exchange(s)

≡ May 2019: TU Delft

= Improvements to the Co-simulation Interface for Geographically Distributed Real-time Simulation, IECON 2019



≡ October 2019: DTU Denmark

= Distributed PHIL with Quasi Stationary Back-to-Back Converter
= Energy Based Metric (EBM) for error quantification



Inbetween

■ MariNet2 Transnational Access Exchange

≡ August 2019

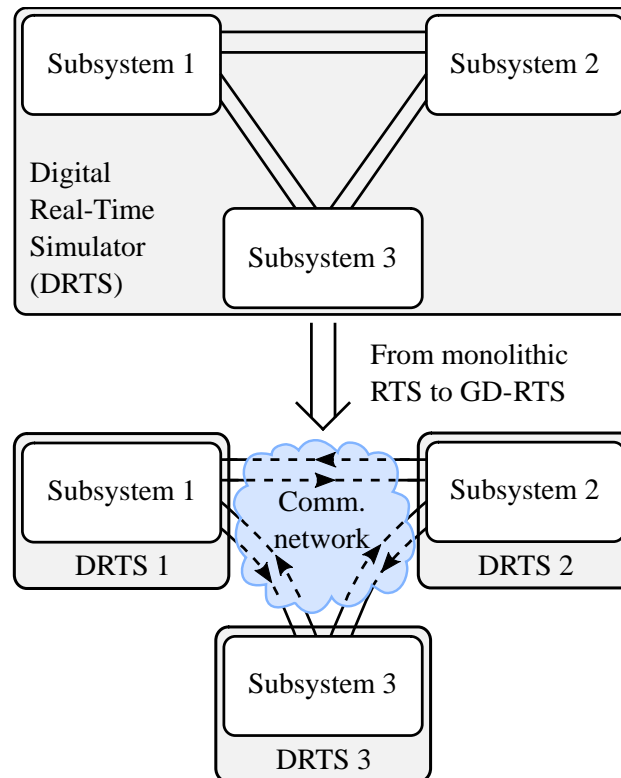


1/ TU Delft

Improvements to the Co-simulation Interface for Geographically Distributed Real-time Simulation

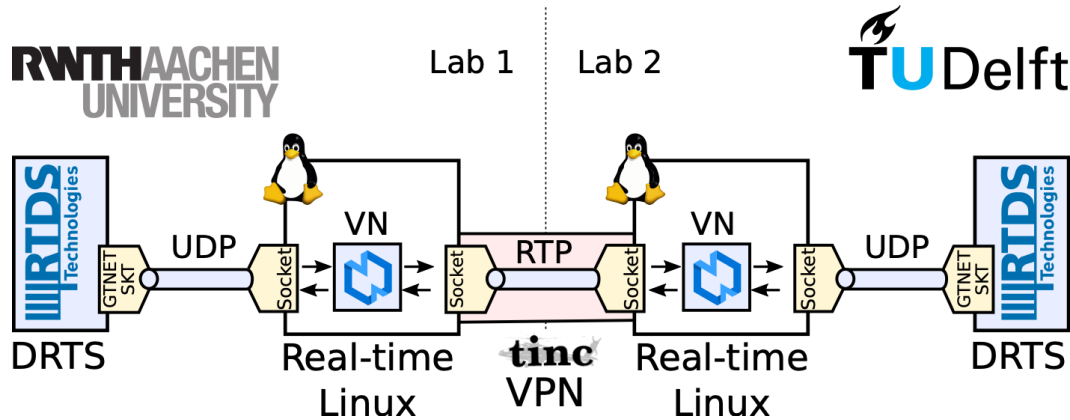
Geographically Distributed Real-time Simulation (GD-RTS)

- A single digital real-time simulation spanning multiple laboratories
 - ≡ Globally or
 - ≡ on Campus
- Motivation
 - ≡ **Large-scale** system-level simulations
 - ≡ Exchange of Knowledge, Human- and Hardware **Resources**
 - ≡ Overcome constraints caused by **data confidentiality**



System Architecture

- 2 Labs:
 - ≡ 2 RTDS Simulators
 - ≡ 2 VILLASnode Gateways
 - ≡ Decentral / Fully-meshed VPN for optimal point-to-point connection with lowest latency



Network Connectivity

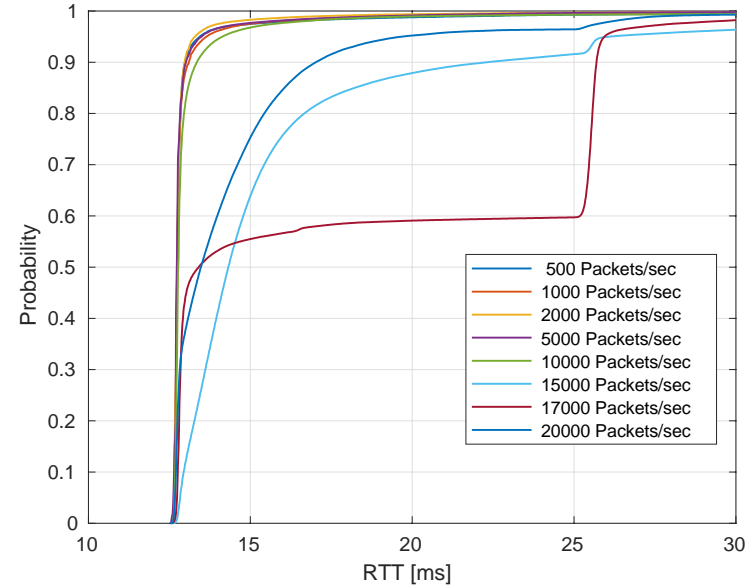
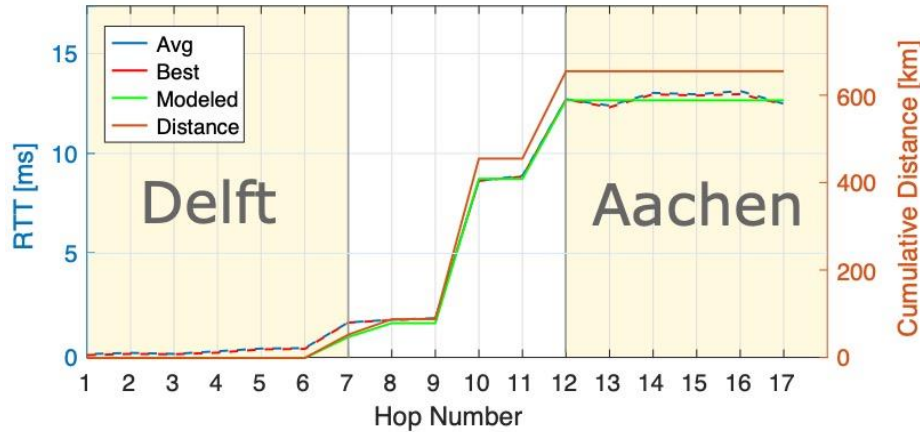
- National Research and Education Networks (NRENs)

 - ≡ DFN, SURFnet, GÉANT

- Mean Round-trip time: **12 ms**

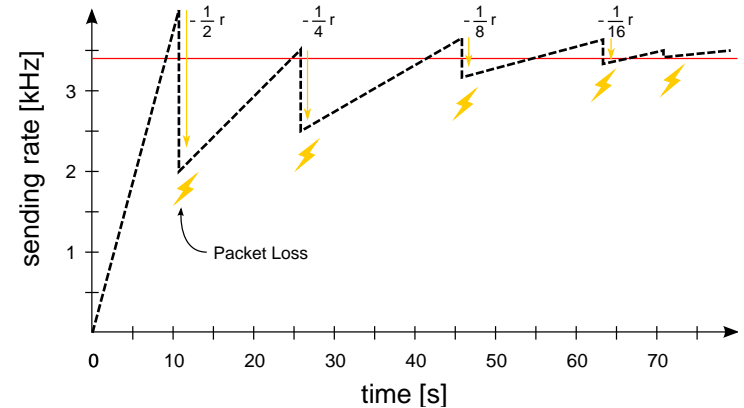
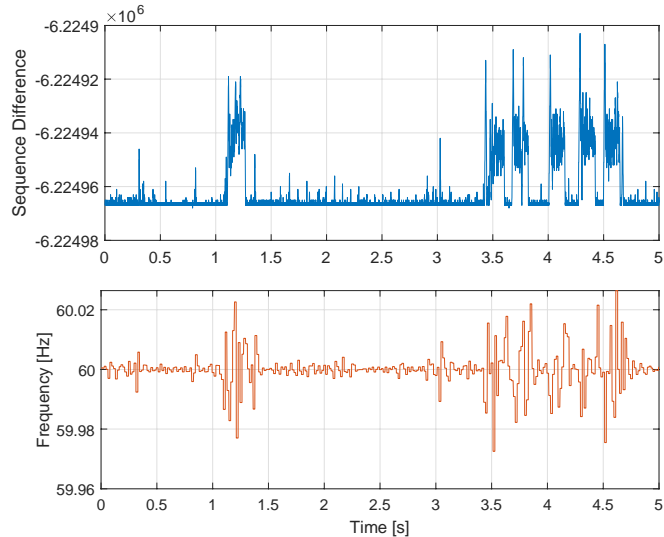
- Routing hops: **13**

- Sending rate: **$\leq 10 \text{ kPkt/s}$**



Real-time Transport Protocol (RTP)

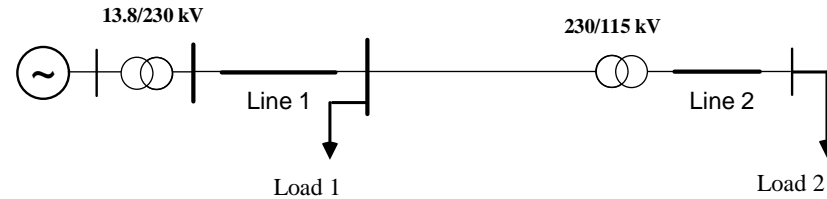
- Different co-sim links vary significantly in quality of service (QoS)
- Adaptive adjustment of communication parameters is helpful
- Additive Increase – Multiplicative Decrease (AIMD)



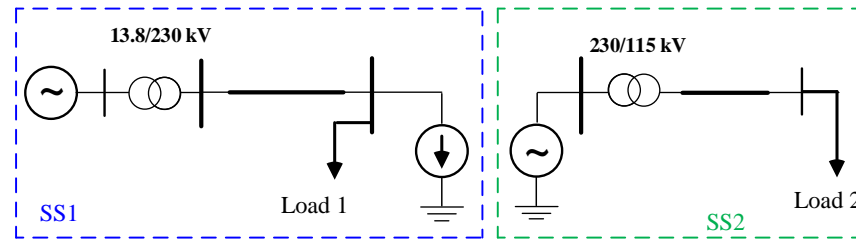
- Discontinuities in sending rate cause frequency disturbances in simulation
- Only useful for initial estimation, not during live simulation

Test Scenario & Methodology

- Simple scenario helped debugging and understanding
- 3 Stages: monolithic, decoupled, distributed



a) Monolithic Model



b) Decoupled / Distributed Model

Simulation Results: Instantaneous V/I

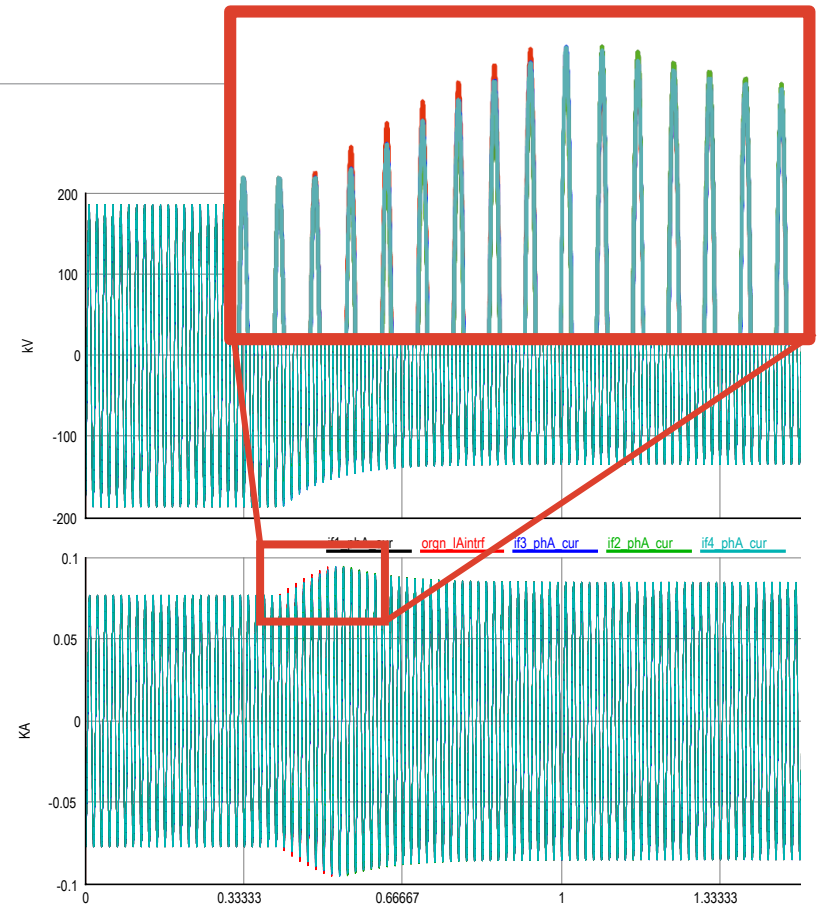
■ Test cases:

- ≡ Voltage Source in SS1 (left)
- ≡ Change of magnitude, frequency, phase

■ No error in steady-state

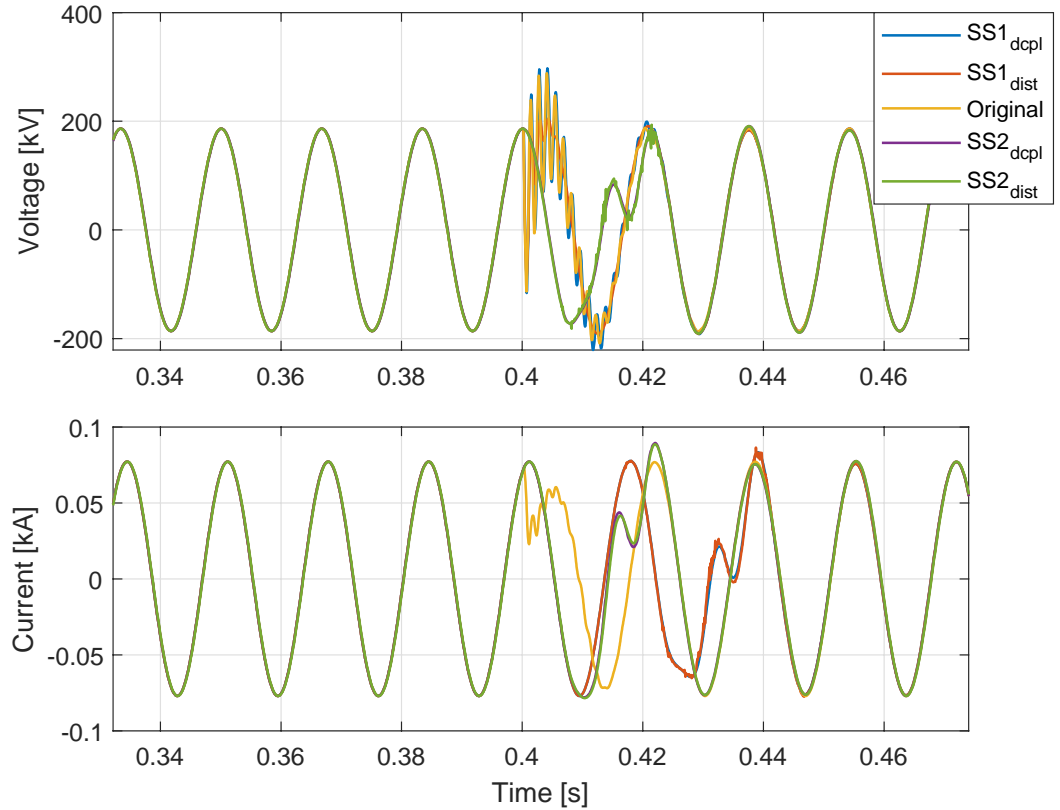
■ Delayed update of

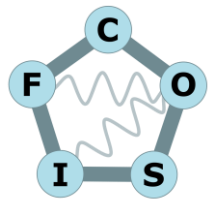
- ≡ Voltage magnitude SS1 (1/2 RTT)
- ≡ Current magnitude on left side (1 RTT)



Limits of GD-RTS

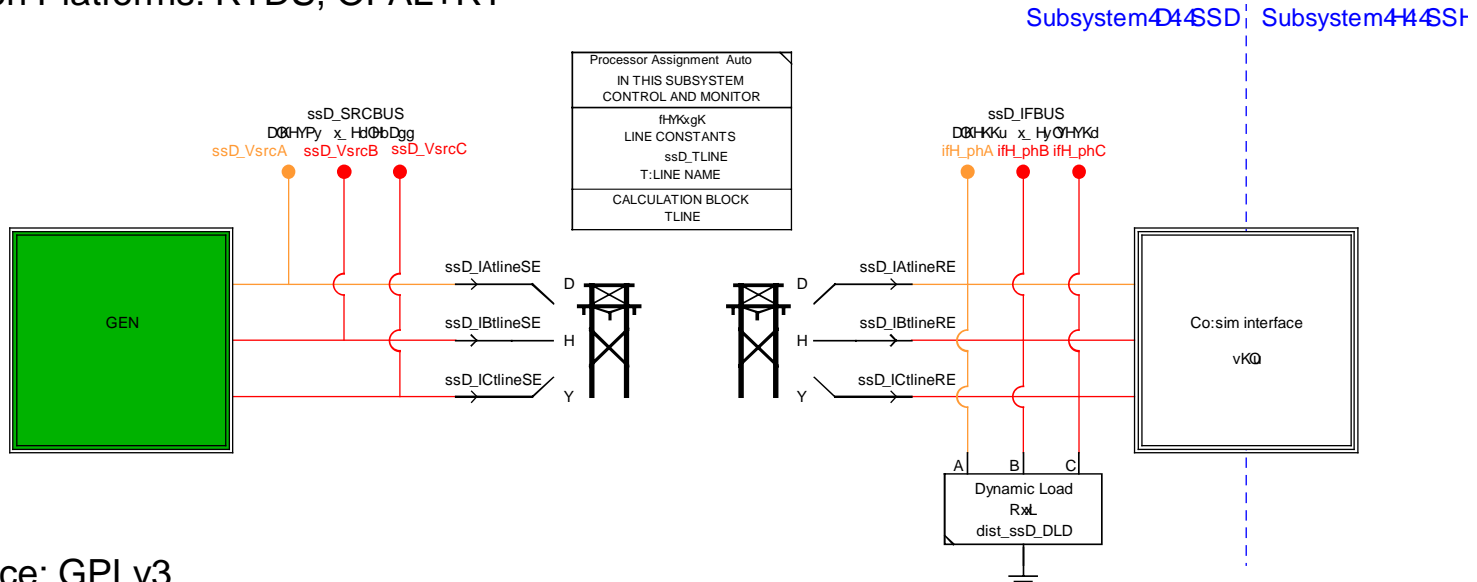
■ Phase jump of π of V_{src}





■ Re-usable library blocks for different:

- ≡ Interface Algorithms: Dynamic Phasors, PQ + V_{rms}, f, ϕ
- ≡ Simulation Platforms: RTDS, OPAL+RT



■ Open Source: GPLv3

≡ <https://fein-aachen.org/projects/cosif/>

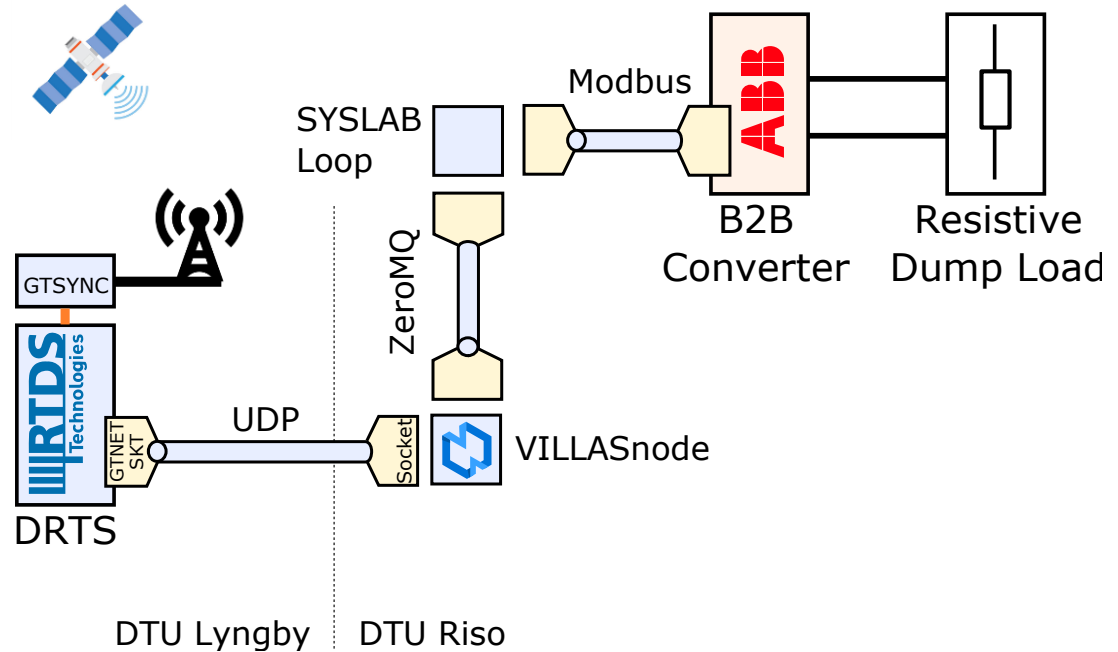


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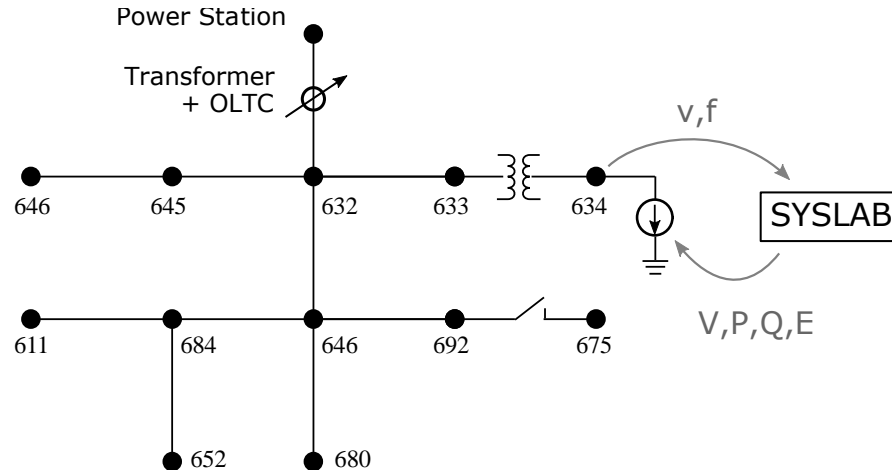
Distributed PHIL with Quasi Stationary B2B Converter

Setup

- Distributed across DTU Lyngby and Riso Campus
- Time-stamped measurements via GTSYNC (GPS) and NTP
- Separate SYSLAB Loop for interfacing Modbus Converter
- Security concerns

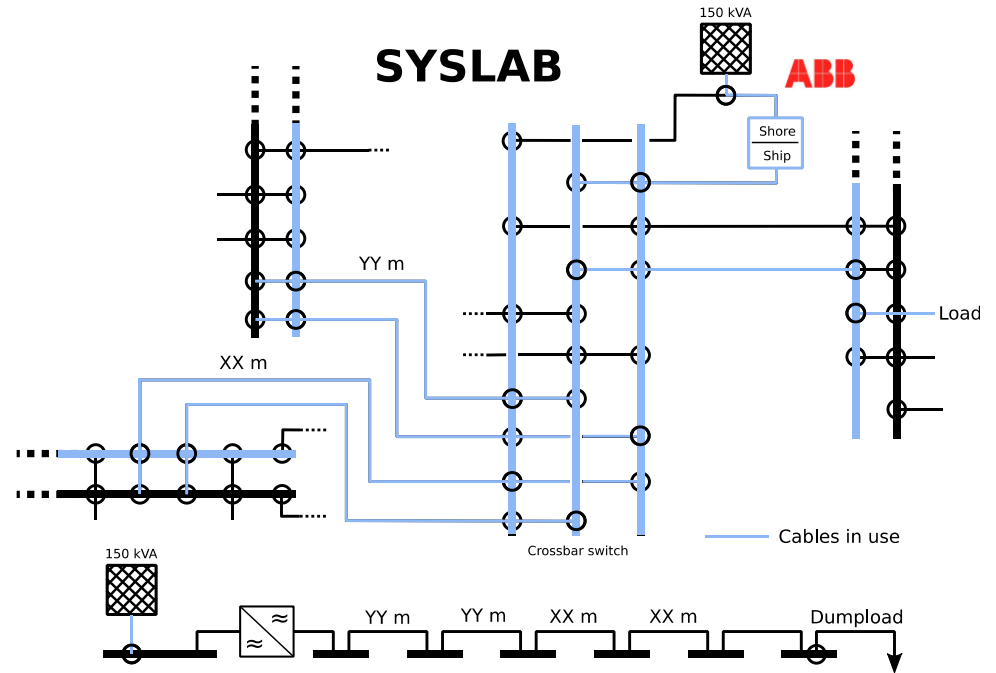


- RTDS with GTNET & GTSYNC
- IEEE 13-bus Distribution Grid Benchmark
 - ≡ Balanced Loads
- SYSLAB PCC at Node 634
- Voltage Control via OLTC
 - ≡ Triggered via change of setpoint of dump load



SYSLAB Configuration

- Simplet setup with ABB Ship-to-Shore converter
- All Lines of SYSLAB are connected in series
- Resistive Dump Load
- Scaling of current injections into simulation

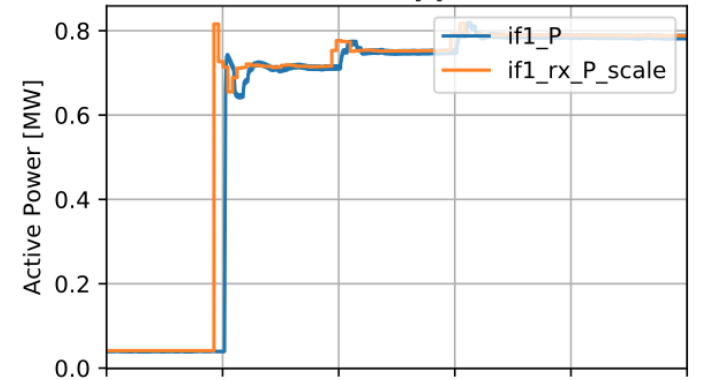
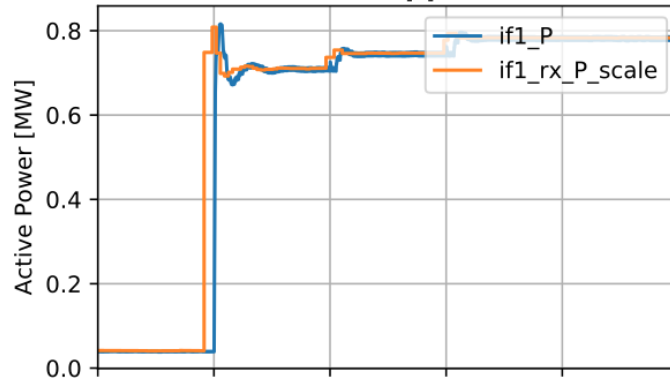
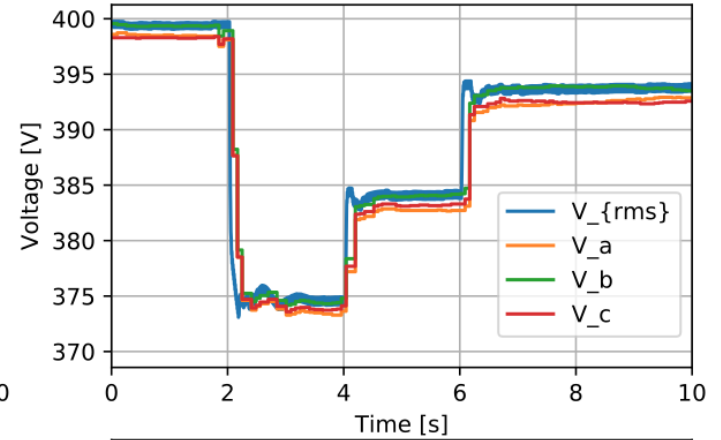
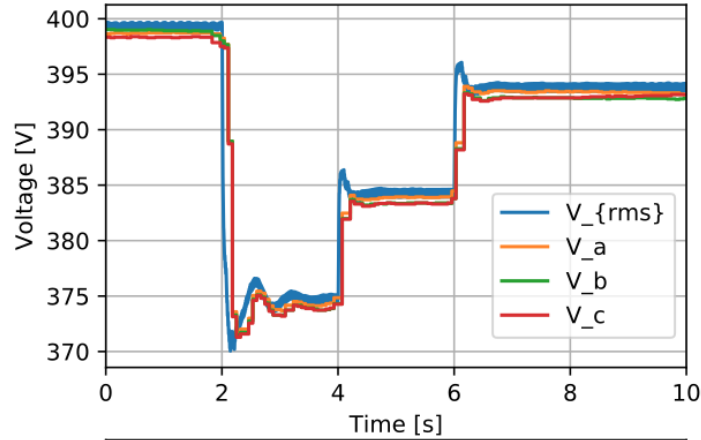


Results /1

■ Tap-Changer Operatio

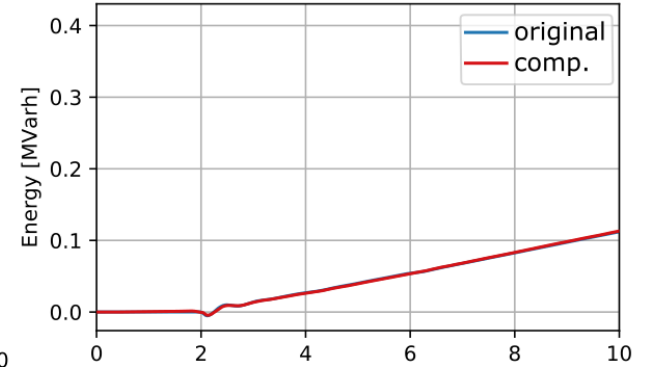
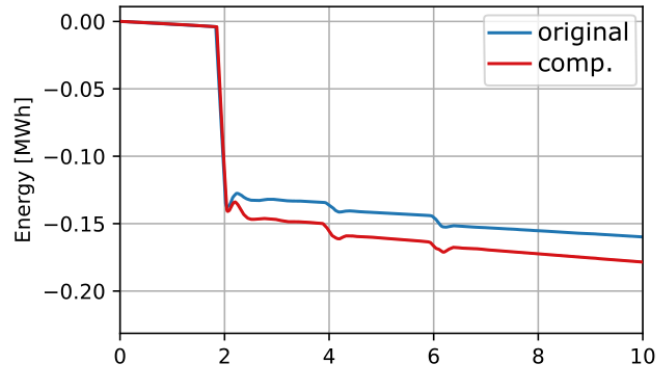
■ Left: Original

■ Right: Compensated



Results /2: Energy Balance

- Energy (Im-) Balance between both ports of the interface
- Compensated case shows even larger error
 - ≡ Caused by unsynchronized measurements, random factor...



Contributions & Conclusion

■ Contributions

1. PoC of IETF Real-Time Transport Protocol (RTP) for streaming simulation data
2. CoSiF – A reusable library for distributed real-time simulation
 1. Improved calculation of Dynamic Phasor Coefficients by moving window average
 2. Fidelity Improvements & Bug Fixes
3. **GD-RTS Simulation Infrastructure for ERIGrid II:
DTU, TUD, SINTEF & RWTH**

■ Conclusions

- ≡ Internet routing is critical for GD-RTS and can often be improved
- ≡ Sending rate adaptation during a GD-RTS should be avoided
 - = But good for tuning parameters upfront
- ≡ Time-synchronized measurements are crucial for distributed PHIL
 - = Compensation requires accurate measurements

Lessons Learned

- DTU's SYSLAB is a great and versatile environment!
- Automation was really useful

- We tried to cover too many topics in a *single* TA
 - ≡ Tri-lateral TAs are nice for collaboration but should target a single objective
 - ≡ We actually worked on separate topics

- Future Plans
 - ≡ More tests with off-nominal frequencies at the interface
 - ≡ FPGA / PCIe-based DRTS interfaces
 - ≡ Improved measurements for distributed PHIL

Acknowledgements

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- ≡ Prof. Palensky
- ≡ Rishabh Bhandia

■ DTU Denmark

- ≡ Prof. Kai Heussen

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- ≡ ERIGrid H2020
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- ≡ RESERVE H2020

■ Software Development / Distribution

- ≡ Fein Aachen e.V.



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Contact

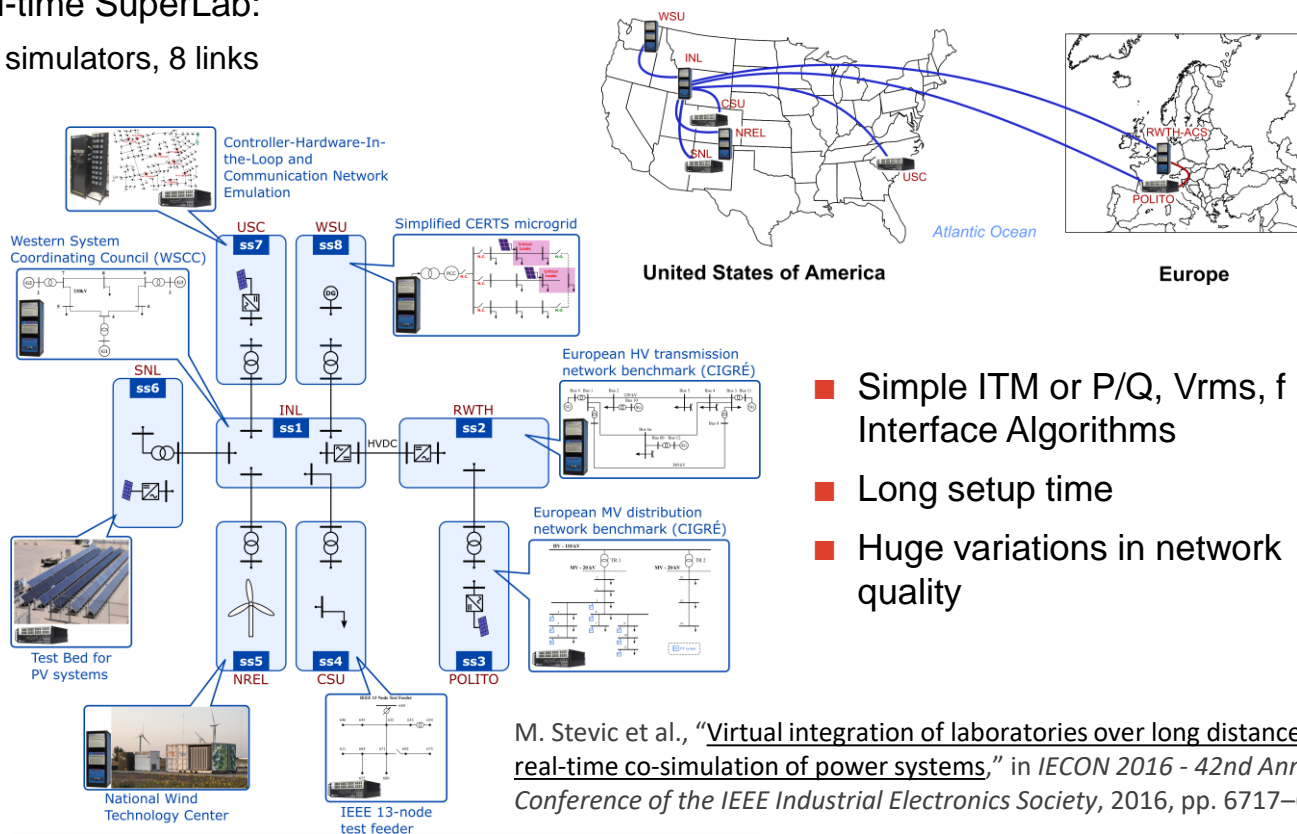
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Background / Motivation

■ Global Real-time SuperLab:

≡ 8 sites, 10 simulators, 8 links

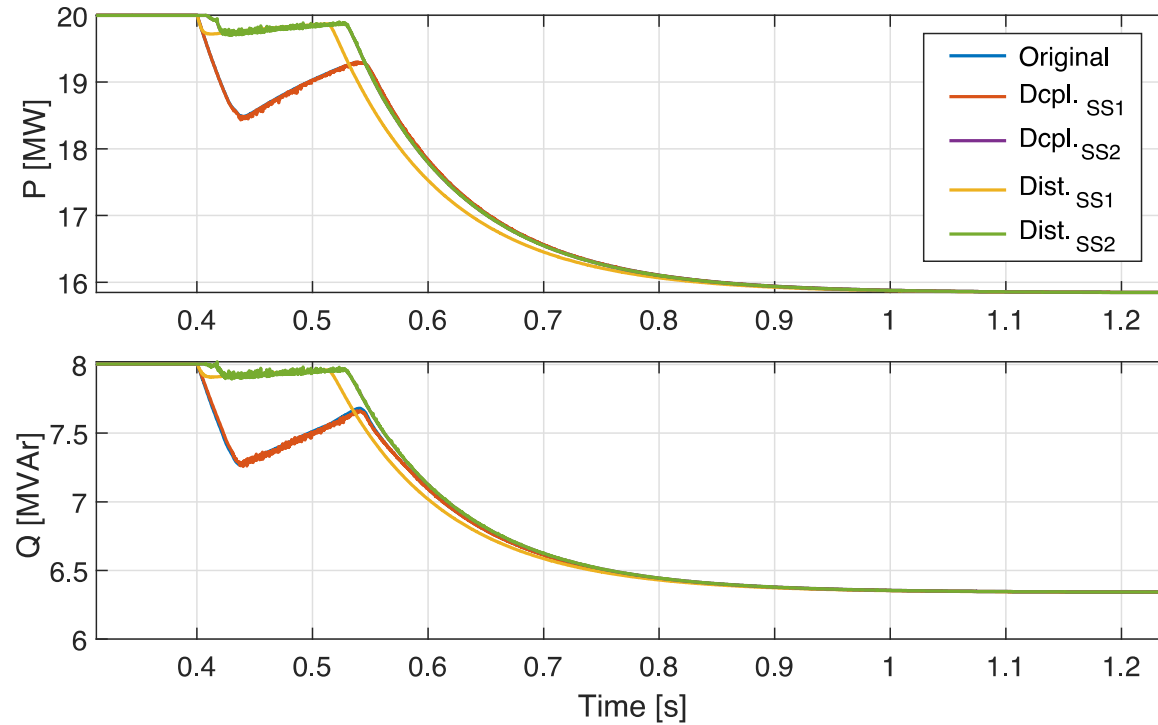


- Simple ITM or P/Q, Vrms, f Interface Algorithms
- Long setup time
- Huge variations in network quality

M. Stevic et al., “Virtual integration of laboratories over long distance for real-time co-simulation of power systems,” in *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, 2016, pp. 6717–6721.

Simulation Results: P/Q RMS

■ Change of source magnitude in SS1 (left side)



Fidelity Improvements I

- Mismatch in DFT window length for 60 Hz systems
- Fundamental period of 60 Hz is not evenly dividable by a $T_s = 50 \mu s$ time-step

- Optimal Simulation Timestep: $T_s = (1/f_0)/334 \approx 49,9 \mu s$.

TABLE I
IMPACT OF THE DFT WINDOW LENGTH ON INTERFACE QUANTITIES.

DFT window			Interface quantity			
			$V_{A,rms}$ [kV]		$I_{A,rms}$ [A]	
T_s [μs]	N	$length$ [ms]	SS1	SS2	SS1	SS2
50	333	16.65	136.7	136.0	51.64	51.9
50	334	16.7	136.6	137.9	52.56	52.05
49.9	334	16.6666	136.6	136.6	52.56	52.56

- Uneven time-steps might cause other issues in relation to synchronization of simulators

Fidelity Improvements II

- Mismatch in active / reactive power due to internal time-step delays between network solution and control systems of DRTS
- Phase compensation for controlled sources required

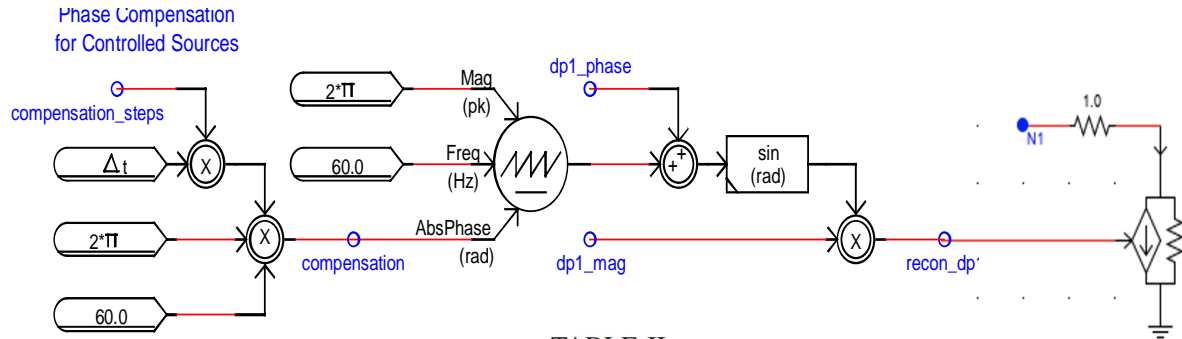
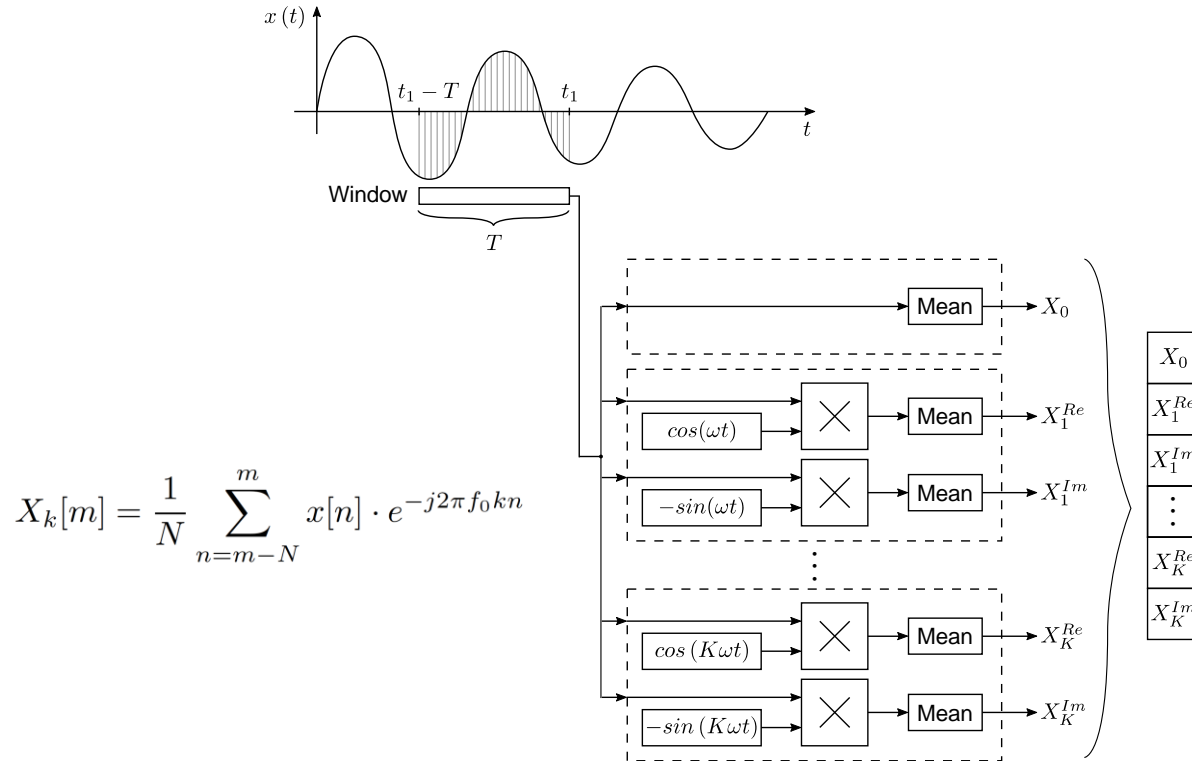


TABLE II
IMPACT OF PHASE COMPENSATION OF SOURCE SIGNALS ON
STEADY-STATE POWER BALANCE AT THE CO-SIMULATION INTERFACE

n_{SS1} [T_s]	n_{SS2} [T_s]	P_{SS1} [MW]	Q_{SS1} [MVar]	P_{SS2} [MW]	Q_{SS2} [MVar]	S [MVA]	V_{rms} [kV]
0	0	19.16	9.846	20.0	8.003	21.54	227.7
1	1	19.52	9.118	20.0	8.003	21.54	227.9
2	1	19.69	8.749	20.0	8.003	21.54	227.9
3	2	20.0	8.003	20.0	8.003	21.54	228.1

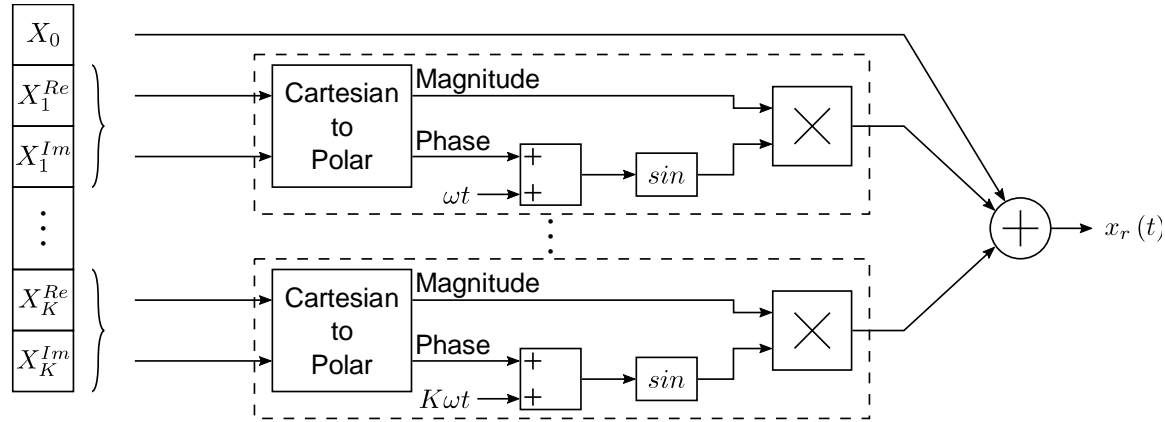
Dynamic Phasor Interface Algorithm (DP-IA)



Calculation of Dynamic Phasor Coefficients from Time-domain Signals.

Dynamic Phasor Interface Algorithm (DP-IA)

$$x[n] = \sum_{k=0}^K X_k[n] \cdot e^{j(2\pi f_0 kn + \varphi_c)}$$



Reconstruction of Time-domain Signals from Dynamic Phasor coefficients.