ADVANCED PROTOTYPE PLATFORM FOR A WIRELESS MULTIMEDIA LOCAL AREA NETWORK

Kimmo Tikkanen, Marko Hännikäinen, Timo Hämäläinen, and Jukka Saarinen
Digital and Computer Systems Laboratory, Tampere University of Technology
Hermiankatu 3 A, FIN-33720 Tampere, FINLAND
Tel: +358 3 365 2111; Fax: +358 3 365 4575
e-mail: kimmot@cs.tut.fi, markoh@cs.tut.fi, timoh@cs.tut.fi, jukkas@cs.tut.fi

ABSTRACT

This paper presents an advanced version of a configurable demonstrator platform developed for a new wireless local area network called TUTWLAN. TUTWLAN is targeted for limited service areas with stationary or portable terminals. Applications range from simple wireless sensors to multimedia laptops. The network supports the different Quality of Service (QoS) requirements of these applications. The improved development platform has been designed because of the restrictions discovered in the first prototype. The new platform provides better testing environment for developing Medium Access Control (MAC) protocols for TUTWLAN and for designing embedded stand-alone applications. Furthermore, various other designs can be tested, for example hardware implementations of encryption algorithms. Both the new and the old prototypes consist of a Digital Signal Processor (DSP), external memory modules for the DSP, and a Field Programmable Gate Array (FPGA) circuit. The platform is connected to a radio module and can be attached to a host computer using Peripheral Component Interconnect (PCI) bus. Compared to the original platform, the new prototype contains more memory, a faster and larger FPGA, and a higher bit-rate radio.

1 INTRODUCTION

A Wireless Local Area Network (WLAN) provides flexible data-services with fast and easy network management for private areas, such as homes, offices, and for limited public access areas, such as libraries and airport lounges. WLANs have been emerging to the markets for several years, but have still not been able to compete with traditional wired LANs. WLAN solutions have gained popularity in specific sectors, such as service and education, where the movement of users is required. However, the WLAN technology has been suffering from low performance, high costs, limited communication range, and lack of compatibility [1].

WLAN standards IEEE 802.11 [2] and High Performance Radio Local Area Network (HIPERLAN) [3] are now available and the specification work proceeds towards higher bit-rates. However, these general-purpose systems could be too complex and expensive for simple, wireless applications and on the other hand too general for specific user services, such as real-time video. Consequently, a new low-cost, reduced complexity TUTWLAN system is being designed and implemented in Digital Systems Laboratory at Tampere University of Technology (TUT) [4] [5]. TUTWLAN is targeted for a broad range of services, including multimedia and real-time circuit switched data. In the TUTWLAN development the goal is to achieve a seamless design flow from high-level requirements to the realisation of a physical device. For TUTWLAN prototyping, a Medium Access Control (TUTMAC) protocol has been designed and implemented with a formal, high abstraction level Specification and Description Language (SDL) [6].

In the TUTWLAN development project, a demonstrator platform has been designed to provide a testing environment for the TUTMAC protocol testing. Currently, the first platform has been implemented and TUTMAC testing is being performed. An advanced version of the platform has now been designed. The scope of this paper is on the implementation of the hardware for this advanced prototype.

This paper is organised as follows. First, an overview of the first platform architecture is presented. After that the advanced platform architecture is depicted and compared with the first platform version. Arguments for design choices made are stated. Furthermore, the most important design considerations are presented. Conclusions summarising the key development experiences and design issues are given in the last section.

2 ORIGINAL DEMONSTRATOR PLATFORM ARCHITECTURE

The block architecture of the original demonstrator platform is depicted in Figure 1 together with components used for implementing these functional blocks. The platform consists of a *radio sub-system*, *radio interface*, *MAC*, and *host interface* modules [5]. The modularity of the system architecture allows different configurations according to desired terminal properties. For example, the radio module can be replaced with another type of radio or with an infrared transceiver by reconfiguring the radio interface.

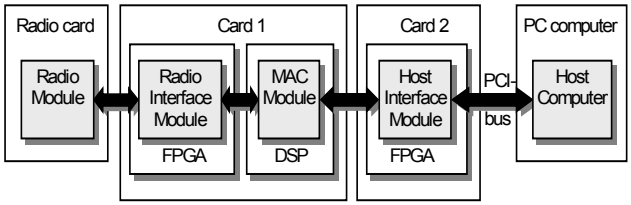

Figure 1. Hardware modules of the first platform.

A host computer is utilised for downloading system configurations into the various modules of the platform. The host computer is also used for verifying the operation of the demonstrator and for measuring the performances of tested configurations. The host computer is a PC with Microsoft Windows NT operating system. Furthermore, interoperability with legacy Internet applications and interconnection to wired LANs are achieved via the host computer. The host computer contains several TUTWLAN specific software blocks, such as device drivers, protocol drivers, and management software [5].

PCI bus was chosen for interconnecting the host computer and the MAC module due to its very high communication bandwidth, low-latency, and support for PCs, workstations, and various embedded systems (industrial PCI). The host interface module is implemented using Xilinx XC4010E FPGA [7]. The logic inside the interface is designed with Very high-speed integrated circuit Hardware Description Language (VHDL), which ensures convenient high-level description of hardware functions and fast reprogramming.

The MAC module consists of a DSP processor, in which the TUTMAC protocol software module is embedded. DSP chosen for the MAC module is Analog Devices' ADSP-21062 processor that contains 2 Mbits on-chip memory and 40 MIPS of processing power [8].

The most important task of the radio interface module is to interconnect the signal lines and buses between the MAC processor and the radio sub-system. This function adapts the non-synchronised data streams by buffering and manages the control line handshaking between the two modules. If a radio module is changed, a new configuration described in VHDL is loaded into the interface chip, which allows testing various WLAN radio modems with the TUTMAC protocol.

In addition, the radio interface module is used for accelerating MAC operations having critical timing requirements. Examples of these tasks are the calculation of a Cyclic Redundancy Check (CRC) sum over a received frame, Forward Error Coding (FEC), synchronisation to the used Time Division Multiple Access (TDMA) of the medium, and data encryption algorithms. These operations are not viable to be computed on the system processor because of the resulting delays. A Xilinx XC4013E FPGA chip is used to implement the radio interface [7].

The radio module in the prototype platform utilises a 2.4 GHz frequency band with a Direct Sequence Spread Spectrum (DSSS) technique. Currently, a 1 Mbit/s link speed is used. The radio module chosen for the demonstrator platform is PRISM1RC-EVAL, manufactured by Intersil [9].

3 NEW DEMONSTRATOR PLATFORM ARCHITECTURE

An advanced prototype platform for TUTWLAN testing is being developed because of certain testing challenges were encountered. These challenges are discussed in the following sections. Furthermore, new improvement ideas were revealed during the development and testing of the first TUTWLAN prototype. For example, the lack of testing points in the first prototype was noticed. Furthermore, programs generated using SDL require larger program memory on the MAC processor. Also, the FPGAs of the first platform should have more capacity and performance.

The first prototype was implemented using two Printed Circuit Boards (PCB). In order to lower manufacturing costs these two PCBs were integrated on a single PCB for the advanced prototype. Architecture and the used components of the new platform are depicted in Figure 2. The figure also illustrates the placement of the original prototype's functional blocks as shaded blocks.

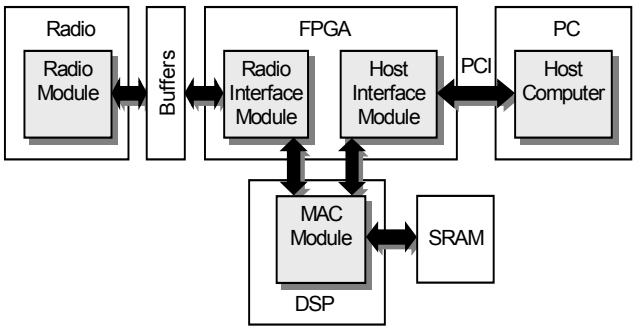

Figure 2. Components and functional blocks of the advanced platform.

3.1 FPGA of the Advanced Platform

In the new prototype, the host interface and the radio interface functional modules are located on a single FPGA compared with the two separate FPGAs of the first prototype. In the new prototype, these functional blocks are implemented with a larger and faster Xilinx XCV800 FPGA [10]. Because the new prototype was designed using a single PCB, two separate FPGAs were found to be too large in their physical dimensions to fit on a same PCB with other needed components in the new prototype.

More FPGA capacity was needed because the host interface module took about 80% of the logic cells on the old FPGA and the radio interface module needed about 75% of its FPGA's capacity. Consequently, it was impossible to add any new functional blocks, such as encryption modules, in the old FPGAs. For example, a well-known encryption algorithm RC4 [14] implemented with a Xilinx 4013E FPGA takes about 40% of its logic cells.

Implementation of more reliable and more secure Triple-DES [14] encryption algorithm is not even possible using this FPGA, since it requires more logic cells than the FPGA provides. The total number of logic cells on the new FPGA is about twenty times larger than the number of the logic cells on the two old FPGAs together.

Performance of the old FPGAs has been a restriction in the old prototype. Written VHDL-models had to be optimised carefully in order to achieve the desired performance level. The new FPGA is considerably faster than the older ones. Therefore, the performance of the FPGA should not prevent the testing of TUTMAC protocol with complete functionality.

The new FPGA also has a lower 3.3V supply compared with the original platform. However, the radio module still requires the same 5V signal levels. New challenges of design were faced when interfacing the radio sub-system to the FPGA. As a result, buffers between these components have to be added. Furthermore, the use of several supply voltages in a same PCB requires adding of several separate power supply layers to the PCB.

Logic inside the new FPGA is designed using VHDL-codes of the first prototype. Only minor changes to the top hierarchy level are needed, e.g. pin mappings have to be changed and component names have to be updated to correspond component names in the new VHDL-libraries of FPGA.

3.2 TUTMAC Protocol Requirements

The TUTMAC protocol is implemented in a separate development environment using SDL. The formal SDL description can be automatically converted into C-language for implementation, but this generated code is usually not space optimised.

In TUTWLAN research, the design tool for SDL has been SDT (versions 3.4 and 3.6) manufactured by Telelogic [11]. SDT belongs to the Telelogic Tau product family. The Cadvanced code generator of the tool has been used for generating the TUTMAC protocol application. SDT also contains the Cmicro code generator that produces a further optimised code and is therefore more suitable for programming embedded systems. However, not all the SDL properties, such as remote procedure calls, enabling conditions, continuous signals, and declaring of infinite number of process instances can be utilised with Cmicro.

The TUTMAC protocol implemented using SDL requires more memory from the target DSP than the original platform provides. The compiled protocol for a TUTMAC base station protocol needs 490 kbytes memory for the program code. In addition, 61 kbytes are required for static variables and approximately 100 kbytes for dynamic memory allocations.

3.3 Processor and Memory Selection

Because of high memory requirements of the generated TUTMAC protocol, DSP chosen for the MAC module of the advanced platform is Analog Devices' ADSP-21060L processor, that is fully compatible with the old platform processor [8]. The new DSP contains 4 Mbit on-chip memory, which is twice as much as the processor in the first prototype. The selected DSP has also 3.3V supply voltage which lowers the power consumption and makes the interfacing with the selected FPGA easier.

In addition to the large internal memory, a large external memory for DSP has been added on the prototype PCB. The selected memory is White Electronic Designs EDI8F32512V-MZ static RAM (SRAM) modules [12]. This memory type was chosen because of its fast access time and high storage capacity. Each memory module provides a 512k x 32 bit memory block. Furthermore, each SRAM-module has two selection signals (cs0 and cs1). By using these signals the module can be used as two separate blocks, both having 512k x 16 bit capacity. The width of the DSP data path is 48 bits. Therefore, three separate memory modules connected to form a 1M x 48-bit memory are used on each PCB. Thus, the total capacity of the DSP program memory is now 6 Mbytes.

Connections between DSP and SRAM-modules are depicted in Figure 3. DSP uses two logically separate external memory blocks. Selection signals (MSX0 and MSX1) are used to choose the corresponding SRAM-modules. The first external memory block of the DSP consists of the SRAM-module 1 and half of the SRAM-module 2. Correspondingly, the second memory block consists of SRAM-module 3 and half of the SRAM-module 2. The advanced platform is expected to provide enough memory capacity to enable testing of embedded applications in addition to the TUTMAC protocol.

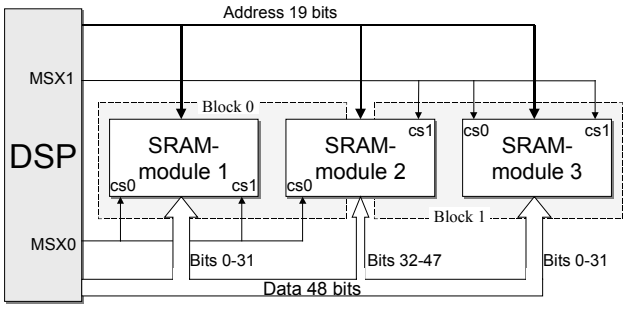

Figure 3. Connections between DSP and SRAM-modules

3.4 Radio Module

Radio used in the advanced prototype is changed to HWB1151-EVAL from Intersil [13], because of its higher 11 Mbit/s data rate compared with the original 1 Mbit/s rate. The radio of the previous prototype can also be used, since the signals and the connector of the new radio are compatible with it. Only the logic inside the radio interface module must be modified. The 11 Mbit/s data rate results into challenges for the prototype design since the transfer speed between the radio interface module and the MAC module might be a bottleneck. However, increasing the

transfer clock rate between the radio interface module and the MAC module should solve this problem.

In the future, the radio module might be replaced with another type of radio sub-systems, such as Bluetooth system [18]. This requires the reconfiguration of the radio interface module.

3.5 Design Considerations

Due to the higher transfer clock rate between the radio module and the radio interface, the electromagnetic compatibility (EMC) design rules must be followed [15]. For example, crosstalk, power-supply noise, and transmission line reflections should be taken into account. Several separate PCB ground planes are used to reduce the problem of crosstalk. Power-supply planes are also used to reduce the power-supply noise. Furthermore, several decoupling capacitors are located near every component that is expected to use large amount of electric current. For example, 33 capacitors are located near the FPGA package according to recommendations of the manufacturer [16]. Signal reflections are reduced using termination resistors for critical signals. EMC design rules are taken into account also in the other parts of the PCB design.

Testing of the first prototype revealed that more test points are needed in PCB to make testing and debugging easier. Therefore, several pin headers are added to the new prototype. For example, all the signals between DSP and FPGA can be measured with a logic analyser system [17]. Test points also enable the using of the chip-on-board emulation of the DSP.

4 CONCLUSIONS

TUTWLAN system has been developed to provide a wireless data-transfer service for office and home environments and for restricted public areas. The most important system requirement has been to achieve a reduced complexity system for supporting real-time, multimedia type of services.

The advanced prototype platform has been developed for providing a general-purpose wireless development platform. Besides the main TUTMAC protocol, by using this platform it is possible to test different types of communication protocols and systems, such as other WLANs and Bluetooth. Through test pins it is also possible to add other kinds of components to the advanced prototype, for example memory can be added near the FPGA that can consequently use this memory without the DSP. With this configuration, various processor models can be tested inside the FPGA.

Currently, the first network demonstrator containing two wireless platforms is under testing and verification. The second prototype platform is under construction and will be completed and operational during the spring 2000. The development continues by porting the VHDL codes of the first prototype to the improved platform. Next, the second prototype is tested in target operational environments. In the future, different MAC protocols and embedded applications generated using SDL are tested in the platform. It is expected that with the new prototype platform, wireless systems with quite high data rates can be implemented.

REFERENCES

[1] Nathan J. Muller, “Wireless Data Networking”, Norwood, Artech House, 1995.

[2] IEEE P802.11 D5.0, IEEE Standard for local and metropolitan area networks: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications, IEEE Standards Department, 19.7.1996.

[3] ETS 300 652, Radio Equipment and Systems (RES); High Performance Radio Local Area Network (HIPERLAN), Type 1; Functional specification, October 1996.

[4] M. Hännikäinen, J. Knuutila, A. Letonsaari, T. Hämäläinen, J. Jokela, J. Ala-Laurila, J. Saarinen, “TUTMAC: A Medium Access Control Protocol for A New Multimedia Wireless Local Area Network”, Proceedings of the Ninth IEEE International Symposium on Personal, Indoor and Mobile Radio Communications (PIMRC'98), USA, September 8–11, 1998, pp. 592-596.

[5] M. Kari, M. Hännikäinen, T. Hämäläinen, J. Knuutila, J. Saarinen, “Configurable Platform for a Wireless Multimedia Local Area Network”, Proceedings of the 5th International Workshop on Mobile Multimedia Communications (MoMuC'98), Germany, October 12-14, 1998, pp. 301-306.

[6] CCITT Specification and description language, ITU-T recommendation Z.100, March 1993.

[7] Xilinx, “XC4000E and XC4000X Series Field Programmable Gate Arrays”, Product Specification, 1997.

[8] Analog Devices Inc., “ADSP-2106X SHARC User’s Manual”, 1997.

[9] Harris Semiconductor, “Wireless Handbook”, 1997

[10] Xilinx, “The Programmable Logic Data Book 1999”, 1999.

[11] Telelogic AB, “Telelogic Tau 3.6 User’s Manual”, 1999.

[12] White Electronic Designs Corporation, “EDI8G32512V Data Sheet”, 1999.

[13] Intersil, “2.4GHz 11Mbs MACless DSSS Radio HWB1151 User’s Guide”, 1999.

[14] Bruce Schneier, “Applied Cryptography: Protocols, Algorithms and Source Code in C”, 2nd edition, John Wiley & Sons, Inc., 1996.

[15] Henry W. Ott, “Noise Reduction Techniques in Electronic Systems”, John Wiley & Sons, 1988.

[16] Xilinx, “Powering Virtex FPGAs”, 1999.

[17] Agilent Technologies, “HP 16600A and 16700A Series Logic Analysis System Mainframes”, 1999.

[18] Specification of the Bluetooth System – Core, v1.0 B, December 1999.