Principle and Topology Derivation of Single-Inductor Multi-Input Multi-Output DC-DC Converters

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***Abstract*— Single-inductor multi-input multi-output (SI-MIMO) dc-dc converters are attractive in the engineering applications due to the advantage of high power density and low cost. In order to explore as many as possible SI-MIMO topologies, this paper proposes a simple and effective topology derivation principle which only requires three steps. Firstly, three basic cells consisting of a single inductor and multiple sets of unidirectional switches as well as inputs/outputs are proposed. Secondly, integrate them with the inductor branch of the typical single-input single-output converters. Finally, implement the topology simplification by removing unnecessary switches/diodes. Based on the proposed principle, a large number of SI-MIMO topologies are derived from buck, boost, buck-boost and non-inverting buck-boost converters in the paper. With more topology choices having different performance characteristics, it is very beneficial for engineers to gain an optimized design that a preferred one can be selected out after comprehensive comparison. As an example, topology comparison and selection among a family of single-inductor single-input dual-output converters is also conducted in the paper. Besides, performance analysis, design considerations and simulation/experiment results of the selected optimum topology are demonstrated in detail to verify its advantages.**

***Index Terms*— Multi-input multi-output (MIMO), principle, single-inductor, topology derivation.**

I. Introduction

In many industrial applications such as photovoltaics [1, 2], electric vehicles [3], data processing centers [4], personal computers [5] and so on [6-8], multiple ports with various voltage levels are demanded. In order to achieve the voltage regulation as well as the power control among different ports, multiple independent single-input single-output (SISO) converters can be simply employed. However, owing to the large number of components, high overall cost and large system volume will be incurred. To address this problem, two types of integrated multi-port dc-dc converters have been proposed, in which the number of semiconductor devices and inductors is effectively reduced, and so that both the cost and power density are improved.

Based on the typical buck [9, 10], boost [11] and buck-boost [12] converters, integrated *N*-port converters with semiconductor devices multiplexed were proposed, which only need *N* switches/diodes. In comparison with the conventional solution with *N* independent SISO converters including 2*N*-2 switches/diodes, the number of semiconductor devices is *N*-2 reduced and hence lower cost can be achieved. Aiming to explore more favorable topologies, a systematic synthesis method was further proposed in [13]. However, because the magnetic components accounting for a very large proportion in the overall volume and weight are not optimized, the improvement of power density is limited in the integrated multi-port converters with semiconductor devices multiplexed.

Fortunately, the inductor can also be multiplexed and only one inductor is employed in the single-inductor multi-input multi-output (SI-MIMO) converter. The inductor functions as a common power flowing path for different ports. Consequently, high power density is achieved in the SI-MIMO converters, which attract increasing attention in the recent years. In general, researches of SI-MIMO converters mainly focus on two aspects, new control and new topologies, to improve converter performance. In terms of the control strategy, there are three common modulation strategies: discontinuous conduction mode (DCM), continuous conduction mode (CCM) and pseudo-CCM/DCM. In [14], the converter is designed to work in DCM with multiple energizing cycles per switching period. It functions similarly as multiple independent SISO converters, and thus good dynamic response is achieved. However, under heavy load conditions, the peak inductor current will become large, which deteriorates both the current stresses and conduction losses. In order to alleviate this problem, the SI-MIMO converters can work in CCM with one energizing cycle per switching period. Nevertheless, because the power transfer among different ports are dependent on a common inductor, severe cross regulation problem will be caused. Based on this, multiple new control schemes had been figured out in the past researches, aiming to achieve reduced cross regulation. Besides of the CCM and DCM, the SI-MIMO converters can also work in pseudo-CCM/DCM with an extra switch connected between the inductor [15, 16]. It makes a compromise between the current stresses and the cross regulation problem. In a word, control strategies of SI-MIMO converters have been widely studied in the past.

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While on the other hand, in terms of the topology configurations, only several SI-MIMO dc-dc converters have been proposed in the existing researches. Six types of single-inductor single-input dual-output (SI-SIDO) topologies based on buck [17-19], boost [17, 20], buck-boost [17] or non-inverting buck-boost [17, 21, 22] converters were presented, and four types of single-inductor multiple-input single-output (SI-MISO) topologies based on buck [23], boost [24], buck-boost [23] and non-inverting buck-boost [25] converters were proposed. In addition, their counterpart multi-input multi-output converters were developed in [26-32] by simply connecting multiple additional input/output branches in parallel. Although the existing topologies can provide favorable performances for the specified applications, they cannot always be the best choices for various applications with different system requirements. For example, for the applications having several inputs/outputs with different voltage/power levels, the direct parallel connection of additional input/output branches is usually not a good solution. Actually, in order to effectively select a preferred converter for an engineering application, as many viable topologies as possible should be provided and compared. However, until now, the principle to derive SI-MIMO topologies is kept unclear and only a limited number of topologies is available.

From above, SI-MIMO converters have the advantages of low cost and high power density, which are attractive in the engineering applications. Their control strategies have been widely discussed in the relevant researches to improve the dynamic characteristics. But for the topology configurations, only several ones are available, and more viable topologies are desired so that a preferred one can be selected out after comprehensive comparison. With this demand, a novel principle of deriving a large number of SI-MIMO topologies from typical buck, boost, buck-boost and non-inverting buck-boost SISO converters is proposed in the paper. Only three steps are needed, and thus it is simple to be implemented. To gain a better understanding, a family of SI-SIDO, single-inductor dual-input single-output (SI-DISO) and single-inductor dual-input dual-output (SI-DIDO) topologies are derived and demonstrated, including the ones presented in [17-22]. Besides, the obtained SI-SIDO boost converters are taken as an example to be compared, and an optimum one is finally chosen for a specific application, whose performance analysis, design considerations and simulation/experiment verification are also illustrated in detail.

II. Principle and Topology Derivation

In this section, the principle and topology derivation of SI-MIMO converters from the typical buck, boost, buck-boost and non-inverting buck-boost SISO converters in Fig. 1 will be depicted in detail, which only needs three steps and thus can be implemented easily. Besides, some of the derived topologies can be further simplified under appropriate working conditions to obtain reduced number of semiconductor devices.

A. Principle

Firstly, three basic MIMO cells (MIMO_1, MIMO_2, MIMO_3) with p outputs and q inputs are proposed in Fig. 2, according to the fundamental operation principle and topology structure of the existing SI-MIMO converters. By connecting multiple inputs/outputs and unidirectional switches with the outflow, inflow or both ports of inductor as shown in Fig. 2 (a) ~ Fig. 2 (c), the current i_L will be multiplexed and will flow into different inputs/outputs during the time interval when their corresponding switches conduct.

Secondly, integrate the MIMO cells in Fig. 2 with the inductor branch of buck, boost, buck-boost and non-inverting buck-boost converters. In order to achieve a unified topology derivation process, the inductor branch of four typical SISO

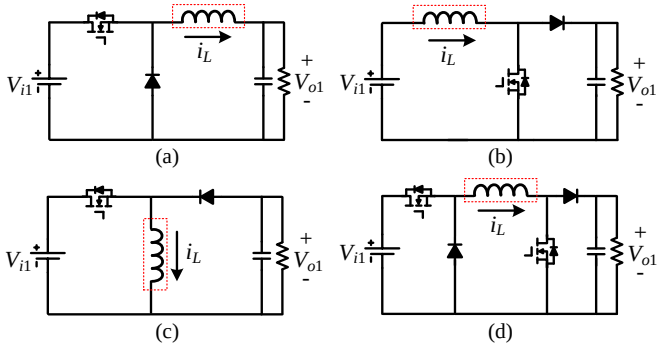


Fig. 1. Four typical SISO dc-dc converters: (a) buck, (b) boost, (c) buck-boost and (d) non-inverting buck-boost.

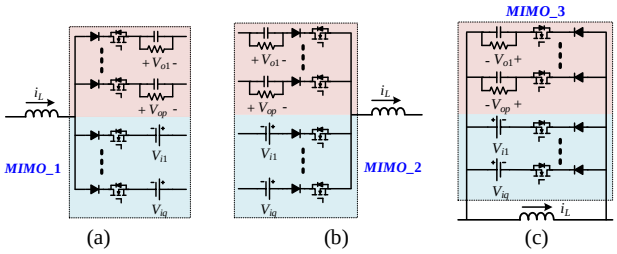


Fig. 2. Three MIMO cells with connection to different ports of the inductor: (a) outflow, (b) inflow and (c) both.

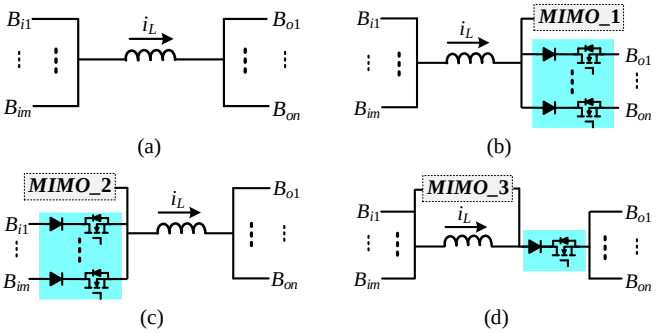


Fig. 3. Three types of SI-MIMO topologies deriving from the four typical SISO converter: (a) SISO, (b) MIMO_1, (c) MIMO_2 and (d) MIMO_3.

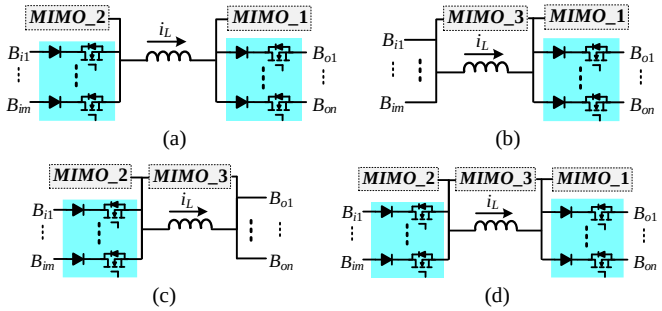


Fig. 4. SI-MIMO topologies with the combination of three MIMO cells: (a) MIMO_1+MIMO_2, (b) MIMO_1+MIMO_3, (c) MIMO_2+MIMO_3 and (d) MIMO_1+ MIMO_2+MIMO_3.

converters are expressed in a general form, as shown in Fig. 3 (a). According to Fig. 1, the values of m and n are either 1 or 2. Then, the integration of one MIMO cell and the inductor branch is depicted in Fig. 3(b)~(d). For the MIMO_1 cell, it is added at the outflow port of inductor, and an extra unidirectional switch is added in each original branch B_{o1}~B_{on}. These additional switches along with the switches in MIMO_1 cell are used to ensure that inductor current i_L can only flow into one path at any time. The integration is similar for the MIMO_2 cell as shown in Fig. 3(c), while it is a little different for the MIMO_3 cell. From Fig. 3(d), only an extra unidirectional switch is needed for the integration of MIMO_3 cell, because it is parallel connected with the inductor. Moreover, two or three different MIMO cells can also be simultaneously integrated with the SISO converters in a similar manner, as shown in Fig. 4. It is noted that the extra unidirectional switch connecting with MIMO_3 in Fig. 3(d) can be removed when it is combined with MIMO_1, MIMO_2 or both, as illustrated in Fig. 4(b)~(d), because there already have unidirectional switches in branches B_{i1}~B_{im} or B_{o1}~B_{on}.

For the SI-MIMO topologies in Fig. 3(b)~(c) and Fig. 4(a)~(d) which employ MIMO_1 cell or MIMO_2 cell, one port of each output V_{o1}~V_{op} or input V_{i1}~V_{iq} is suspended. Theoretically, the suspended ports can be connected to any nodes of typical SISO converters other than the two nodes of inductor, and hence more than one SI-MIMO topology can be correspondingly developed. In the following section, it is shown that with the integration of MIMO_1 cell or MIMO_2 cell, 2 SI-SIDO/SI-DISO topologies can be derived from the buck, boost as well as buck-boost converters, and 3 topologies for non-inverting buck-boost converters.

Finally, simplify the above derived SI-MIMO topologies by removing unnecessary switches. It is obvious that there are unnecessary switches since many extra unidirectional switches are added. Some of them are reduplicated and some are useless. As shown in Fig. 5, two mosfets/diodes connected in series are reduplicated and it can be simplified by deleting the reduplicated one. Furthermore, denote the voltage across the unidirectional switch consisting of a mosfet and a diode as v_s. If it is larger than or equal to zero all the time, the diode will always be forward biased and thus it can be removed. On the other hand, if v_s is always less than or equal to zero, the parallel diode of mosfet conducts all the time and it can also be removed.

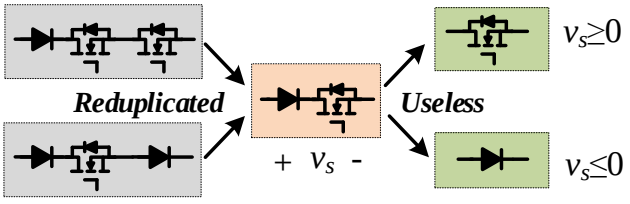


Fig. 5. Simplification of switches.

B. Topology Derivation

With the above principle, various SI-MIMO converters can be easily derived. Taking the combination of boost converter and MIMO_3 cell with one output branch (p=1, q=0) as an example, its detailed topology derivation process is demonstrated in Fig. 6. After integrating MIMO_3 cell with the boost converter in Fig. 6(a), the extra unidirectional switches are moved to connect in series with switch S_1 and diode D_{s2} in Fig. 6(b). According to the simplification in Fig. 5, the reduplicated mosfet and diode are deleted in Fig. 6(c). Then, by turning on the switch S_1, S_2 and S_3 one-by-one, the inductor current i_L will flow into different path in a switching period. When S_1 is off, the voltage across D_{s1} and S_1 is equal to V_{o1} and $V_{i1}+V_{o2}$ in the interval with S_2 and S_3 on, respectively. Therefore, it is always larger than zero and the diode D_{s1} can be further removed. Finally, a viable SI-SIDO topology is derived in Fig. 6(d). To the best knowledge of the authors, this topology has not been reported in previous researches.

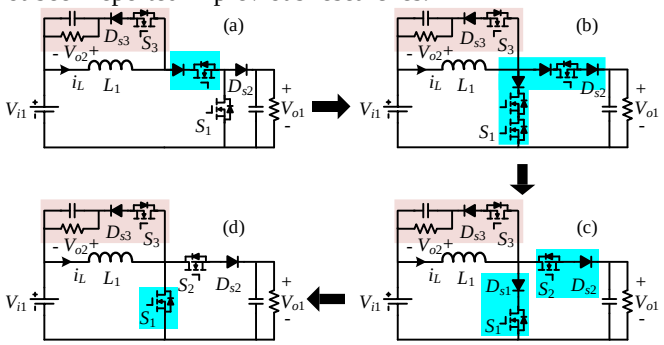


Fig. 6. Topology derivation process of SI-SIDO converter with combination of boost converter and MIMO_3 cell with one output branch.

In addition, Table 1 and Table 2 also summarize a family of SI-SIDO and SI-DISO converters derived from typical buck, boost, buck-boost and non-inverting buck-boost converters using the proposed topology derivation method. 5, 5, 3, and 7 viable SI-SIDO/SI-DISO topologies are respectively obtained, among which there is always one including MIMO_3 cell. According to Fig. 1, except for the two nodes of inductor, there are 2 other nodes in the buck, boost, buck-boost converter, and hence 2 corresponding topologies can be respectively obtained for them by integrating one MIMO_1 or MIMO_2 cell. It is noted that the SI-SIDO/SI-DISO buck-boost topologies consisting of MIMO_1 or MIMO_2 cells are the same, because its outflow and inflow ports of the inductor are equivalent. For the non-inverting buck-boost converters, there are 3 other nodes, and likewise, 3 topologies are derived with MIMO_1 or MIMO_2 cell. In these SI-SIDO/SI-DISO topologies, several ones have been presented in [17-22], and the rest are firstly found with the proposed principle in this paper. Because their performance characteristics are different, engineers can select a preferred one for a specified application after comprehensive comparison, which is very beneficial for the practical design. And in order to help engineers to better select the required topology, the basic voltage and current requirements of topologies in Table 1 and Table 2 are also respectively summarized, according to the voltage-second balance and ampere-second balance. Taking the topology in Table 1(ii) (a) as an example, the inductor voltage will be equal to V_{i1}, V_{i1}-V_{o1} or V_{i1}-V_{o1}-V_{o2} in different interval with different switch/diode on. Hence, V_{i1} must be smaller than $V_{o1}+V_{o2}$, otherwise the average voltage of inductor in a switching period won't be zero. In addition, according to the ampere-second balance of capacitor, the average current I_{o1} of first output is equal to the sum of the average current I_{o2} of second output and the current of unidirectional switch. Therefore, $I_{o1}>I_{o2}$ is obtained, and it is compulsory to use first output V_{o1} to guarantee the normal

Table 1. A family of SI-SIDO converters derived from buck, boost, buck-boost and non-inverting buck-boost converters.

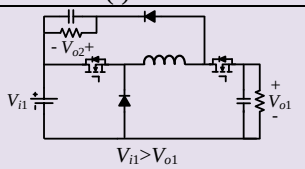
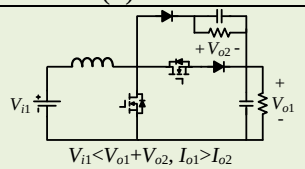
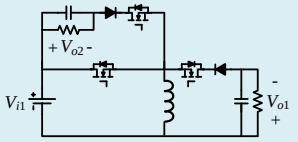
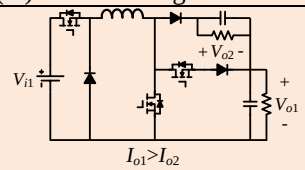
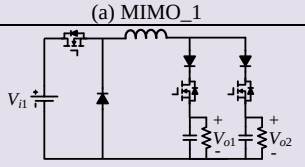
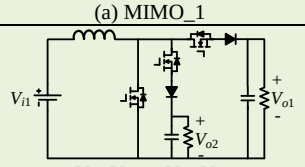
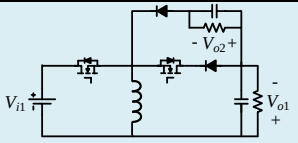
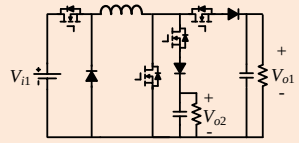
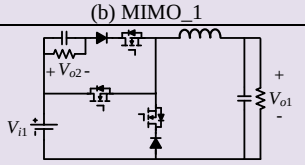
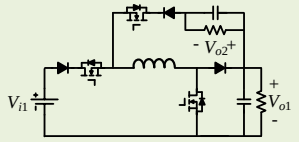
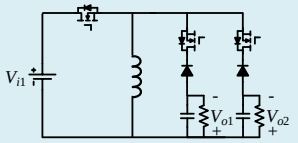
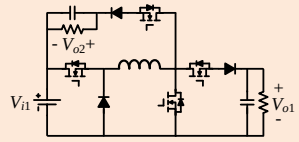
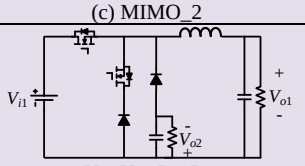
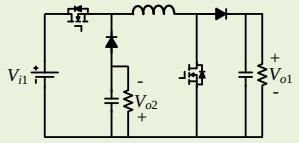
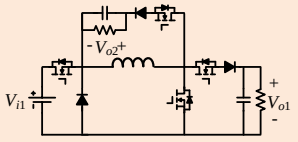
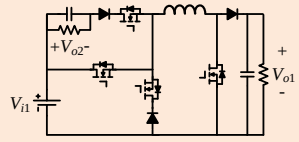
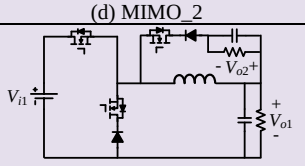
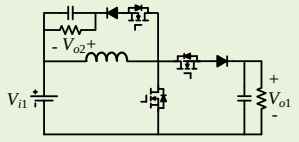
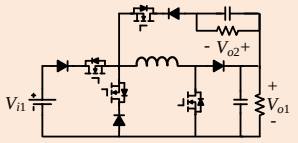
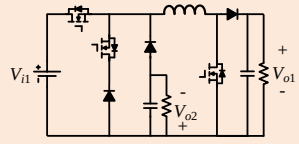
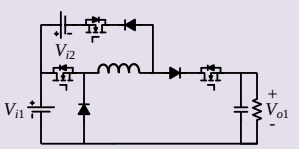
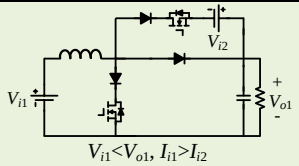
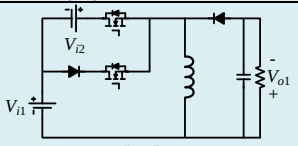
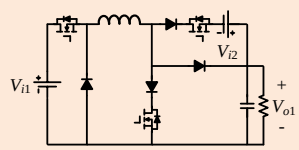
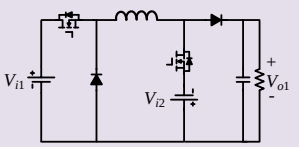
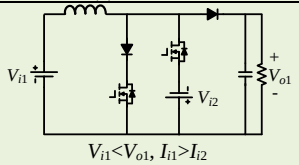
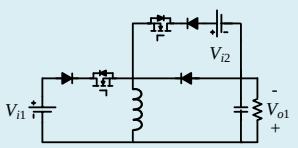
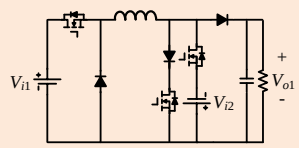
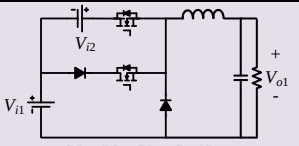
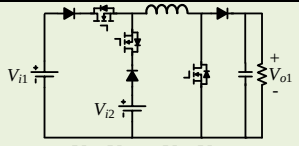
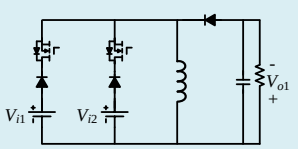
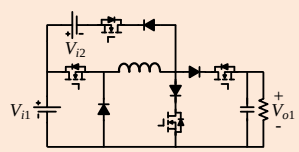
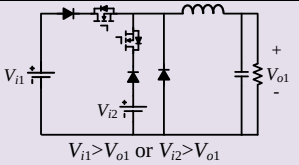
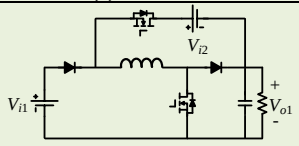
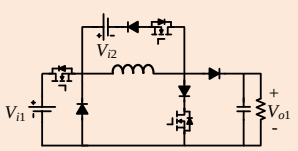
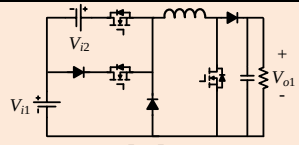
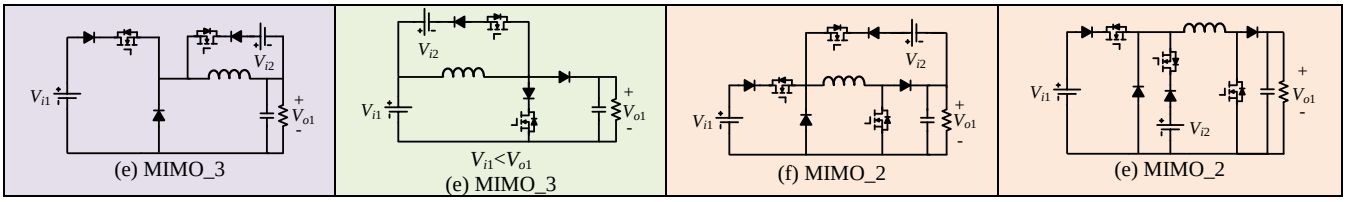
(i) buck	(ii) boost	(iii) buck-boost	(iv) non-inverting buck-boost
 $V_{i1}>V_{o1}$ (a) MIMO_1	 $V_{i1}<V_{o1}+V_{o2}$, $I_{o1}>I_{o2}$ (a) MIMO_1	 (a) MIMO_1& MIMO_2	 $I_{o1}>I_{o2}$ (a) MIMO_1
 $V_{i1}>V_{o1}$ or $V_{i1}>V_{o2}$ (b) MIMO_1	 $V_{i1}<V_{o1}$ or $V_{i1}<V_{o2}$ (b) MIMO_1	 $I_{o1}>I_{o2}$ (b) MIMO_1& MIMO_2	 (b) MIMO_1
 $V_{i1}>V_{o1}$, $I_{o1}>I_{o2}$ (c) MIMO_2	 (c) MIMO_2	 (c) MIMO_3	 (c) MIMO_1
 $V_{i1}>V_{o1}$, $I_{o1}>I_{o2}$ (d) MIMO_2	 (d) MIMO_2	 (g) MIMO_3	 (d) MIMO_2
 $V_{i1}>V_{o1}$ (e) MIMO_3	 (e) MIMO_3	 (f) MIMO_2	 (e) MIMO_2

Table 2. A family of SI-DISO converters derived from buck, boost, buck-boost and non-inverting buck-boost converters.

(i) buck	(ii) boost	(iii) buck-boost	(iv) non-inverting buck-boost
 (a) MIMO_1	 $V_{i1}<V_{o1}$, $I_{i1}>I_{i2}$ (a) MIMO_1	 $I_{i1}>I_{i2}$ (a) MIMO_1& MIMO_2	 (a) MIMO_1
 (b) MIMO_1	 $V_{i1}<V_{o1}$, $I_{i1}>I_{i2}$ (b) MIMO_1	 (b) MIMO_1& MIMO_2	 (b) MIMO_1
 $V_{i1}+V_{i2}>V_{o1}$, $I_{i1}>I_{i2}$ (c) MIMO_2	 $V_{i1}<V_{o1}$ or $V_{i2}<V_{o1}$ (c) MIMO_2	 (c) MIMO_3	 (c) MIMO_1
 $V_{i1}>V_{o1}$ or $V_{i2}>V_{o1}$ (d) MIMO_2	 $V_{i1}<V_{o1}$ (d) MIMO_2	 (g) MIMO_3	 $I_{i1}>I_{i2}$ (d) MIMO_2



operation of second output V_{o2}. It is noteworthy that the requirements can be further refined if more specified parameters are provided.

Moreover, with the increasing number of ports, more viable SI-MIMO topologies can be developed. Taking the SI-DIDO topologies based on boost converter as an example, it has 25 viable topologies in total, which can be classified into 6 types in terms of the different MIMO cells. An example topology of each type is respectively demonstrated in Fig. 7. In Fig. 7 (a)~(c), two same MIMO cells are added in the boost converter simultaneously, while two of three cells are combined in Fig. 7(d)~(f). In comparison with the SI-MIMO converters which have multiple additional inputs/outputs only connecting in parallel [26-31], the characteristics of additional ports in the newly obtained SI-MIMO topologies are diverse and thus can be a better solution for the application with different inputs/outputs.

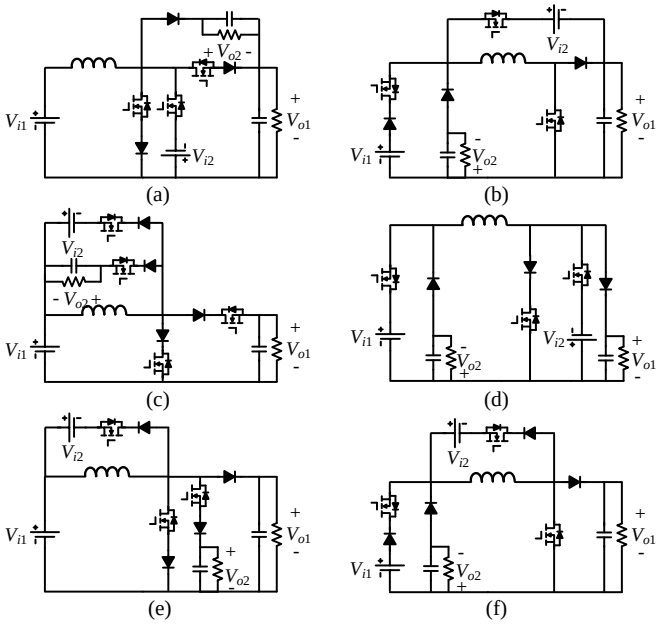


Fig. 7. SI-DIDO topologies based on boost converter with different MIMO cells: (a) MIMO_1+MIMO_1, (b) MIMO_2+MIMO_2, (c) MIMO_3+MIMO_3, (d) MIMO_1+MIMO_2, (e) MIMO_1+MIMO_3, (f) MIMO_2+MIMO_3.

C. Further Discussion

Actually, some of the above derived SI-MIMO topologies can be further simplified if they work under appropriate voltage conditions. According to Fig. 5, the mosfet or diode will become useless in their series-connected structure if its voltage is always positive or negative, and thus can be deleted. Taking the SI-SIDO converters based on boost converter in Table 1 (ii) as an example, topologies in (b), (c) and (e) can be respectively simplified into the ones in Fig. 8, Fig. 9 and Fig. 10, when the corresponding relationships among V_{i1}, V_{o1} and V_{o2} are satisfied. After simplification, the number of required semiconductor device is reduced and so is the conduction losses.

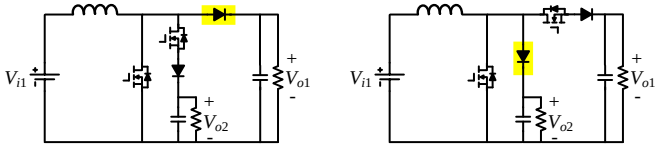


Fig. 8. Further simplification of the SI-SIDO boost converter in Table 1 (ii) (b) with voltage relationships: (a) $V_{o1}>V_{o2}$ and (b) $V_{o1}<V_{o2}$.

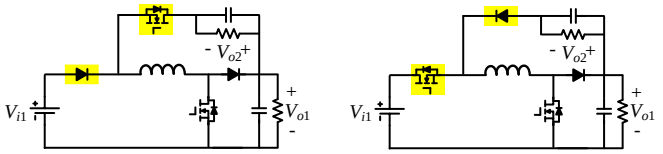


Fig. 9. Further simplification of the SI-SIDO boost converter in Table 1 (ii) (c) with voltage relationships: (a) $V_{o2}<V_{o1}-V_{i1}$ and (b) $V_{o2}>V_{o1}-V_{i1}$.

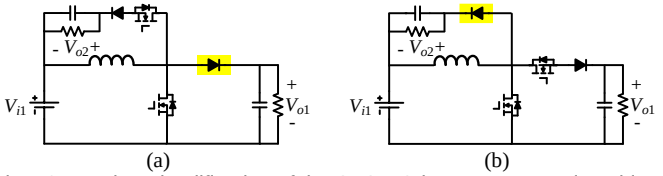


Fig. 10. Further simplification of the SI-SIDO boost converter in Table 1 (ii) (e) with voltage relationships: (a) $V_{o2}<V_{o1}-V_{i1}$ and (b) $V_{o2}>V_{o1}-V_{i1}$.

III. Topology Comparison and Performance Analysis

A. Topology Comparison

After deriving various SI-MIMO topologies, their performance characteristics will be compared and then an optimum one could be selected out for a specified application. As an example, the obtained SI-SIDO topologies based on boost converter in Table 1 (ii) and Fig. 8~Fig. 10 will be detailed compared in this section. Afterwards, topology selection is conducted for a specific application with input voltages V_{i1}=18~30V, output voltages V_{o1}=60V, V_{o2}=24V. Because V_{o2} is always smaller than V_{o1} and V_{o1}-V_{i1}, the SI-SIDO boost converters in Table 1 (ii) (a) and (d), Fig. 8(a), Fig. 9(a) and Fig. 10(a) can be employed. Their comparison results in terms of the average inductor current I_L, the working condition and the semiconductor devices, are summarized in Table 3.

For the topologies in Table 1 (ii) (a) and Fig. 8(a), their average inductor currents are smaller which is equal to the input currents I_{i1}, and the number of active semiconductor devices in conduction is also smaller. However, their working conditions are limited. The output current I_{o2} must be less than I_{o1} in Table 1 (ii) (a), and the relationship between I_{o1} and I_{o2} is restricted under the condition with $V_{o2}<V_{i1}$ in Fig. 8(a), e.g. I_{o1} cannot be no-load with $V_{o2}<V_{i1}$, otherwise the inductor will be always charged. In a word, although the topologies in Table 1 (ii) (a) and Fig. 8(a) are favorable in terms of the average inductor current and semiconductor devices, they are not suitable for the

specific application due to the restricted working conditions. The undesired restriction is avoided in the topologies in Fig. 9(a), Table 1 (ii) (d) and Fig. 10(a). And I_L is equal to $I_{i1}+I_{o2}$ in all these three converters. Their differences mainly lie in the number of active semiconductor devices in different working stage. From Table 3, all working stages have two active semiconductor devices in the topologies Fig. 9(a) and Table 1 (ii) (d), while only one stage has two and the rest two stages have one in the topology Fig. 10(a). Therefore, thanks to the smaller number of active semiconductor devices in conduction and consequently lower conduction losses, the topology in Fig. 10(a) is chosen for the specific application.

Table 3. Comparison among available SI-SIDO topologies in Table 1 (ii) (a) and (d), Fig. 8(a), Fig. 9(a) and Fig. 10(a).

Topology	I_L	Working Condition	Semiconductor Devices	
			Total	Active
Table 1 (ii)(a)	I_{i1}	$I_{o1}>I_{o2}$	2S2D	1S+1D+1S1D
Fig. 8(a)	I_{i1}	I_{o1}/I_{o2} is restricted with $V_{o2}<V_{i1}$	2S2D	1S+1D+1S1D
Fig. 9(a)	$I_{i1}+I_{o2}$	—	2S2D	1S1D+1S1D+2D
Table 1 (ii)(d)	$I_{i1}+I_{o2}$	—	2S2D	2S+2D+1S1D+1S1D
Fig. 10(a)	$I_{i1}+I_{o2}$	—	2S2D	1S+1D+1S1D

*S: switch, D: diode

B. Operation Analysis

The proposed SI-SIDO topology in Fig. 10(a) is re-depicted in Fig. 11(a). It can operate in discontinuous conduction mode (DCM) as shown in Fig. 12(a), or continuous conduction mode (CCM) as illustrated in Fig. 12(b). v_{gs1} and v_{gs3} are the drive signals of S_1 and S_3, respectively. i_L, i_{s1}, i_{s3} and i_{Ds2} are the inductor current, drain-to-source currents of S_1, S_3 and current of D_{s2}, respectively. The corresponding equivalent circuits in different stages are shown in Fig. 11(b)~(e). It is noted that all components are assumed to be ideal to simplify the analysis.

(a) DCM Operation

According to Fig. 12(a), a switching period T_s is divided into two equal parts [t_0, t_3] and [t_3, t_6] in DCM. During the interval [t_0, t_3], switch S_3 is turned off and the power is transferred from input V_{i1} to output V_{o1}. Switch S_3 conducts during the interval [t_3, t_6], and then the power is transferred from input V_{i1} to output V_{o2}. The output voltages V_{o1} and V_{o2} are respectively controlled by the duty-cycle D_1 and D_2 of S_1 in each half switching period.

Stage 1 (t_0~t_1): Switches S_1 conduct while S_3 is turned off in this stage, as illustrated in Fig. 11(b). Inductor L is charged by V_{i1}, and thus the inductor current i_L increases. The drain-to-source current i_{s1} is equal to i_L. Two diodes D_{s2} and D_{s3} are both reverse biased, which are respectively clamped by V_{o1} and $V_{i1}+V_{o2}$.

Stage 2 (t_1~t_2): At t_1, switch S_1 is turned off, and then diode D_{s2} turns to be forward biased, as shown in Fig. 11(c). In this stage, inductor L is discharged by V_{i1}-V_{o1}, and thus the inductor current i_L decreases. The drain-to-source current i_{Ds2} is equal to i_L. Switches S_1 and S_3 are respectively clamped by V_{o1} and V_{o1}-V_{i1}-V_{o2}.

Stage 3 (t_2~t_3): At t_2, the inductor current i_L decays to zero. Then, all semiconductor devices are inactive in this stage, as illustrated in Fig. 11(d).

Stage 4 (t_3~t_4): At t_3, switches S_1 and S_3 are turned on. The operation in this stage is the same with that of stage 1.

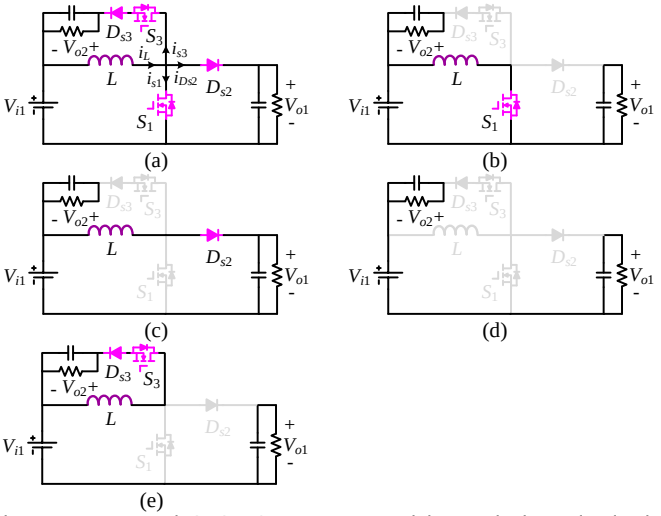


Fig. 11. Proposed SI-SIDO converter and its equivalent circuits in different working stages: (a) converter, (b) [t_0, t_1] in both DCM and CCM, [t_3, t_4] in DCM (c) [t_1, t_2] in both DCM and CCM, (d) [t_2, t_3], [t_5, t_6] in DCM and (e) [t_4, t_5] in DCM, [t_2, t_3] in CCM.

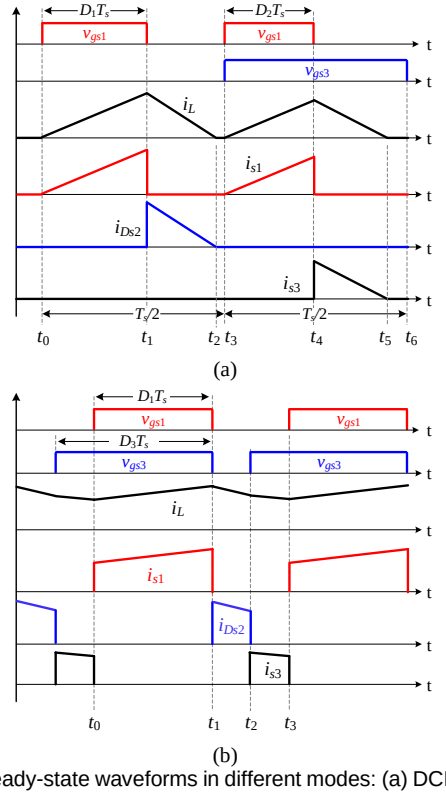


Fig. 12. Steady-state waveforms in different modes: (a) DCM and CCM.

Stage 5 (t_4~t_5): At t_4, switch S_1 is turned off. Because S_3 is on and $V_{o2}+V_{i1}$ is smaller than V_{o1}, the diode D_{s3} will turn to be forward biased and the inductor current i_L commutes to output V_{o2}, as shown in Fig. 11(e). In this stage, inductor L is discharged by -V_{o2}, and thus the inductor current i_L decreases. The diode D_{s2} and switch S_1 are respectively clamped by V_{o1}-V_{i1}-V_{o2} and $V_{i1}+V_{o2}$.

Stage 6 (t_5~t_6): At t_5, the inductor current i_L decays to zero, which is the same with that of stage 3.

From above, the proposed SI-SIDO converter in Fig. 11(a) operates as a typical boost and buck-boost converter in turn during different half switching period T_s/2. Then the voltage relationships among V_{o1}, V_{o2} and V_{i1} can be correspondingly

obtained in (1). From (1), by adjusting the duty-cycles D_1 and D_2, the output voltages V_{o1} and V_{o2} can be independently controlled. In addition, the power P_{o1} and P_{o2} of two outputs V_{o1} and V_{o2} are calculated in (2), which can also be respectively controlled by the duty-cycles D_1 and D_2.

$$\begin{cases} V_{o1} = (1+\sqrt{1+\dfrac{2D_1^2T_sR_1}{L}})\dfrac{V_{i1}}{2} \\ V_{o2} = \sqrt{\dfrac{R_2T_s}{2L}}D_2V_{i1} \end{cases} \quad (1)$$

$$\begin{cases} P_{o1} = \dfrac{V_{i1}^2V_{o1}T_s}{2L(V_{o1}-V_{i1})}D_1^2 \\ P_{o2} = \dfrac{V_{i1}^2T_s}{2L}D_2^2 \end{cases} \quad (2)$$

where R_1 and R_2 are the output resistances of V_{o1} and V_{o2}.

(b) CCM Operation

According to Fig. 12(b), a switching period T_s includes three stages [t_0, t_3] in CCM. The stages [t_0, t_1], [t_1, t_2] and [t_2, t_3] of CCM are respectively similar with the stages [t_0, t_1], [t_1, t_2] and [t_4, t_5] of DCM, except that the inductor current i_L is continuous instead of discontinuous. The inductor current flows to the first output V_{o1} during the stage [t_1, t_2] and flows to the second output V_{o2} during the stage [t_2, t_3]. Then, with the neglect of inductor current ripple, equation $I_L=V_{o1}/R_1/(1-D_3)=V_{o2}/R_2/(D_3-D_1)$ is derived. In addition, the inductor is charged by V_{i1} in the stage [t_0, t_1], and is discharged by V_{i1}-V_{o1} and -V_{o2} in the stage [t_1, t_2] and [t_2, t_3] respectively. Then, equation D_1V_{i1}= (1-D_3)(V_{o1}-V_{i1})+(D_3-D_1)V_{o2} can be obtained according to the flux balance of inductor. With the above two equations, the voltage relationship between V_{o1}, V_{o2} and V_{i1} is calculated in (3). From (3), both V_{o1} and V_{o2} are determined by D_1, D_3, R_1 and R_2. Therefore, severe cross regulation problem will be incurred under load variation. In order to improve the dynamic response, the existing proposed solutions such as control loop decouple [33, 34], multivariable control [35], predictive control [36-38] and deadbeat control [39] can be employed, but with increased complexity.

$$\begin{cases} V_{o1} = \dfrac{R_1(1-D_3)(1+D_1-D_3)}{R_1(1-D_3)^2+R_2(D_3-D_1)^2}V_{i1} \\ V_{o2} = \dfrac{R_2(D_3-D_1)(1+D_1-D_3)}{R_1(1-D_3)^2+R_2(D_3-D_1)^2}V_{i1} \end{cases} \quad (3)$$

IV. Design and Experiment Verification

In order to verify the theoretical analysis, a prototype circuit of proposed SI-SIDO converter in Fig. 11(a) with system parameters in Table 4 is built. In this section, its design considerations in both DCM and CCM are explained firstly. Then, the simulation and experiment results under input voltages V_{i1}=18 and 30V, are demonstrated.

A. Design Considerations

In DCM, the peak inductor current $i_L(t_1)$ and $i_L(t_4)$ are obtained in (4) from the performance analysis in above section. Then, according to the average output current $I_{o1}=i_L(t_1)\times(t_2-t_1)/2$ and $I_{o2}=i_L(t_2)\times(t_5-t_4)/2$, the values of t_2-t_0 and t_5-t_3 are calculated in (5), and they should be less than $T_s/2$. Based on this requirement, the available inductance L is calculated in (6) and is depicted in Fig. 13(a) with the aforementioned system parameters. The available inductance varies with different input voltage V_{i1}, for example, $L\leq$74μH for V_{i1}=30V while $L\leq$37μH for V_{i1}=18V. Because the DCM operation is demanded to be guaranteed under whole input voltage range, the smallest range of inductance L should be selected, i.e. $L\leq$37μH. Besides, with the consideration of margin and non-ideal parameters in the practical circuit, the inductance L is finally designed as 30μH. Then, the duty-cycles D_1 and D_2 are derived in (7) from (1) and are also demonstrated in Fig. 13(b). They decrease with the increment of input voltage V_{i1}. Afterwards, substituting (7) into (4), the peak inductor current $i_L(t_1)$ and $i_L(t_4)$ as a function of V_{i1} are illustrated in Fig. 13(c), which respectively obtain maximum value 7.48A and 5.66A at V_{i1}=18V. Moreover, according to Fig. 12, the root-mean-square (RMS) value of inductor current I_{L_rms} and drain-to-source current I_{s1_rms}, I_{s3_rms} are obtained in (8). Their maximum values 3.57A, 2.89A and 1.37A are also obtained at V_{i1}=18V, as shown in Fig. 13 (c) and (d). And from Fig. 11(a), the average current I_{DS2}~I_{DS3} of D_{s2}~D_{s3} are equal to the average currents I_{o1} and I_{o2}, respectively. On the other hand, the maximum drain-to-source voltages of S_1 and D_{s2} are V_{o1}, and the voltage stresses of S_3 and D_{s3} are V_{o1}-V_{i1}-V_{o2} and V_{i1}+V_{o2}, respectively. Based on above analysis, a ferrite core EI-28 with 12 turns are employed to implement the inductor L, mosfet IPP530N15N3 is chosen as switches S_1 and S_3, and MBR20200CT is employed as diode D_{s2} and D_{s3} in the prototype circuit.

Table 4. Parameter Specifications

Parameter	Value	Parameter	Value
Input Voltage V_{i1}	18~30V	Inductance L_1	30μH/DCM 1.4mH/CCM
Output Voltage V_{o1}	60V		
Rated Output Current I_{o1_full}	0.5A	Switches $S_{1,3}$	IPP530N15N3
Output Voltage V_{o2}	24V	Diodes $D_{s2,2}$	MBR20200CT
Rated Output Current I_{o2_full}	0.5A	Switching Period T_s	40μs

$$\begin{cases} i_L(t_1) = \dfrac{V_{i1}}{L}D_1T_s = \dfrac{V_{o1}-V_{i1}}{L}(t_2-t_1) \\ i_L(t_4) = \dfrac{V_{i1}}{L}D_2T_s = \dfrac{V_{o2}}{L}(t_5-t_4) \end{cases} \quad (4)$$

$$\begin{cases} t_2-t_0 = \dfrac{V_{o1}}{V_{i1}}\sqrt{\dfrac{2LI_{o1}T_s}{V_{o1}-V_{i1}}} < \dfrac{T_s}{2} \\ t_5-t_3 = \dfrac{V_{i1}+V_{o2}}{V_{i1}}\sqrt{\dfrac{2LI_{o2}T_s}{V_{o2}}} < \dfrac{T_s}{2} \end{cases} \quad (5)$$

$$L \leq \min\left(\frac{V_{i1}^2(V_{o1}-V_{i1})T_s}{8V_{o1}^2I_{o1}}, \frac{V_{i1}^2V_{o2}T_s}{8(V_{i1}+V_{o2})^2I_{o2}}\right) \quad (6)$$

$$D_1 = \sqrt{\frac{((2V_{o1}/V_{i1}-1)^2-1)L}{2T_sR_1}}, \quad D_2 = \frac{V_{o2}}{V_{i1}}\sqrt{\frac{2L}{R_2T_s}} \quad (7)$$

$$\begin{cases} I_{L\_rms} = \sqrt{\dfrac{t_2 - t_0}{3T_s} i_L(t_1)^2 + \dfrac{t_5 - t_3}{3T_s} i_L(t_4)^2} \\ I_{s1\_rms} = \sqrt{\dfrac{D_1}{3} i_L(t_1)^2 + \dfrac{D_2}{3} i_L(t_4)^2}, I_{s3\_rms} = \sqrt{\dfrac{t_5 - t_4}{3T_s}} i_L(t_4) \end{cases} \quad (8)$$

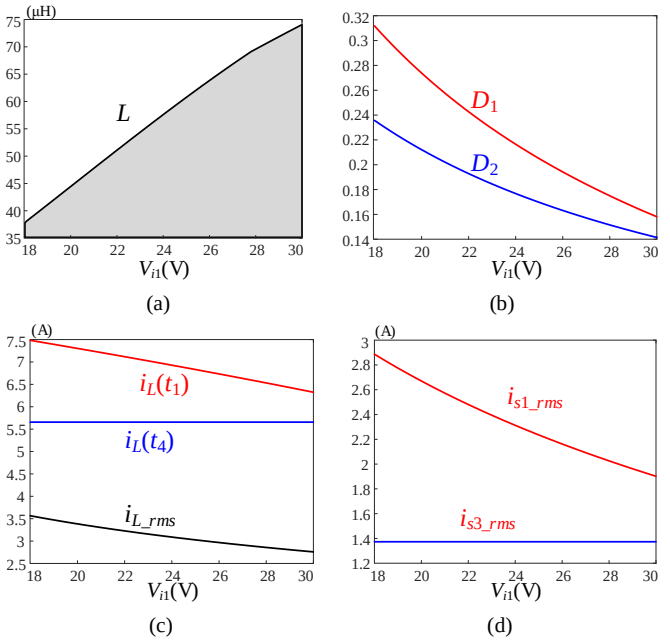


Fig. 13. Design considerations in DCM: (a) inductance L, (b) duty-cycles D_1, D_2, (c) $i_L(t_1)$, $i_L(t_4)$, i_{L_rms} and (d) I_{s1_rms}, I_{s3_rms}.

In CCM, the required inductance is different from that in DCM, whose value is designed to ensure the ripple current Δi_L of inductor in (9) is less than 20% of its average value I_L. Similarly, according to the system parameters in Table 4, the inductance is designed as 1.42mH. In addition, the voltage stresses of semiconductor devices are the same with that in DCM, while their current stresses are decreased due to the smaller ripple current. Hence, the mosfet IPP530N15N3 and diode MBR20200CT are still used.

$$\begin{cases} \Delta i_L = \dfrac{V_{i1}}{L} D_1 T_s \\ I_L = I_{i1} + I_{o2} = \dfrac{V_{o1} I_{o1} + V_{o2} I_{o2} + V_{i1} I_{o2}}{V_{i1}} \end{cases} \quad (9)$$

B. Simulation and Experiment Results

Experiment waveforms of the proposed converter in Fig. 11(a) working in DCM are illustrated in Fig. 14~Fig. 16, which are in well coincidence with the aforementioned theoretical analysis. From Fig. 14, by adjusting the duty-cycles D_1 and D_2 of drive signal v_{gs1} of switch S_1, the output voltages v_{o1} and v_{o2} are kept constant under different input voltage v_{i1}. And with the increase of v_{i1}, both D_1 and D_2 decrease which effectively verifies the analysis in Fig. 13(b). Besides, from Fig. 15, $i_L(t_1)$ is a little decreased and $i_L(t_4)$ is almost unchanged with the increase of v_{i1}. It also validates the correctness of Fig. 13(c). In addition, according to Fig. 16, the steady voltage stress v_{s1} and v_{Ds2} of S_1 and D_{s2} are always equal to V_{o1}, irrespective of the variation of the input voltage. On the other hand, the voltage stresses v_{s3} and v_{Ds3} of S_3 and D_{s3} are V_{o1}-V_{i1}-V_{o2} and V_{i1}+V_{o2}, which are respectively decreased and increased with the increase of v_{i1}. It is noteworthy that the oscillation of v_{s1}, v_{Ds2}, v_{s3} and v_{Ds3} during the interval when i_L=0, is caused by the resonance of the inductor L and the parasitic capacitors of semiconductor devices.

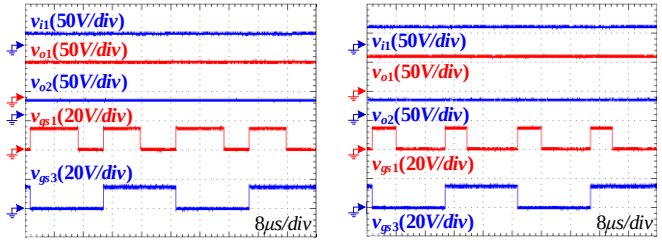


Fig. 14. Experimental waveforms of input voltage v_{i1}, output voltages v_{o1}~v_{o2}, drive signals v_{gs1}, v_{gs3} at different v_{i1} in DCM: (a) v_{i1}=18V and (b) v_{i1}=30V.

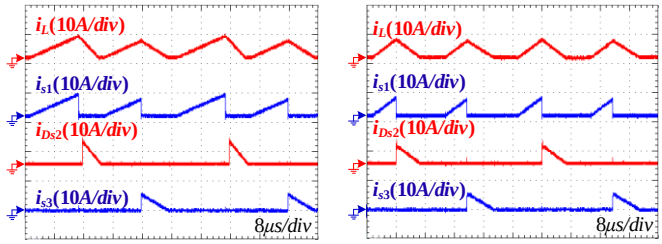


Fig. 15. Experimental waveforms of inductor current i_L, drain-to-source currents i_{s1}, i_{s3}, and diode current i_{Ds2} at different v_{i1} in DCM: (a) v_{i1}=18V and (b) v_{i1}=30V.

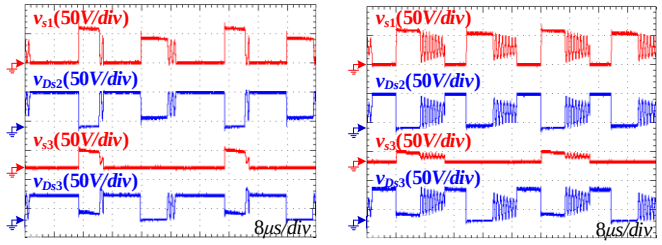


Fig. 16. Experimental waveforms of drain-to-source voltages v_{s1}, v_{s3}, and diode voltages v_{Ds2}, v_{Ds3} at different v_{i1} in DCM: (a) v_{i1}=18V and (b) v_{i1}=30V.

Fig. 17 also depicts the measured efficiencies of proposed converter at different input voltage v_{i1}. Because there are two conducting switches/diodes in only one stage while one switch/diode conducts in the rest two stages, the number of active semiconductor devices in the proposed converter is small. Therefore, low conduction losses are achieved, contributing to high efficiencies. In Fig. 17, the minimum efficiency is 0.919 and the maximum efficiency is 0.98. It is noteworthy that the practical efficiencies would be a little decreased with the consideration of the loss of drive circuits.

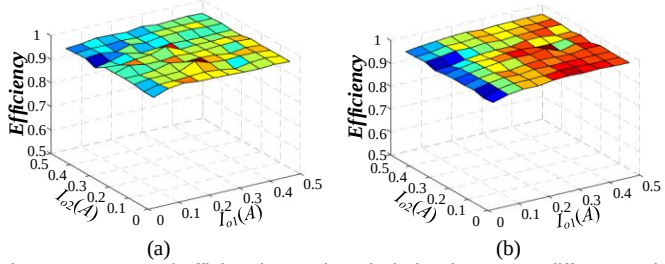


Fig. 17. Measured efficiencies under whole load range at different v_{i1} in DCM: (a) v_{i1}=19V and (b) v_{i1}=30V.

Likewise, experiment waveforms of the proposed converter in Fig. 11(a) working in CCM are also illustrated in Fig. 18~Fig. 20, which are in well coincidence with the theoretical analysis. Unlike the discontinuous currents in DCM, the inductor current is continuous in CCM. Hence, the oscillation of v_{s1}, v_{Ds2}, v_{s3} and v_{Ds3} won't appear, as shown in Fig. 20. However, because of the hard-switching operation of switches and the reverse-recovery process of diodes, spike turn off/on voltage and currents are incurred in Fig. 19~Fig. 20.

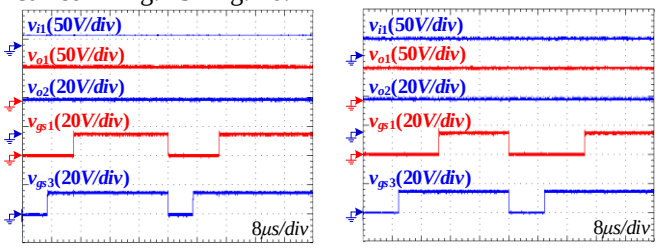


Fig. 18. Experimental waveforms of input voltage v_{i1}, output voltages v_{o1}~v_{o2}, drive signals v_{gs1}, v_{gs3} at different v_{i1} in CCM: (a) v_{i1}=18V and (b) v_{i1}=30V.

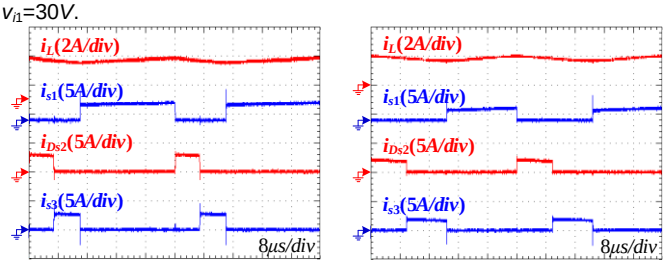


Fig. 19. Experimental waveforms of inductor current i_L, drain-to-source currents i_{s1}, i_{s3}, and diode current i_{Ds2} at different v_{i1} in CCM: (a) v_{i1}=18V and (b) v_{i1}=30V.

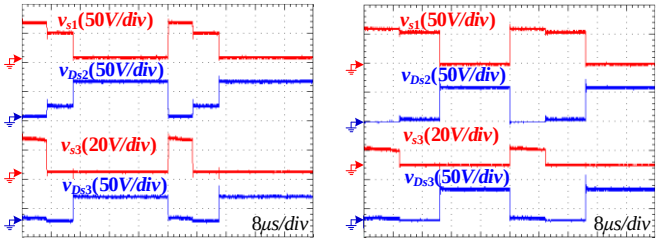


Fig. 20. Experimental waveforms of drain-to-source voltages v_{s1}, v_{s3}, and diode voltages v_{Ds2}, v_{Ds3} at different v_{i1} in CCM: (a) v_{i1}=18V and (b) v_{i1}=30V.

Besides, the dynamic response under load variation in DCM and CCM are shown in Fig. 21(a) and (b), respectively. In DCM, the two outputs are independently controlled and thus the variation of i_{o1}/i_{o2} only has an influence on v_{o1}/v_{o2}. Also, the simulation results of dynamic response under input voltage variation in DCM is also shown in Fig. 22, which is similar as two separate buck-boost and boost converters. On the other hand, severe cross regulation problem exists in CCM that both v_{o1} and v_{o2} will be influenced with the change of either i_{o1} or i_{o2}. Hence, improved control strategies are urgently demanded to improve the dynamic performance in CCM. Finally, the photo of the prototype circuit in DCM is also given in Fig. 23. In CCM, only the inductor L is different and thus its photo is not illustrated again.

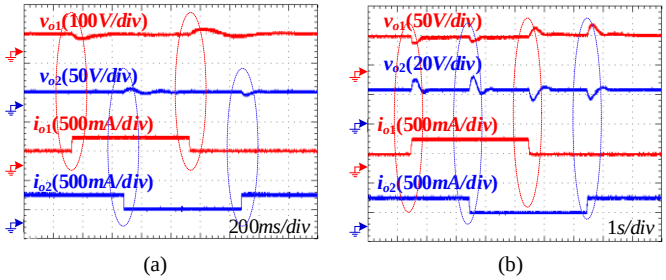


Fig. 21. Experimental waveforms of dynamic response under load variation: (a) DCM and (b) CCM.

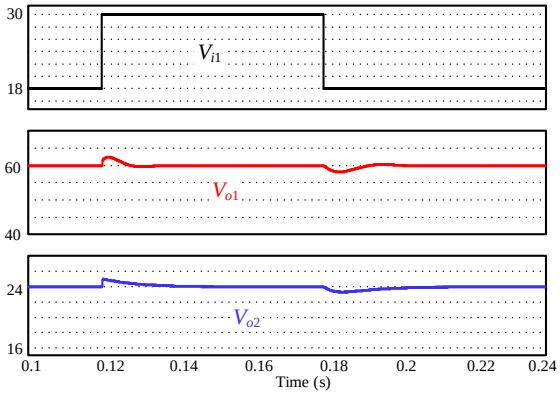


Fig. 22. Simulation waveforms of dynamic response under input voltage variation in DCM.

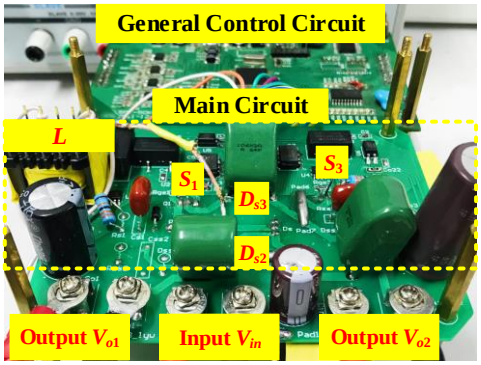


Fig. 23. Photograph of prototype SI-SIDO converter in Fig. 11(a).

V. Conclusion

In this paper, a simple principle of deriving SI-MIMO topologies from typical buck, boost, buck-boost and non-inverting buck-boost converters with only three steps is revealed. And as an example, a family of SI-SIDO, SI-DISO and SI-DIDO topologies are derived and demonstrated in detail. With the proposed principle and the obtained SI-MIMO topologies, more choices are available and then an optimum one can be selected out for an engineering application. In addition, a family of SI-SIDO boost converters are also taken as an example to be compared under input voltages V_{i1}=18~30V, output voltages V_{o1}=60V and V_{o2}=24V, and a preferred one with lower conduction losses is finally selected, analyzed and validated experimentally.

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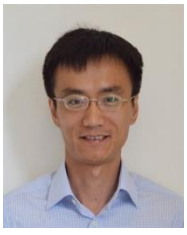

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