Toward Temperature Tracking With Unipolar Metal-Oxide Thin-Film SAR C-2C ADC on Plastic

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***Abstract*— The maturity of metal–oxide thin-film transistors (TFT) highlights opportunities to develop robust and low-cost electronics on flexible and stretchable substrates over large area in an industry-compatible technology. Internet-of-Everything applications with sensor nodes are driving the development of analog-to-digital converters (ADCs). In this paper, a self-biased and self-digital-controlled successive approximation ADC with integrated references and sensor read-in circuitry together with a printed negative temperature coefficient (NTC) sensor using unipolar dual-gate metal–oxide (InGaZnO) TFTs is demonstrated. The system is operated at a clock of up to 400 Hz and a total power dissipation of 245 mW (73 μW from analog) at a maximum power supply of 30 V is measured. The radio-frequency identification-ready ADC comprises of a total of 1394 indium–gallium–zinc oxide TFTs and 31 metal–insulator–metal capacitors. A figure of merit of 26 nJ/c.s. is achieved from the ADC driven from external microcontroller. The robustness of the various blocks of the chip is characterized and the yield is discussed.**

***Index Terms*— Analog-to-digital converter (ADC), C2C, digital control, flex, indium–gallium–zinc oxide (IGZO), Internet of Everything, Internet of Things (IoT), polyimide (PI), pseudo-CMOS, radio-frequency identification (RFID), sensor, successive approximation (SAR), tag, temperature.**

I. Introduction

RADIO-frequency identification (RFID) tags are offering branding, security control, and fast-tracking features to the end users. RFIDs can propagate these benefits if attached to cash, health patches, bank cards, delivery boxes, and other valuable items. Metal–oxide thin-film technology, as low cost, flexible, very thin, and large area compatible, can widen the range of RFID applications [1]–[6]. Due to the maturity of the process, indium–gallium–zinc oxide (IGZO) thin-film transistors (TFTs) are becoming mainstream technology for the flat panel display (FPD) industry [7]. The increasing stability of the TFT technology initiates the expansion of the technology to other applications, such as sensor applications for environment sensitive products or medical prevention and diagnosis [8]. Moreover, Internet-of-Everything evolution demands sensor-ready RFID tags, preferable by monolithic integration of humidity, pressure, or temperature sensors on IC. The revolution of smart environment-aware tags needs analog-to-digital converters (ADCs) on flexible substrates to not only be surface-shape independent but also low-cost in order to be suitable for short lifetime and nonreusable everyday applications (see Fig. 1).

For RFID applications, poly-silicon TFTs have high cost, are nonuniform over large area, and have high leakage [9], [10]. Organic TFT is not yet fully industry mature and with small performance [11]–[15]. Amorphous silicon TFT, despite being the mainstream FPD technology are very slow and lack stability [13]. On the other hand, dual-gate (DG) etch-stop-layer (ESL) IGZO TFTs have fair stability, extremely low leakage currents [16], low fabrication cost, and fair uniformity at room temperature fabrication [17], [18] and are compatible with flexible substrate. Recently, an asynchronous delta–sigma modulator on foil was presented [19], generating pulsewidth modulated (PWM) signal at mW-range power dissipation. In this paper, we propose a six-pin RFID-ready self-biased successive approximation (SAR) C-2C ADC with integrated digital control, references, and sensor readin using DG IGZO TFTs on a very thin flexible substrate and demonstrate it with a printed sensor as well.

II. Metal Oxide Technology

A. Fabrication Process

A DG top-contact TFT with an ESL was fabricated on 32 cm $\times$ 35 cm (first generation) Toyobo 40-μm thick polyimide (PI) substrates [17], [18]. A molybdenum–chromium (MoCr) metal was deposited using sputtering for gate metal and first interconnect layer. A 200-nm-thick plasma-enhanced chemical vapor deposited (PECVD) SiO_2 gate dielectric layer was deposited at 250 °C followed by the deposition of the 12-nm-thick IGZO layer using dc sputtering.

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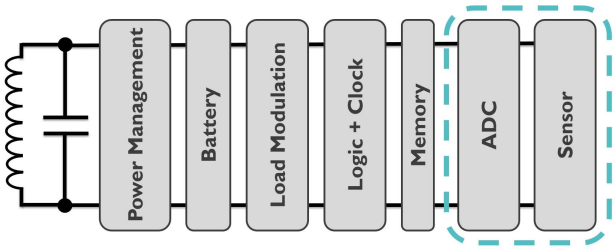

Fig. 1. High-level environment-aware RFID system blocks with investigated ADC and temperature sensor blocks.

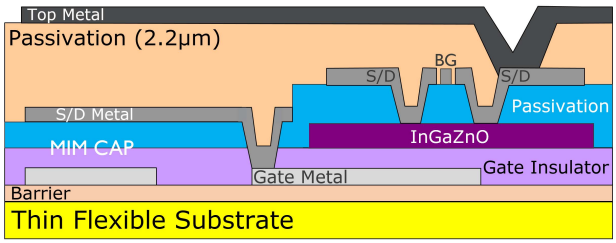

Fig. 2. ESL DG IGZO TFT and capacitor cross section. The second gate (BG) of the TFT and the location of the MIM capacitor are indicated.

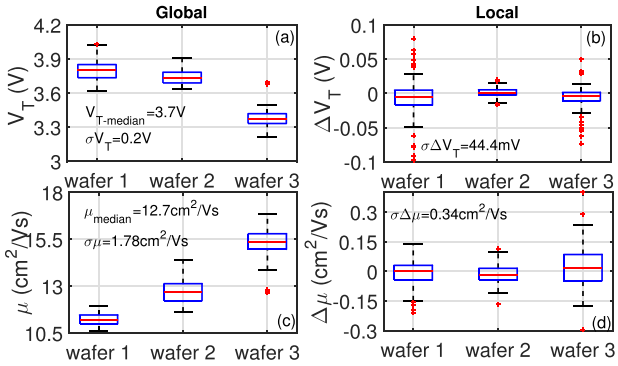

Fig. 3. Extracted (a) and (c) global and (b) and (d) local offset V_T and mobility spreads (228 samples per wafer) of $W/L = 500\ \mu$m/30 μm of measured TFTs over three wafers (840 cm^2) and wafer-to-wafer median and standard deviation (σ) extracted values.

A 100-nm-thick SiO_2 layer was grown using PECVD on the top of the patterned semiconductor. A MoCr layer was sputtered for source–drain contact metals (SD metal) and second interconnect metal layer. The TFT stack was encapsulated with a 2.2-μm-thick photopatternable SU8 layer. The third 100-nm-thick MoCr metal layer (Top metal) was deposited on top and patterned. A schematic cross section of the ESL TFT layout together and a metal–insulator–metal (MIM) capacitor are shown in Fig. 2. The second gate (BG) is located between the source and drain contact, routed in the same metal layer as source drain.

B. Technology Mismatch

In Fig. 3(a) and (c), the global wafer-2-wafer median threshold voltage $V_T = 3.7$ V ($\sigma V_{T-W2W} = 0.2$ V) and median charge-carrier mobility $\mu = 12.7$ cm^2/Vs ($\sigma\mu = 1.78$ cm^2/Vs) over three wafers (840-cm^2 total area) are shown. Focusing on wafer level, standard deviations of the

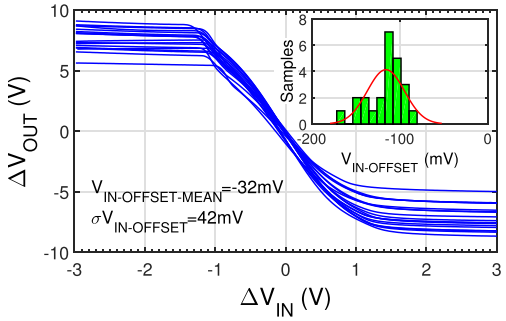

Fig. 4. Measured voltage transfer curves of 24 samples of DG diode-load DAs [see Fig. 10(b)] and the extracted input voltage offset ($V_{\text{IN-OFFSET}}$) distribution over 280 cm^2.

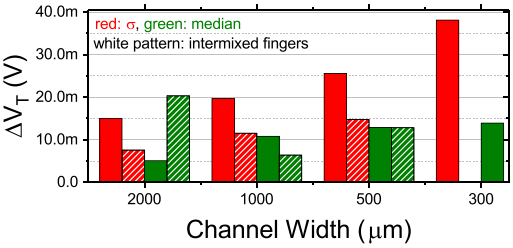

Fig. 5. Median and standard distribution (σ) of the extracted threshold voltage of various channel widths ($W = 2$, 1, 0.5, and 0.3 mm) of measured normal finger and interdigitated DG IGZO TFTs over 280 cm^2.

V_T drops to $\sigma V_{\text{T-WAFER}} = 63$ mV and corners of the median of the V_T are 3.21 and 3.63 V. Moreover, in Fig. 3(b) and (d), the threshold voltage (ΔV_T) and mobility offset ($\Delta\mu$) spread of neighboring IGZO TFTs over three wafers are shown. A wafer-2-wafer $\sigma|\Delta V_T| = 44.4$ mV [Fig. 3(b)] and $\sigma|\Delta\mu| = 0.34$ cm^2/Vs [Fig. 3(d)] for neighboring DG IGZO TFTs of $W/L = 500\ \mu$m/30 μm is monitored. Again on a wafer level, standard deviations of ΔV_T drop to 19 mV.

The aforementioned local variability is translated to an input offset of median value of $V_{\text{OFFSET}} = -32$ mV ($\sigma V_{\text{OFFSET}} = 42$ mV) (see Fig. 4), for a diode-load differential amplifier (DA) [see Fig. 10(b)] at a power supply of $V_{\text{dd}} = 15$ V. The transfer curves in Fig. 4 are from 24 samples over 280-cm^2 area. In the inset of Fig. 4, the distribution of the extracted input offset of the DAs is shown. The input offset is a limiting factor for ADC resolution and has to be compensated for when a practical ADC is aimed.

In Fig. 5, the offset between two neighboring TFTs for various channel widths (W) for normal interdigitated and intermixed fingers of two TFTs is shown. Parameters, such as the median and standard deviation of the absolute of the difference of threshold voltage ($|\Delta V_T|_{\text{median}}$ and $\sigma|\Delta V_T|$) of 119 pairs of neighboring TFTs ($W = 2000$, 1000, 500, and 300 μm and $L = 30\ \mu$m), are plotted, suggesting the Pelgrom law for both normal and intermixed finger configuration. The intermixed TFTs have better or equally good uniformity figures than the normal finger configuration. In addition, $A_{|\Delta V_T|}$ is calculated as 3.48 Vμm for normal and 1.74 Vμm for intermixed, suggesting a stronger WL dependence of the $|\Delta V_T|$ of normal paired TFTs than intermixed. Intermixed finger configuration is used for IGZO TFT DAs on flexible substrate to improve matching.

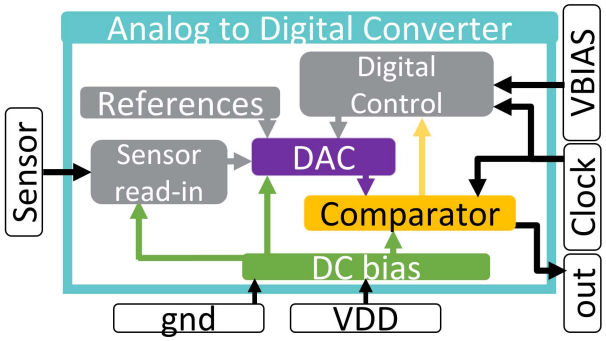

Fig. 6. Implemented ADC block diagram with external pins needed.

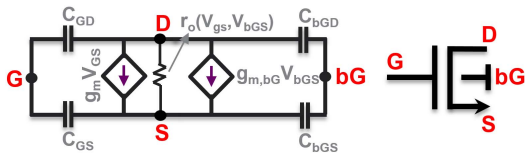

Fig. 7. Proposed π-small-signal model schematic and the schematic symbol for DG IGZO TFTs.

III. Details on Blocks Design

The selected ADC architecture for an RFID-ready sensor system on plastic foil is an SAR ADC. SAR systems have lower power dissipation compared to other architectures, good resolution and accuracy, and a relative small form factor in their C-2C implementation. The low power dissipation of SAR ADC systems is a major advantage when a unipolar technology is used and a mobile RF-powered application is targeted. Moreover, the metal–oxide technology offers excellent MIM capacitor uniformity, which is a basic device of the C-2C SAR architecture (see Fig. 6).

In Fig. 6, a high-level block diagram of the implemented C-2C SAR ADC is shown. The ADC comprises of six main blocks: the digital-to-analog converter (DAC) networks, a comparator with offset cancellation, a dc bias circuitry, a digital control circuit (DCC), the read-in circuitry of the sensor, and the reference resistors. All blocks are integrated on a 40-μm-thick PI foil (see Fig. 19). The six required external pins are illustrated as well. In Sections III-A–III-D, all the blocks are described, explaining in parallel the decisions that are made toward an RFID-ready robust temperature-tracking system on plastic foil.

A. Analog Blocks

The analog blocks of the designed ADC are a comparator, inverters and buffers, dc bias circuitry, and Dickson's charge pump. In the following, before the various blocks are analyzed, the used DG small-signal model is briefly described and supported with measurement results.

1) Dual-Gate Small-Signal Model: In Fig. 7, a DG small-signal model is proposed to theoretically analyze the analog designs. The model is also verified against the experimental results. The small-signal model consists of two dependent sources for the two gates, and the corresponding coupling capacitors from the two gate nodes to source and drain nodes. Moreover, the output resistance r_o is depended both to gate voltage (V_{GS}) and to the BG voltage (V_{bGS}), respectively. The width of the BG improves the output resistance, as shown in Fig. 8, from measurements of TFTs with various widths of the BG ($W_{BG} = 0$ to 35 μm), where $W_{BG} = 0$ means that no BG is present.

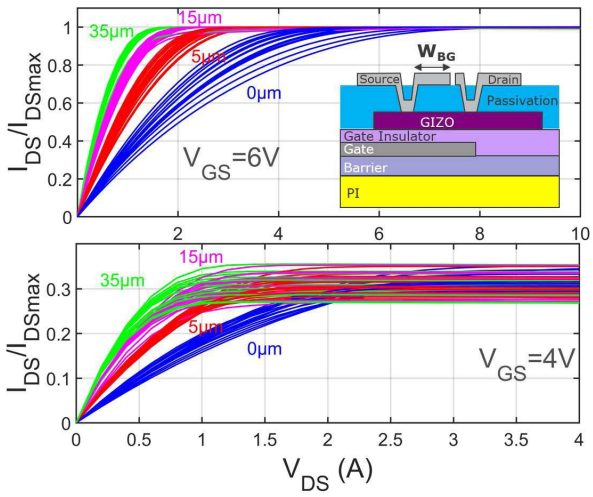

Fig. 8. Measured normalized output curves of $W/L = 50$ μm/50 μm IGZO TFT, where the back gate is connected to source for various back gate widths ($W_{BG} = 0$, 5, 15, and 35 μm) and for $V_{GS} = 4$ and 6 V. 18 samples are plotted for each size from three wafers (840 cm^2).

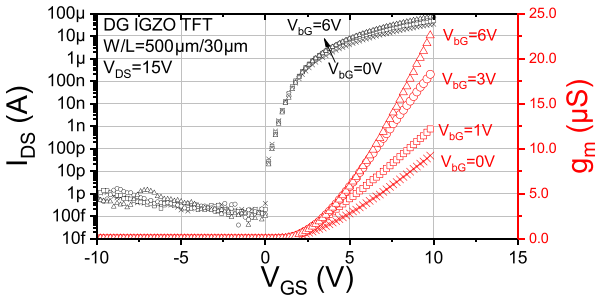

Fig. 9. Measured drain current and the corresponding calculated total transconductance g_mT of the DG IGZO TFT of $W/L = 500$ μm/30 μm for various back gate voltages $V_{BG} = 0$, 1, 3, and 6 V and $V_{DS} = 15$ V.

The BG transcondactance $g_{m,BG}$ is given $g_{m,bG} = \eta \cdot g_m$. The effect of the amplification factor η can be seen in Fig. 9 [21], where I_{DS} of a DG IGZO TFT of $W/L = 500$ μm/30 μm and the corresponding total transconductance $g_{mT} = g_m + g_{m,BG}$ is plotted when the BG is biased for various voltages from $V_{BG} = 0$ V to up to 6 V.

2) Differential Amplifiers: The basic block of the comparator is the DA. In order to increase the yield of the design, various DA topologies are investigated to identify the most robust topology. The BG of the TFT is used accordingly to improve the performance and the yield of the designs. Diode-connected load is used due to the lack of complementary-type TFT. Zero-V_{GS} (or gate–source shorted) load is not investigated due to the <pA-range drain current at $V_{GS} = 0$ V (limited by measurement setup) of DG-ESL technology, as shown in Fig. 9. In addition, feedback is used to improve the

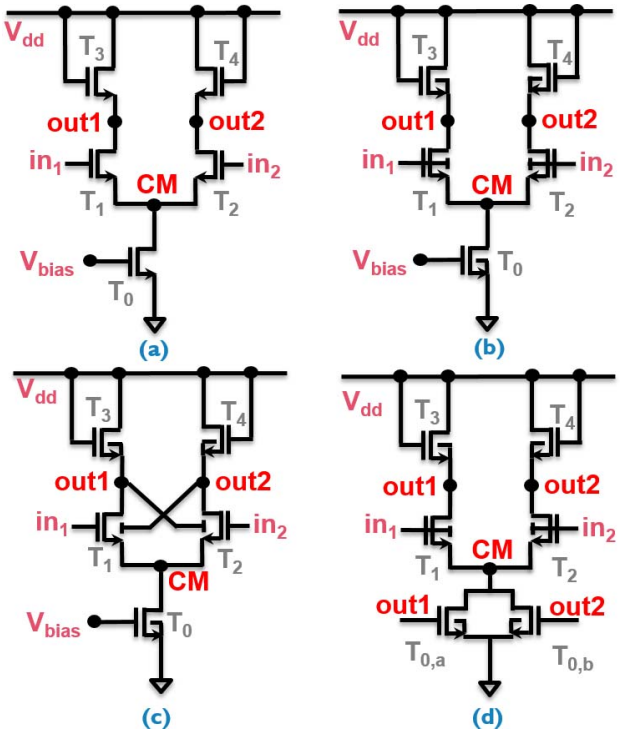

Fig. 10. Circuit schematics of (a) single-gate diode load (SGDL), (b) DG diode load (DGDL), (c) ISFB, and (d) LCMF DAs.

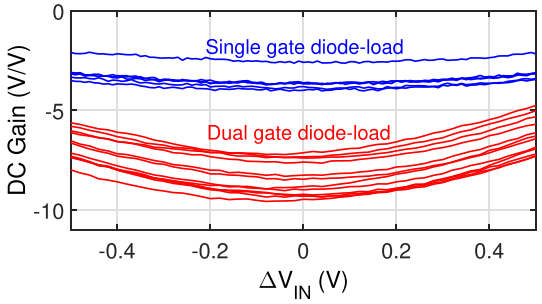

Fig. 11. Measured dc gain mapping of DGDL and SGDL DA for differential input $\Delta V_{\rm IN}$ over 280 cm^2.

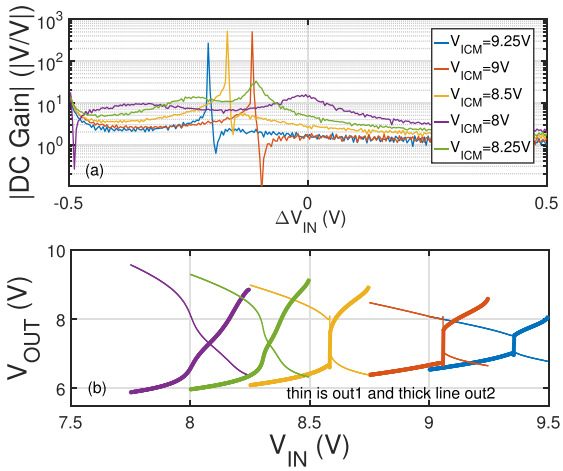

Fig. 12. Measured (a) dc gain of in-stage BG feedback DA for various common-mode input range $V_{\rm ICM}$ of input TFTs and (b) corresponding dc output responses out1 and out2 for differential input signals $\rm in_1$ and $\rm in_2$.

specifications of the DAs. Increasing the gain of a single stage can reduce the number of stages of the comparator, namely, the complexity, area, and yield of the overall design. Other parameters that are considered are the input offset, the input common-mode range ($V_{\rm ICM}$), and the 3-db bandwidth of the designs (BW).

In Fig. 10, four DA topologies are shown: (a) single-gate diode-connected load (SGDL), (b) DG diode-connected load (DGDL), (c) in-stage back gate positive feedback (ISFB), and (d) linear common-mode feedback topology (LCMF). The SGDL topology is used as initial reference. A small-signal analysis, assuming large output resistance, gives for DGDL DA [see Fig. 10(b)] gain: $A_{\rm DGDL} = (g_{m,2} + g_{m,\rm bG2})/g_{m,4}$, whereas for SGDL [see Fig. 10(a)]: $A_{\rm SGDL} = g_{m,2}/g_{m,4}$.

In the DGDL topology, the BG of the current-source TFT T_0 and the load TFTs $T_{3,4}$ are connected to the source to increase the output resistance, as shown in Fig. 8. Moreover, the BG of the input TFTs $T_{1,2}$ are connected to the gates to increase $g_{\rm mT}$, as shwon in Fig. 9. In Fig. 11, the measured dc gain of 12 samples of DGDL DA and six samples of SGDL over 280 cm^2 are shown. The median value of measured dc gain of the DGDL DA is 8.72 V/V and for SGDL 3.7 V/V. The spread of the measured gain is marginally better for the SGDL where the standard deviation of the measured gain is 0.5 V/V (15% of actual gain) compared to 0.88 V/V (10% of actual gain) for DGDL. The measured input common-mode range of the DGDL DA is $V_{\rm ICM} = 6$ V for $V_{\rm dd} = 15$ V. The measured power supply rejection ratio (PSRR) of the DGDL DA is $\rm PSRR_{dgdl} = 47$ dB and the common-mode rejection ratio (CMRR) of the DGDL DA is 60 dB for $V_{\rm dd} = 15$ V. PSRR is measured at $V_{\rm dd} = 10$ V and at 15 V. The DGDL DA offers good robustness statistics and decent performance numbers.

In Fig. 10(c), the in-stage BG feedback (ISFB) DA is shown. The BG of input TFTs is cross connected to the output nodes of the DA providing positive feedback. The gain of this topology is given by $A_{\rm ISFB} = g_{m,2}/(g_{m,4} - g_{m,\rm bG2})$. In Fig. 12, (a) the absolute of the measured dc gain and (b) the measured output voltage response of the two outputs of the DA are shown for various common-mode input ($V_{\rm ICM}$) voltages. The gain of the DA is dropping dramatically when $V_{\rm ICM}$ of the input transistors is under 8.25 V and decreases slowly over 9.25 V. Therefore, the common-mode input range is very limited (<1 V) for this topology. The common-mode input range can be increased by design in expense of the dc gain.

Finally, driving the current-source TFTs, $T_{0,a}$ and $T_{0,b}$, from the outputs of the DA [see Fig. 10(d)], i.e., a LCMF, gives an increased gain compared to DGDL but not for $V_{\rm ICM} = V_{\rm dd}/2$. In Fig.13, (a) the measured gain of six LCMF samples and (b) the voltage response of the two outputs of the DA for various $V_{\rm ICM}$ are shown. The median of the dc gain is 11.9 V/V and the standard deviation 0.62 V/V. The input offset of LCMF topology is higher than DGDL and SGDL, where the median of the input offset is $V_{\rm OFST} = 51$ mV and $\sigma V_{\rm OFST} = 26$ mV. The $V_{\rm ICM}$ of LCMF [see Fig. 13(b)] is smaller than DGDL

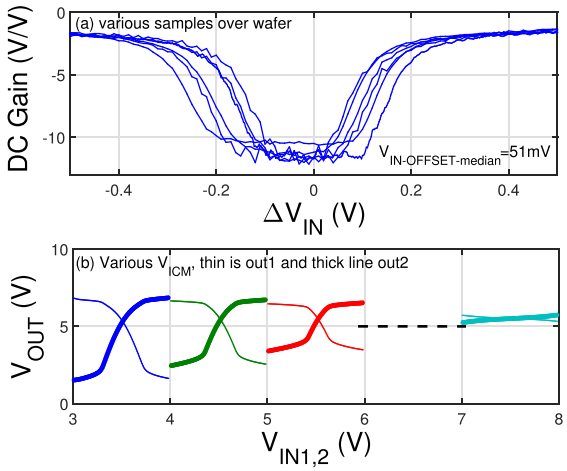

Fig. 13. Measured (a) dc gain and offset mapping of LCMF DA topology for differential input $\Delta V_{\rm IN}$ over 280-cm^2 area and (B) measurements of common-mode inputs ($V_{\rm ICM}$ = 3.5, 4.5, 5.5, and 7.5 V) of the LCMF DA.

TABLE I

SIZES OF TFT OF FOUR DA TOPOLOGIES TESTED EXPERIMENTALLY

design	T_0	$T_{1,2}$	$T_{3,4}$
SGDL	400/30	2000/30	20/40
DGDL	400/30	2000/30	20/100
ISFB	400/30	2000/30	20/30
LCMF	2*130/30	2000/30	20/100
channel Width/Length, in µm			

and the differential input range ($\Delta V_{\rm IN}$) is also narrower than the diode load topology, as shown in Fig. 13(a) compared to Fig. 11. For $\Delta V_{\rm IN} > 0.2$, the gain reduces down to ~2 V/V. In Fig. 13(b), the reduction of the gain of the LCMF topology is illustrated for larger $V_{\rm ICM}$. Notice that the dc bias on the gate of the input transistors, T1 and T2, has to be lower than $V_{\rm dd}/2$ to bias, $T_{0,a}$ and $T_{0,b}$, in linear regime.

All DG topologies are giving promising experimental results in different specifications and, thus, are being investigated experimentally in comparator's topology, to evaluate their yield and robustness, in Section III. DGDL topology has best yield and offset performance, the LCMF needs less bias nodes, and the back gate feedback topology (ISFB) has promising gain performance. The channel widths over lengths (W/L) for the experimental results of all topologies presented in this section are given in Table I.

3) Comparator: In this section, various comparators are formed by cascading three stages of DG DAs topologies from Section II. The main target is to achieve a robust differential dc gain above 60 dB. Wide common-mode input range will broaden applications spectrum and increase the resolution of the ADC. High PSRR is targeted due to expected ringing from rectified RFID-harvested power. In addition, high CMRR will improve immunity to noise interference. Speed is not a main concern since the main application of the developed ADC is a temperature sensor system. Besides the selected DA topologies, another variant, applying feedback to the input TFTs of each stage from the next stage feed back (NSFB), is introduced and evaluated.

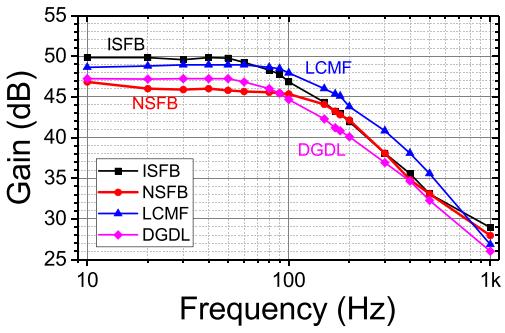

Fig. 14. Measured Bode gain plot for four comparator topologies for a load of 25 pF. The plotted NSFB result is for a comparator, where the second and third stage have $W_{1,2}$ four times smaller than the $W_{1,2}$ of first stage.

TABLE II

MEASURED PERFORMANCE COMPARISON TABLE OF THE VARIOUS COMPARATORS TOPOLOGIES

design	Gain (dB)	PSSR (dB)	CMRR (dB)	V_{ICM} (V)	BW (Hz)
NSFB*	46.5	80	69	2.5-6.5	110
ISFB	50	53	44	1.5-9.5	100
DGDL	47.2	60.2	48	2.5-8.5	120
DGDL**	-	90	81	2.5-8.5	-
LCMF	49.2	-	-	3-7	200
*2^{rd} and 3^{rd} stage has smaller $W_{1,2}$, **Double W_0					

In Fig. 14, the Bode gain plot of all four comparator topologies are plotted for a load of 25 pF and for $V_{\rm dd}$ = 15 V. The designs are optimized for max gain performance, except from the NSFB comparator which is optimized for speed. The second and third stage of the NSFB design has $W_{1,2}$ four times smaller than the $W_{1,2}$ of 1st stage. The ISFB design has the highest ac gain of 50 dB and BW of 100 Hz. The LCMF has lower gain of 49.2 dB but it is faster. A BW of 200 Hz is achieved, most likely because of higher bias currents. The DGDL has slightly lower gain (47.2 dB) and BW of 120 Hz. The smaller input transistors of the second and third stage of the NSFB is indeed increasing the bandwidth of the topology but it results in the smallest gain (46.5 dB).

In addition, in Table II, measurements for the CMRR, PSSR, and common-mode input range are shown. The DGDL design has decent performance in all parameters in addition to robustness, as shown in Fig. 4. Similar numbers are also demonstrated from the ISFB topology, plus the extra wide input range, most likely caused by the extra gain push by the BG. LCMF is last in our choices due to the narrower ICM, which actually is also under $V_{\rm dd}/2$. Improvement of PSSR and CMRR performance is noticed when bias TFT T_0 is doubled in width, most likely due to the larger bias current. PSSR and CMRR performances are measured in dc mode. The chosen comparator architecture for the ADC is the DGDL with TFTs: $T_{1,2}$ = 2 mm/30 μm, $T_{3,4}$ = 20 μm/80 μm, and T_0 = 400 μm/30 μm (see Table III).

4) Output Buffers: Output buffers are placed after the comparator, not only to amplify the signals but also to provide another option to filter out variabilities and to adjust the output zero threshold level of the comparator. The zero threshold level of the output signal can be moved when DG inverter is used [4]. The cross point of the inverter is shifted toward

TABLE III
SIZES OF TFT OF ALL STAGES OF FOUR COMPARATOR TOPOLOGIES TESTED EXPERIMENTALLY

design	all T_0	stage 1 $T_{1,2}$	stage 1 $T_{3,4}$	stage 2 $T_{1,2}$	stage 2 $T_{3,4}$	stage 3 $T_{1,2}$	stage 3 $T_{3,4}$
NSFB	400/30	2000/30	20/60	1000/30	20/60	1000/30	20/60
ISFB	400/30	2000/30	20/60	2000/30	20/60	2000/30	20/60
DGDL	400/30 (800/30)	2000/30	20/60	2000/30	20/60	2000/30	20/60
LCMF	2*130/30	2000/30	20/80	2000/30	20/80	2000/30	20/80
channel Width/Length, in μm							

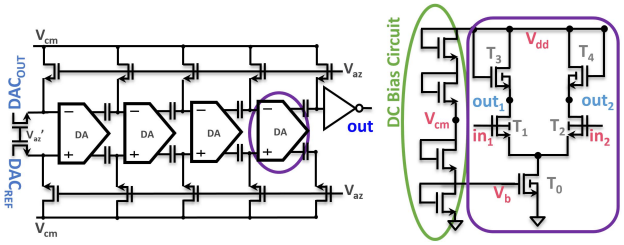

Fig. 15. Implemented comparator block diagram with open-loop offset cancellation and detailed schematics of the DA stages and the dc bias circuitry.

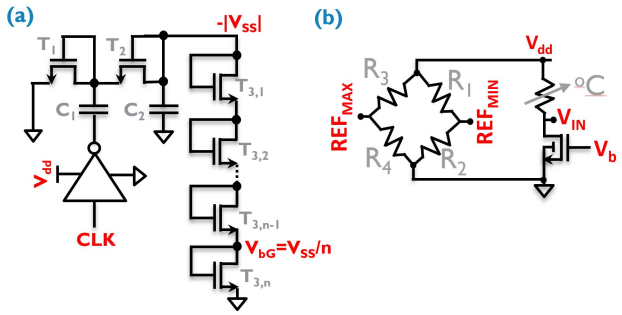

Fig. 16. (a) Dickson charge pump driven by a pseudo-CMOS driver and resistive divider for negative BG voltage level creator. (b) Schematic of the implemented sensor read-in circuitry and the sensor (as temperature-dependent resistor) and the references resistor network.

lower or higher input voltages by changing the bias of the BG of the pull-down TFT. The appropriate negative BG voltages can be generated on PI foil by a charge pump, which is discussed in Section VI. The sizing of the TFT of inverter are 1 mm/30 μm for the pull-down TFT and 30 μm/60 μm for the pull-up TFT.

5) Offset Cancellation: Auto-zeroing with output offset storage (open-loop) of each stage of the comparator (see Fig. 15) is used to cancel the observed offset between neighboring TFTs. With offset cancellation, the minimum detectable V_{LSB} is decreased resulting in an increase of the achieved ADC resolution. Due to the capacitive voltage divider created with the input transistor of the next stage, the overall gain of the comparator is reduced. Therefore, an additional DA stage is used to boost the gain to meet the system specification. The offset cancellation operates in two phases. In the first phase, the signals V_{AZ} are high, resetting the input nodes of the DAs of all four stages of the comparator with voltage V_{cm}. The output offset is stored at the capacitors. At the second phase, the inputs to be compared are set to the input of the comparator.

6) DC Bias Circuitry and Dickson Charge Pump: The system is using only two power supplies (V_{DD} and V_{BIAS}), a ground and a clock. All other required bias voltage levels are generated on PI foil using four cascoded and diode-connected TFTs as is shown (green circle) in the schematic of Fig. 15. The system has low-level current requirements, mainly because the high-impedance nodes are biased, i.e., gates and BGs of TFTs. Therefore, the accuracy of the required generated levels; $V_b = 3.75$ V for biasing the current sources T_0 of the comparator; and $V_{\mathrm{cm}} = 7.5$ V to reset the input $T_{1,2}$ of the DAs, is under 1%.

Output buffers, as mentioned in Section IV, need negative voltages to regulate their zero threshold level. Negative voltages are created on PI foil using a Dickson charge pump [22], where the clock, power supply V_{DD}, and ground of the system are inputs [see Fig. 16(a)]. From measurements, the output voltage V_{SS} is kept to less than 10% voltage drop for loads up to 1 nA. In addition, a laser-tunable resistive divider, formed by diode-connected TFTs, is connected to the output of the charge pump to set the optimum voltage level for biasing the BG of the output inverters of the comparator, as explained in Section IV. Note that $C_2/C_1 = 10$, $T_{1,2} = 10$ μm/15 μm, and $T_3 = 10$ μm/50 μm.

7) C-2C DAC: The DAC is implemented by two C-2C capacitor networks (see Fig. 17), one for the sensor's input V_{IN} (network A) and the other to form the reference value of the comparator from the minimum reference $\mathrm{REF_{MIN}}$ of the sensor's operation range (network B) (see Fig. 6). The C-2C topology is chosen due to the excellent matching of the MIM capacitors and the small footprint. A local standard deviation of 22 fF is measured for a 11.4-pF capacitor (0.2% variation). In simulation, applying the variation on all capacitors at any of the two networks gives a minimal variation at output $\Delta V_{C2C}/V_{\mathrm{LSB}} = 1.78\%$. In addition, the capacitors are placed in a concentric way for each network so that no overlaps of the metal lines are present from the switches. The order of the capacitors is following the sequence: bit4, bit5, bit3 bit2, bit0 and bit 1 to spread any technology variations over the bits. The capacitor networks and the applied control signals (min, ... min_5, max, ... max_5, in) are identical except for the input signals. Network A is driven by the voltage in conversion V_{IN}, the minimum reference ($\mathrm{REF_{MIN}}$), and the maximum reference ($\mathrm{REF_{MAX}}$), whereas the second C-2C network is only driven by $\mathrm{REF_{MIN}}$ following the switching pattern of network A. The purpose of B is to alleviate any distortion caused by the switching effects, the injected charges and the coupled noise.

B. Digital Control Block

The DCC block is used to control the switch TFTs of the C-2C networks and the offset cancellation TFTs of

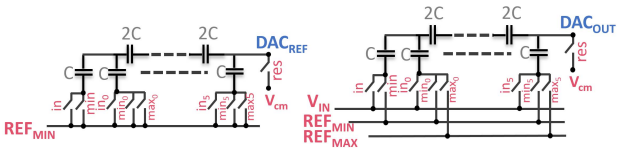

Fig. 17. Implemented C-2C DAC schematic for the ADC.

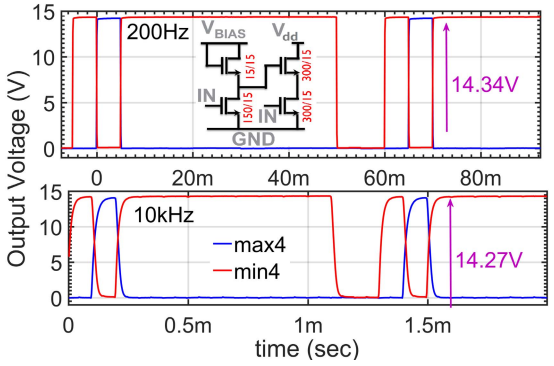

Fig. 18. Measured transient output response of the two digital control signals (from 13) created from the digital control block with TFTs on flex substrate and used to control the analog block of the ADC.

the comparator. The DCC has two input signals: the output of the comparator of the ADC and the clock. The DCC has 13 outputs since it is designed for 5-bit C-2C ADC. The operation principle of the DCC is described in detail in Section IV. The footprint of the digital control block measures 8.2 mm × 9.2 mm.

The digital control was implemented using pseudo-CMOS logic [23], shown in the inset of Fig. 18. The pseudo-CMOS logic was chosen to increase robustness and to create accurate rail-to-rail signals to drive the switches of the C-2C networks. Robust and accurate signals ensure the maintenance of the charges at the capacitors of the C-2C network and the uniformity of the injected charges to the capacitors of the C-2C network. The drawbacks of this implementation are the doubled area (four TFT inverters) and the power efficiency for the lowest power supply. Power dissipation can be improved by the optimization of the pseudo-CMOS gates [5], where 7.5 mW is reported from 1712 TFTs comprising a digital block. For a 19-stage ring oscillator, a power reduction of up to one order of magnitude is measured with 50% increase in stage delay for the same supply voltages by optimized TFT sizing of the logic gates. Furthermore, power and area reduction can be achieved with the use of DG logic [4] already available in the technology and feedback reduces power up to 90% [25]. Finally, the use of more logic gates and improvement of the digital flow can decrease the number of used TFTs in the block.

The measured power dissipation of the DCC is $P_{\mathrm{DCC}} = 226.1$ mW at $V_{\mathrm{DD}} = 15$ V and $V_{\mathrm{BIAS}} = 30$ V. The generated control signals have a peak-to-peak voltage of $V_{\mathrm{DCC}} = 14.34$ V with accurate timing. The majority of the power is dissipated from the V_{BIAS} branch. Reducing V_{BIAS} to 20 V lowers the power dissipation more than three

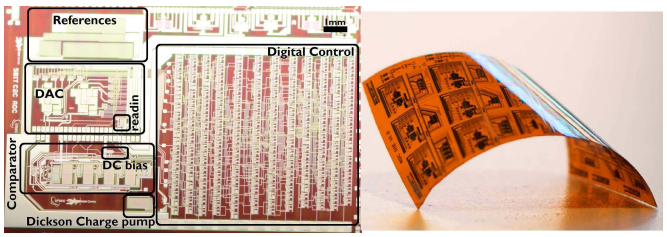

Fig. 19. Microphotograph of the RFID-ready SAR C-2C ADC with labels indicating all the main blocks at the top and a photograph of the bent ADC die on PI foil at the bottom.

times to $P_{\mathrm{DCC}} = 71$ mW, but V_{DCC} decreases 17% to 13.2 V. The rise time of the control signals is $t_{\mathrm{rise}} = 27\ \mu$s and the fall time $t_{\mathrm{fall}} = 22\ \mu$s for load of 1 pF and 1.25 MΩ. In Fig. 18, the response of two signals (max4 and min4) are shown for 200 Hz clock and 10 kHz clock for $V_{\mathrm{DD}} = 15$ V and $V_{\mathrm{BIAS}} = 30$ V. The maximum OFF voltage achieved is 0.09 V, which is considered sufficient to turn off the switch TFTs used in the C-2C. As seen in Fig. 9, the drain current for $V_{\mathrm{GS}} = 0.1$ V is in the pA range for high $V_{\mathrm{DS}} = 10$ V.

C. References

The references are formed by SD metal routing, which has a resistivity of 3 Ω/square and a good global variability $\sigma < 0.1\Omega$/square over 280-cm^2 area. More importantly, SD metal has excellent local variability, achieving 0.7% offset matching. Therefore, the references ($\mathrm{REF_{MIN}}$ and $\mathrm{REF_{MAX}}$) for the ADC are created by two pairs of resistors (R_1 and R_2, R_3, and R_4) in series biased by V_{DD} and ground [see Fig. 16(b)]. The four resistors are in the kΩ range, to balance power dissipation and footprint (about 10 mm^2). In addition, extra space is used to make the resistor tunable by laser-cut to tweak the final value of the resistors and accommodate any sensor technology variations up to 30%. Several metal lines (n) of equal length (and resistance ΔR) are shorted to the main resistor R (smaller than the needed one). By a step-by-step laser-cut process the lines are added to the main resistor to increase the final value of the total resistor $R_{\mathrm{TOTAL}} = R + n \cdot \Delta R$.

D. Sensor Read-In

In this implementation, the current-source sensor read-in scheme is chosen. First, because only the NTC sensor is used, and second, due to the excellent output resistance properties achieved when the BG of the TFT is connected to source (see Fig. 8). Output resistance up to $r_o = 1$ GΩ and 200 MΩ for $V_{\mathrm{GS}} = 3.75$ V and 7.5 V is calculated from the measurements of $L = 30\ \mu$m TFTs. In addition, the bias of the temperature-dependent resistor with a constant current source provides a wider output voltage range to the ADC compared to any bridge resistor configuration, without a pre-amplifier, except the case where both positive and NTC are available and matching.

IV. Analog-to-Digital Conversion

In Fig. 19, a microphotograph of the fabricated system on PI foil with labels of the basic blocks, discussed in Section III,

TABLE IV

PERFORMANCE SUMMARY AND STATE-OF-THE-ART COMPARISON TABLE (*CALCULATED)

	Complementary Technology				Unipolar Technology						
Technology	Poly-Si (2009)	Poly-Si (2010)	OTFT (2010)	OTFT (2013)	OTFT (2011)	a-Si:H (2012)	OTFT (2013)	DG ESL IGZO			
Architecture	2nd $\Sigma\Delta$	Flash	SAR	Counting	1st $\Delta\Sigma$	Flash	VCO-based	ADSM	C-2C SAR	C-2C SAR	
Tech Specs	L=3µm 1P2M LTPS	μ_n=281cm^2/Vs μ_p=98cm^2/Vs L<8m	μ_n=0.02cm^2/Vs μ_p =0.5cm2/Vs L=20µm	Printing	Pentacene based dual gate organic TFTs	BCE V_T=1.2V μ_n=0.8cm^2/Vs	L=5µm	μ_n=14cm^2/Vs L>15µm	μ_n=8.8cm^2/Vs V_T=3.8V L>15µm	μ_n=12.7cm^2/Vs, V_T=3.7V L=30µm (Analog), L=15µm (Digital)	
ADC specs	SDR=69dB SNDR=65.63dB OSR=128	3 bit	6 bit	SDR=25.7dB SNDR=19.6dB ENOB=3bit	SDR=24.5dB SNR=26.5dB OSR=16	5 bit	SNR=48dB ENOB=7.7bit	SNDR=50dB ENOB=8bit | SNDR=40dB ENOB=6bit	SNDR=37.1dB ENOB=5.87bit	SNDR=35.9dB ENOB=5.7bit	5bit
FoM (µJ/c.s.)	0.014*	-	-	17	3.45	-	0.69	0.390 | 0.039	0.0667	0.026	-
Power *(mW)*	63.3 (11.2V)	13V	0.004 (3V)	0.540 (40V)	1.5 (15V)	13.6 (20V)	0.048 (20V)	2 (20V)	0.049 (15V)	0.073 (15V)	245 (30V)
Sampling Rate *(S/s)*	400k	3M	10	2	15.6	2k	167m	10 | 300	13.3S/s | 26.6S/s	26.67	13.34
FSR *(V)*	-	10	2	-	-	10	-	-	6	6	
Footprint *(mm^2)*	26	3.75	700	2450	260	-	19.4	27.9	27.5	27.5	150
substrate	glass	Steel foil	glass	foil	foil	Flex compatible	foil	PI foil	PI foil	PI foil	
Integration	Only analog	+Decoder	Only analog	Counter Comparator and DAC	Only analog	Only analog	+Metal resistors +Logic	PWM output only	+offset cancellation +DC biasing	+offset cancel +DC biasing	+Digital Control +References Sensor read-in
Authors	Lin et al. [9]	Jamshidi-Roudbari et al.[10]	Xiong et al. [12]	Abdinia et al. [15]	Marien et al.[11]	Dey and Allee [13]	Raiteri et al. [14]	Garripoli et al. [19]	Papadopoulos et al. [20]	This work	

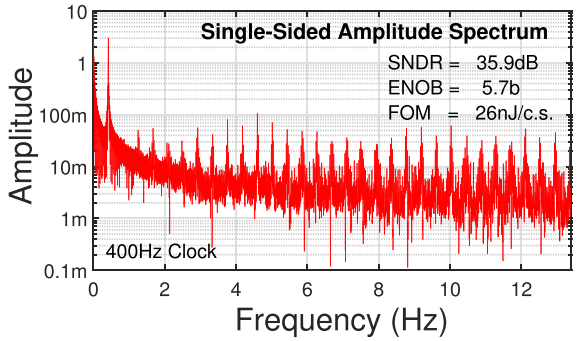

Fig. 20. Amplitude spectrum of the output of the ADC at a clock frequency of 400 Hz and $V_{dd} = 15$ V for a sine wave of 416-mHz signal.

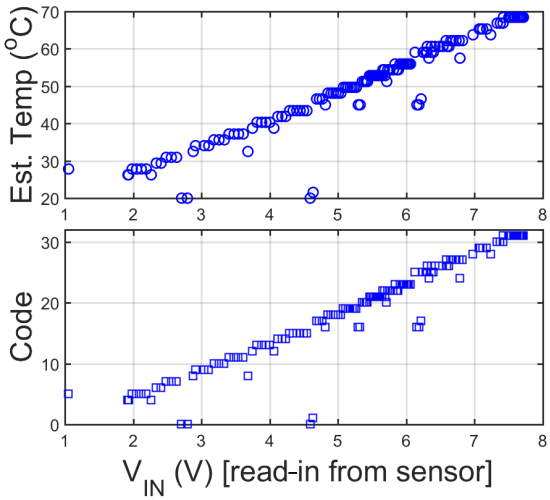

Fig. 21. Measured digital code output and estimated temperature readout from analog input of printed NTC sensor on PI foil and converted from the fabricated RFID-ready ADC.

is shown. Also, at the bottom of Fig. 19, a photograph of the flexible 40-μm PI die is shown demonstrating the bending properties of the substrate [24]. The footprint of the RFID-ready ADC is 1.5 cm^2. Only six pins are needed to interface the developed sensor system: two power supplies V_{DD} and V_{BIAS}, ground, clock, serial digital output, and analog input from the sensor (see Fig. 6).

Each conversion cycle starts resetting the output nodes of the DAC (DAC_{OUT} and DAC_{REF}) and also sampling the analog V_{IN} from the sensor readin to the bottom plates of the capacitors of network A, by shorting switches res and in. Then, res opens leaving DAC_{OUT} and DAC_{REF} floating and the bottom plates connect to REF_{MIN} through switches min, min_0 to min_5 (switch in opens). Subsequently, only max_5 goes high (and simultaneously min_5 goes low) and shorts the corresponding node to REF_{MAX} initiating the first comparison of the MSB. Depending on the result of the comparison, max_5 and min_5 created by the digital control block will retain their state or toggle to the opposite. Then bits 4, 3, 2, 1, and 0 are similarly evaluated. The digital output of the ADC is serial in time.

A. Analog Performance Evaluation

To evaluate the analog performance of the system, only the analog part of the ADC, namely, comparator, DAC, and dc bias circuitry, is driven by an external microcontroller and a sine wave of $V_{pp} = 6$ V and 416 mHz is applied to its input. The FFT of the reconstructed sine wave signal from the comparator's output is calculated and plotted in Fig. 20 to extract SNDR = 35.9 dB and calculate an ENOB = 5.7 bit for a clock of 400 Hz (26.67 S/s). The figure of merit (FoM) is also calculated as FoM = 26 nJ/c.s. for an ADC on 40-μm-thick PI foil. The power dissipation of the analog part including the dc biasing circuitry is 73 μW.

Table IV shows the summary of the state-of-the-art thin-film ADCs. The presented 6b C-2C ADC achieves state-of-the-art FoM for unipolar technology and second best overall thin-film ADC FoM. The overall footprint of the design is, considering the large length TFT used, relatively small. The speed (26.67 S/s) of the design is rather slow, due to the required number of clocks (15) to complete the successive comparisons, compared to the ADSM implementation [19]. The load at the output of the ADC is 25 pF, due to measurement setup.

B. RFID-Ready ADC With Temperature Sensor

Furthermore, the RFID-ready version of the ADC, namely, the ADC with plastic digital control, integrated references, and

sensor readin was evaluated together with a printed −4.6/°C NTC sensor on a different PI foil. A hot plate was used to gradually increase the temperature on the sensor from room temperature (25 °C) to approximately 70 °C. The measured output digital code from the RFID-ready ADC to the analog input of the NTC sensor is shown in Fig. 21. The total experiment time is 42 min, due to the slow transfer of the heat from the hotplate to the sensor. The resolution of the implemented RFID-ready ADC is 5 bit, as also verified by the 32 digital codes in Fig. 21. In addition, the estimated uncalibrated temperature is shown in Fig. 21. The response of the output of the RFID-ready ADC to the read-in analog input is linear at the sampling speed of 13 S/s, with some outliers. The total power dissipation is 245 mW at $V_{\rm dd} = 15$ V and $V_{\rm BIAS} = 30$ V. The breakdown of the power is: 226.1 mW for digital control, 17.7 mW for reference creation, 1.425 mW for sensor readin, and 73 μW for the analog. The footprint of the six-pin RFID-ready ADC is 1.5 cm^2.

V. Conclusion

This paper presents and validates an RFID-ready ADC on thin PI foil for low-cost Internet-of-Everything applications using unipolar DG ESL IGZO TFTs. The presented measurements correspond to a design that not only implements the analog part but also demonstrates the accurate dc self-biasing and offset compensation to overcome accuracy and increase the effective resolution, digital control circuitry, laser programmable references, and sensor read-in circuitry. The analog part of the ADC achieves an ENOB = 5.7 bit and FoM = 26 nJ/c.s. from 15-V supply when driven from an external microcontroller. The RFID-ready ADC is working with an externally supplied clock up to 400 Hz to generate on foil the appropriate control signals to drive the C-2C ADC. The presented RFID-ready ADC is realized on 40-μm-thick PI foil and is demonstrated and verified together with a printed NTC sensor to enable on-skin and sensor tags applications occupying 1.5 cm^2 in $L > 15$-μm technology. In total, only six pins are needed to operate the ADC: two power supplies, ground, sensor's analog input, serial digital output, and clock.

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Dr. Myny was listed as one of Belgium's top tech pioneers by the business newspaper De Tijd. In 2016, he received a prestigious European Research Council Starting Grant from the European Commission to enable breakthrough research in thin-film transistor circuits (FLICs).