# Flexible 16nJ/c.s. 134S/s 6b MIM C-2C ADC using Dual Gate Self-aligned Unipolar Metal-Oxide TFTs

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***Abstract*—In this work a metal-oxide (Indium Gallium Zinc Oxide) 6-bit successive approximation metal-insulator-metal C-2C analog to digital converter (ADC) fabricated on 15$\mu$m thick flexible substrate is demonstrated. The ADC is operated at a clock speed of 2kHz and at a power supply of 15V. The power dissipation including output buffers is 212$\mu$W at 15V and the a sampling rate of 134S/s. The ADC achieves a figure of merit (FoM) of 16.58nJ/c.s. and no missing codes using dual gate self-aligned n-type thin-film transistors on polymeric substrate.**

## I. Introduction

Analog oriented circuitry on metal-oxide large area technologies (LAE) and flexible substrates using Indium Gallium Zinc Oxide (IGZO) thin-film transistors (TFTs) are being demonstrated in recent literature [1]-[6]. The LAE technology is expanding to other applications than flat panel displays, such as inductive RFID tags [7] for Internet-of-Everything applications, bio-potential measurements [6] and imaging for fingerprint sensing.

More specifically, multiple ADC topology implementations using LAE technologies (a-Si, organic or low-temperature polycrystalline silicon) on glass or flexible substrates have been presented in the literature [8]-[12]. Recently, more specifically $\Delta$-$\Sigma$ [3] or successive approximation (SAR) implementations [2] are enabling new temperature sensing applications counting on uniformity over large areas, stability and relative high mobility of IGZO TFTs. Other applications, such as in-panel fingerprint sensing on mobile displays, require faster sampling rates than temperature sensing. Etch-stop-layer (ESL) IGZO TFTs exhibit fair stability, very low leakage currents, low fabrication cost and good uniformity at room temperature fabrication but suffer from metal-overlap parasitics. Self-aligned dual gate (SADG) IGZO TFTs can provide faster responses due to negligible overlap parasitics [7]. Therefore, we propose a new design of a 6-bit metal-insulator-metal (MIM) C-2C ADC using unipolar SADG IGZO TFT.

This paper is outlined as follows. The performance and uniformity of the dual gate self-aligned gate metal oxide technology is briefly discussed in section II. The proposed ADC design and operation is presented in section III followed by the experimental results in section V. SectionVI summarizes the C-2C ADC results.

## II. Metal Oxide Technology

Fig.1 shows the cross-section of the SADG IGZO technology [13]. The dual-gate transistor comprises of two gates: a back-gate (BGate M0) and a front-gate (Gate M1). No additional metals are available for interconnect and routing purposes of the ADC. The self-aligned architecture is selected for its minimum parasitic overlap capacitance between gate and source-drain, its smaller footprint and its ability to decrease the channel length to the critical dimension of the technology, compared to ESL or back-channel etch (BCE) TFT architectures. The total thickness of the wafer is 15$\mu$m.

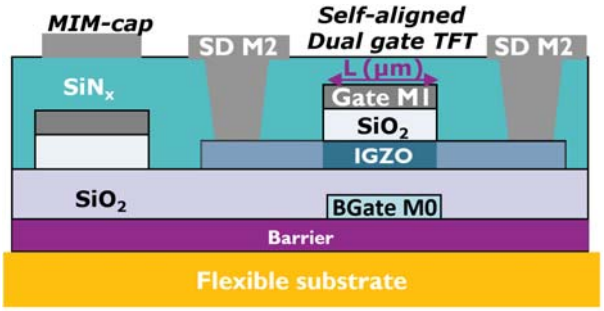


Fig. 1. Dual Gate Self-aligned IGZO TFT and metal-insulator-metal capacitor cross section.

SADG TFT were fabricated on GEN1 (320x352mm) substrate size. Since for circuitry performance, 'local' uniformity is key, Fig. 2 shows the transfer curves (IDS-VGS) in saturation of 32 devices across a 150mm$^2$ wafer area cut down from GEN1, whereby Gate and BGate are connected. The samples have channel width and length of respectively 480$\mu$m and 20$\mu$m, which is the largest footprint TFT used in the design of the ADC. The off current measurement is limited by the semi-automatic measurement setup. Fig. 3 plots the extracted variability on threshold voltage ($V_T$) and effective dual-gate mobility ($\mu_{EFF}$) over 150mm$^2$ wafer for the 32 devices. The wafer average $V_T$ is 1.77V ($\sigma V_T$=93mV) and average $\mu_{EFF}$ is 22.97cm$^2$/Vs ($\sigma\mu$=1cm$^2$/Vs) over 150$mm^2$ area. The apparent mobility is larger compared to literature because of the effect of having two gates controlling the channel.

## III. Details on ADC Design

Fig. 4 depicts the block diagram of the implemented SAR ADC. The flexible ADC comprises of a C-2C network, a comparator and voltage buffers implemented with the SADG TFT technology. The digital signals (min, min0-6, max0-6, SELIN, res, VAZ) to control the flexible analog TFT chip have been generated by programming a silicon microcontroller.

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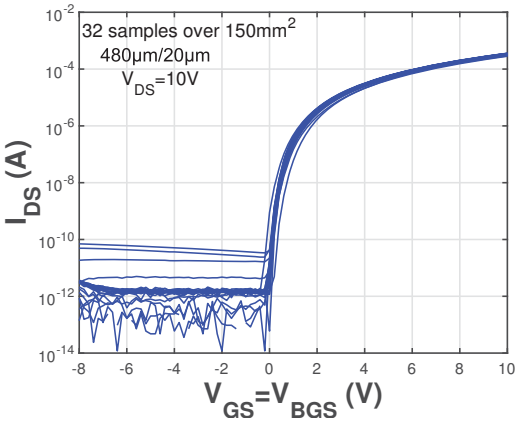


Fig. 2. Measurements of 32 devices of 480$\mu$m/20$\mu$m SADG IGZO TFT across a 150mm$^2$ wafer.

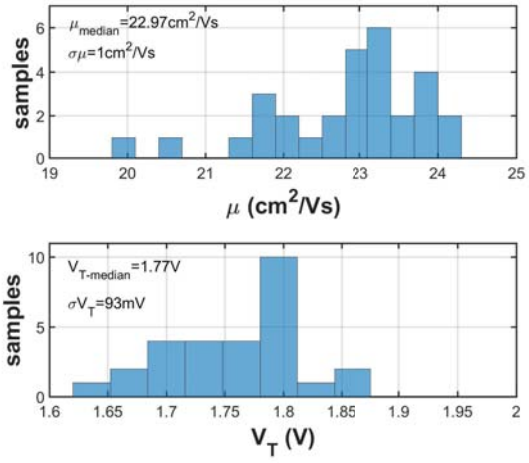


Fig. 3. Wafer threshold voltage ($V_T$) and effective mobility ($\mu_{EFF}$) spread (32 samples) of W/L=480$\mu$m/20$\mu$m SADG IGZO TFTs extracted at $V_{DS}$=10V across a 150mm$^2$ wafer.

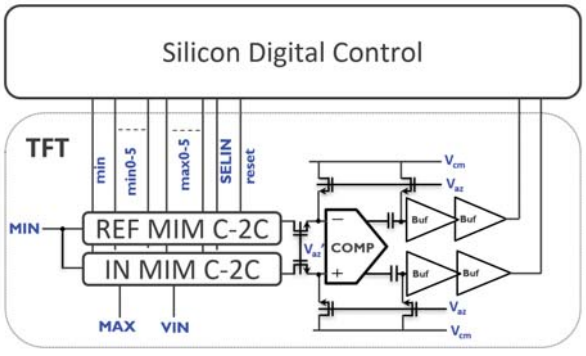


Fig. 4. The implemented SADG TFT ADC block diagram driven with external silicon digital control.

The C-2C networks are utilizing metal-insulator-metal (MIM) capacitors between Gate and SD layer due to the very small

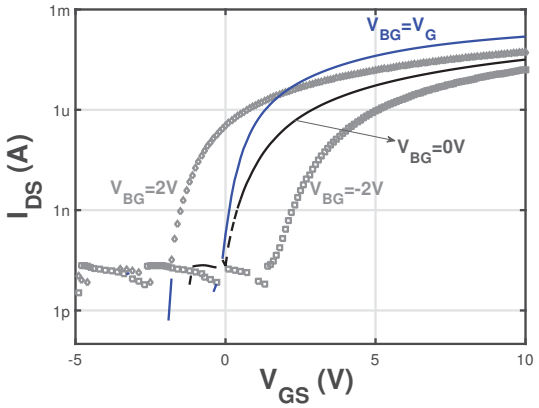


Fig. 5. Measured transfer characteristics of SADG IGZO TFT when back gate (BG) connected to various biases (-2,0,2V) including when shorted to front gate (G).

mismatch ($< 0.2\%$). Each capacitor of the C-2C networks is 5pF. The access switches of the C-2C network are dual gate transistors with shorted BG to G. Shorting BG to G improves the subthreshold-slope of the transistor decreasing the leakage current when TFTs are switched off, as is shown in Fig.5. In addition, shorting BG to G improves the on resistance of the switch compared to all the other bias options.

Two different implementations of the comparator have been designed, whereby the minimum TFT size has been down-scaled from 20$\mu$m to 5$\mu$m (Fig.6). The transient response of the comparator with open-loop offset cancellation is shown in Fig.7 for those two channel length designs. Auto-zeroing with output offset storage is used to cancel the observed offset of TFTs of more than 100mV, necessary considering both mobility and threshold voltage mismatch (fig.3). Fig.7 depicts the response of the comparator for two different input signals: $\Delta V_{in}$=0V and $\Delta V_{in}$=10mV operating at (a) 3kHz for L=20$\mu$m design and (b) at 10kHz for the L=5$\mu$m design. Offset cancellation is necessary to decrease the minimum detectable $V_{LSB}$ and increase the achieved resolution of the ADC minimizing non-uniformities. A microcontroller is used to control the ADC. Recently, TFT digital control circuits have been demonstrated successfully [2] with more than 1300 IGZO TFTs for a 5b ADC on flexible substrate.

## IV. Experimental Results

In Fig. 8 a micrograph of the fabricated TFT ADC on 15$\mu$m flexible polyimide foil is shown. The total footprint of the design measures 8.88mm$^2$. The two main block are labeled on the micrograph image. The comparator and C-2C network occupy the majority of the space. A total number of 91 SADG TFTs and 34 capacitors (C=5pF each) for the C-2C and 6 capacitors (32pF each) for the auto-zero offset cancellation are used in the ADC. The switches are designed with a channel length of L=5$\mu$m and the minimum TFT channel length in the comparator is L=20$\mu$m. The ADCs maximum clock of 2kHz is a consequence of the long channel length of the comparator.

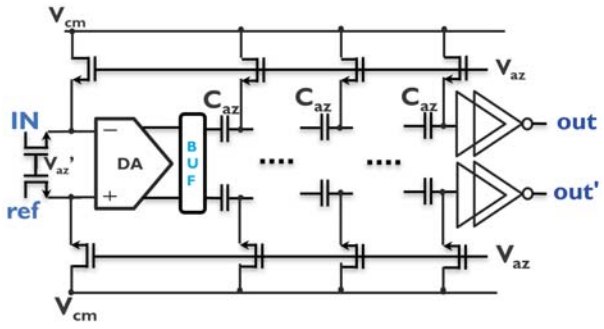


Fig. 6. The schematic of the comparator with offset cancellation and the voltage output buffers.

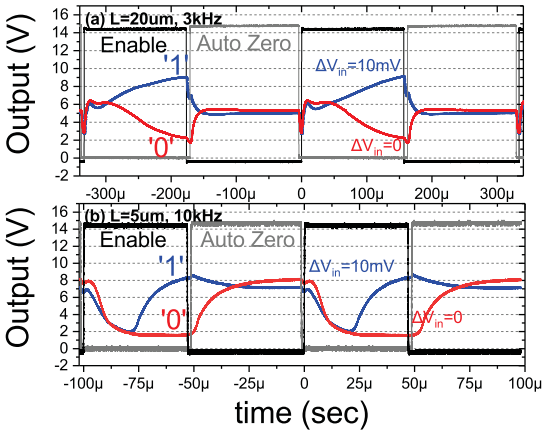


Fig. 7. Measured comparator output with auto-zero offset cancellation for designs using TFT of minimum (a) L=20$\mu$m at 3kHz and (b) L=5$\mu$m at 10kHz.

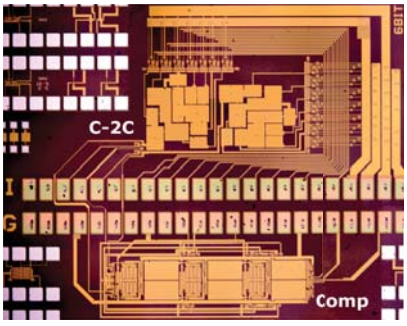


Fig. 8. A microphoto of the 6-bit MIM C-2C ADC on flexible substrate.

According to Fig.7 (b), sampling speed of the comparator can be increased to more than 5 times by scaling down the channel length to 5$\mu$m, enabling a 1fps readout for a 1 megapixel fingerprint imager.

## V. Experimental Results

Fig. 9 shows the DNL and INL performance of the L=20$\mu$m ADC at 2kHz (134S/s). The maximum obatined DNL and INL are 0.83LSB and 0.9LSB respectively at a clock frequency of

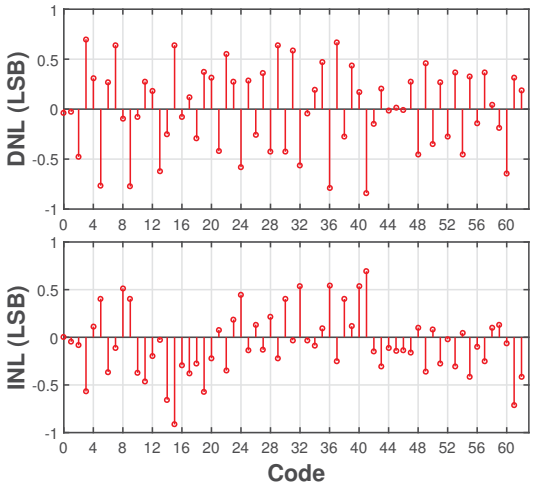


Fig. 9. Measured DNL and INL of the 6 bit MIM C-2C ADC operated at 2kHz on flexible substrate.

2kHz. The total power dissipation of the TFT-part of the ADC is 212$\mu$W at $V_{dd}$=15V. whereby comparator dissipates only 6$\mu$W (2.8%). The majority of the power is dissipated by the 2-stage output buffers (206$\mu$W).

In Fig.10 the reconstructed sinusoidal wave signal (green circles) from the digital output of the ADC is shown compared to the 2.064Hz sinusoidal wave (pink line) applied at the input of the ADC. In the bottom graph the FFT of the reconstructed sinusoidal wave signal is plotted to extract a SNDR=35.48dB. The calculated ENOB is 5.61bit at a system clock of 2kHz (134S/s). The obtained figure of merit (FoM) of the ADC on foil with integrated offset cancellation is also therefore 16.58nJ/c.s. for this 2kHz clock.

Table I displays a thin-film ADC state-of-the-art comparison and performance summary table. The presented TFT C-2C ADC on flexible substrate has 40% smaller FoM compared to state-of-the-art for unipolar technologies [2], [3], [10],[12] and is only 2nJ/cs larger than state-of-the-art of complementary TFT technologies. Moreover, the proposed ADC achieves DNL/INL figures smaller than 0.9LSB, demonstrating no missing codes. The proposed ADC has up to 5 times faster sampling speeds compared to earlier C-2C implementations and threefold smaller footprint. The larger power dissipation is mainly attributed to the high power dissipation of the output buffers.

## VI. Conclusion

This paper presents a 6 bit TFT-based C-2C ADC on thin flexible substrate (15$\mu$m) using SADG IGZO TFTs occupying only 8.88mm$^2$. The presented measurements achieve a SINAD=35.48dB and ENOB=5.61bit with 220$\mu$W dissipated power at 15V supply. The ADC is operating at a clock up to 2kHz supplied externally from a microcontroller due to the L=20$\mu$m comparator. The calculated FoM is 16.58nJ/c.s. Moreover, a more than 5 times faster comparator with down-scaled SADG IGZO TFTs (L=5$\mu$m) is demonstranted promis-

TABLE I
PERFORMANCE SUMMARY AND STATE-OF-THE-ART COMPARISON TABLE (*CALCULATED)

| | Complementary Technology | | | Unipolar Technology | | | | |
|---|---|---|---|---|---|---|---|---|
| **Technology** | Poly-Si (2009) | Poly-Si (2010) | OTFT (2010) | a-Si:H (2012) | OTFT (2013) | DG ESL IGZO (2017-18) | | SADG IGZO |
| **Architecture** | 2nd $\Sigma\Delta$ | Flash | SAR | Flash | VCO-based | ADSM | C-2C SAR | C-2C SAR |
| **Tech Specs** | L=3µm 1P2M LTPS | $\mu_n$=281cm$^2$/Vs $\mu_p$=98cm$^2$/Vs L<8µm | $\mu_n$=0.02cm$^2$/Vs $\mu_p$ =0.5cm2/Vs L=20µm | BCE $V_T$=1.2V $\mu_n$=0.8cm$^2$/Vs | L=5µm | $\mu_n$=14cm$^2$/Vs L>15µm | $\mu_n$=12.7cm$^2$/Vs, $V_T$=3.7V, L=30µm | $\mu_{EFF}$=22.4cm$^2$/Vs, $V_T$=2.56V, L=20µm |
| **ADC specs** | SDR=69dB SNDR=65.63dB OSR=128 | 3 bit | 6 bit | 5 bit | SNR=48dB ENOB=7.7bit | SNDR=50dB ENOB=8bit \| SNDR=40dB ENOB=6bit | SNDR=35.9dB ENOB=5.7bit | SNDR=35.53dB ENOB=5.61bit |
| **DNL/ INL** *(LSB)* | - | 0.25/0.25 | -0.6/0.6 | 1/1.8 | 0.6/1 | - | 0.8/0.69 | 0.83/0.9 |
| **FoM** (nJ/c.s.) | 14* | - | - | - | 69 | 390 \| 39 | 26 | 16.58 |
| **Power** *(mW)* | 63.3 (11.2V) | 13V | 0.004 (3V) | 13.6 (20V) | 0.048 (20V) | 2 (20V) | 0.073 (15V) | 0.212 (15V) |
| **Sampling Rate** *(S/s)* | 400k | 3M | 10 | 2k | 167m | 10 \| 300 | 26.6 | 134 |
| **Footprint** *($mm^2$)* | 26 | 3.75 | 700 | - | 19.4 | 27.9 | 27.5 | 8.88 |
| **substrate** | glass | Steel foil | glass | Flex compatible | foil | PI foil | PI foil | PI foil |
| **Integration** | Only analog | +Decoder | Only analog | Only analog | +Metal resistors +Logic | PWM output only | +offset cancellation +DC biasing | +offset cancellation |
| **Authors** | [8] | [9] | [10] | [11] | [12] | [3] | [2] | This work |

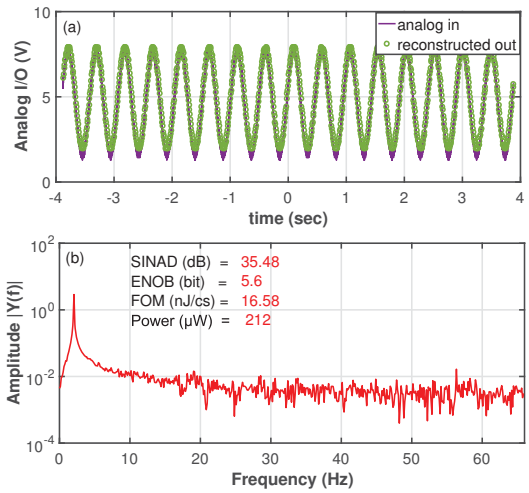


Fig. 10. (a) The analog input 2.061Hz sinwave signal to the ADC and the reconstructed output points from the digital output of the ADC at a clock frequency of 2kHz and (b) the amplitude of the fft of the digitized output of the ADC.

ing faster ADCs aiming for in-panel fingerprint sensing for flat panel displays applications.

## ACKNOWLEDGMENT

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