A mission profile-based reliability analysis framework for photovoltaic DC-DC converters

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Abstract

Reliability of DC-DC converters is important in photovoltaic (PV) applications like building integrated PV systems, where the module-level converter may be stressed significantly. Understanding and predicting the most failing components with accurate degradation models in such systems enables the design for reliability. In this paper, a photovoltaic mission profile-based reliability analysis framework is proposed where the inputs and models of the framework can be adjusted according to the converter topology, the components and the failure mechanisms under investigation. The framework is demonstrated by comparing the influence of two different one-year mission profiles on the solder joint degradation of a MOSFET in an interleaved boost converter. This is done by using an electro-thermal circuit simulation in PLECS and a finite element MOSFET model in COMSOL. In future work, the mesh and the geometry of the solder joint can be adjusted to more closely match the practical stress-cycle (S-N) curve used to determine the lifetime. This framework allows for exploring more accurate models or even simplify parts with low sensitivity in order to obtain a thorough understanding of their accuracy and to determine the overall converter reliability.

1. Introduction

Building integrated photovoltaics (BIPV) are becoming more popular, where module-level DC-DC converters are employed. Under varying operation conditions, the DC-DC converter may be stressed significantly, leading to failures. Typical lifetimes of facade building elements are 50-75 years [1], meaning that the converters in BIPV systems should be designed to avoid frequent replacements—the power converter should be highly reliable. Degradation models of the most failing components provide insights in the overall reliability of the converter. By considering the mission profile, they also determine whether the converter can be over or under dimensioned and potentially reduce the entire cost. In this regard, reliability modelling and analysis is of importance. The reliability modelling of electronic components has evolved towards a more physics-based approach to better understand and counteract the failures [2]. A flexible framework is needed to investigate the influence of different mission profiles and/or different physics-based models on the calculated lifetime of the components.

2. Framework structure

In this paper, a reliability framework is proposed which allows any input or (sub)component-model to be exchanged by alternate or improved versions depending on the application, topology, components or failure mechanism(s). The flowchart of the framework is shown in Fig. 1. This paper demonstrates this methodology on the case of an interleaved boost converter for BIPV systems. More specifically, the influence of two one-year mission profiles from Denmark and Arizona on the material degradation of the solder joint of the MOSFET is investigated as it is known to be strongly affected by thermal cycling [3]. This means that the stress profile on the solder joint, which in this case only consists of thermomechanical stress due to the coefficient of thermal expansion (CTE) mismatch, becomes of interest. This profile is obtained by using an electro-thermal circuit simulation in PLECS that translates a mission profile (i.e., the irradiance and ambient

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temperature profiles for the converter system) to the temperature profile of the MOSFET. It should be noted that a steady state look-up table, which eliminates any transients, is used to drastically lower the computation time. A finite element MOSFET model in COMSOL is then used to further translate the temperature profile to a local solder joint stress profile. Lastly, the remaining useful lifetime (RUL) of the solder joint is calculated by using the cumulative damage model in COMSOL which is based on the solder material's stress-cycle (S-N) curve.

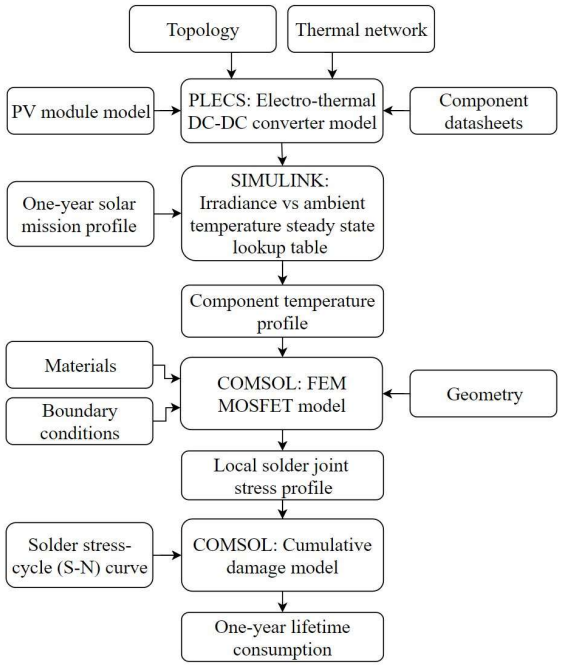

Fig. 1. Flowchart of the framework structure

3. Electro-thermal model

3.1 Electrical model

Isolated and non-isolated high step-up converters can be used in (BI)PV applications. Reviews on non-isolated topologies can be found in [4, 5]. In previous work, a cascade of an interleaved boost converter and an isolated full bridge converter using wide-bandgap (WBG) components was proposed and experimentally tested [6, 7, 8]. However, the overall efficiency was considered too low and the component temperature increase too high. In this work another topology is studied, being an isolated interleaved boost converter, as depicted in Fig. 2. This topology is a current-fed converter that was derived via the duality principle from a voltage-fed half bridge [9]. The converter was successfully applied for PV applications in [10] where it was operated in discontinuous conduction mode. In this work, the converter is operated in continuous conduction mode and the gain is given by Eq. 1.

$$G = \frac{V_{out}}{V_{in}} = \frac{2n}{1-\delta} \tag{1}$$

With n being the transformer turns ratio and δ being the duty cycle. According to Eq. 1, it can be noticed that the normal boost gain is multiplied by the transformer turns ratio, which allows to achieve high step-up conversion ratios. The factor 2 is a consequence of the voltage doubler rectifier that is being used in the output. Another advantage is that the gate signals of the switches are phase-shifted by half the switching period T_s, leading to an effective ripple current reduction in the input. The main disadvantage of this converter is that two inductors and a transformer are used, making it rather bulky compared to, for example, switched capacitor or flying capacitor boost converters [11, 12]. An overview of the used components for evaluating the converter is given in Table 1.

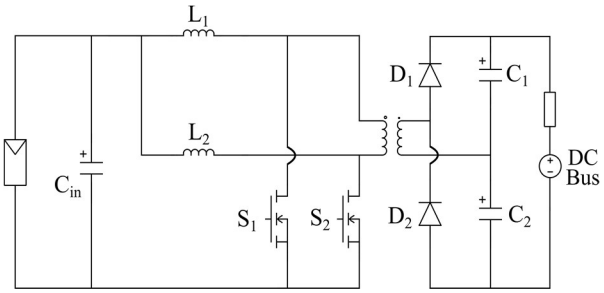

Fig. 2. Topology of an isolated interleaved boost converter

Table 1
Overview of the components used in the interleaved isolated boost converter

Component	Type	Value
Input capacitor C_{in}	KEMET C475M1R2C7186	100 V 5 x 4.7 µF
Switches S_1, S_2	TOSHIBA TPH3R70APL	100 V R_{on} = 3.1 mΩ
Inductors L_1, L_2	BOURNS SRP2313AA-470M	14 A 47 µH
Diodes D_1, D_2	ST STTH12R06	600 V V_f = 1.4 V
Output capacitor C_1, C_2	EPCOS B32672P5105K000	520 V 4 x 1 µF

A PV module of KC200GT from Kyocera Solar is adopted as the input. It is based on the single-diode model, includes temperature-dependent behaviour and has been fully described in [13]. As mentioned before, this input can be interchanged by more advanced PV module models that can include the effect of shading etc. [14]. An internal current control loop was designed with a proportional gain K_p of 0.015 and an integral gain K_i of 102.2. The reference for the PI current controller comes from an MPPT Perturb and observe (P&O) algorithm that runs at a frequency of 300 Hz.

3.2 Thermal model

The thermal model is based on several assumptions regarding geometry, boundary conditions for temperature and heat transfer [15, 16]. Firstly, the converter is soldered on a printed circuit board (PCB) consisting of FR-4 material with the following dimensions: 150 x 100 x 1.6 mm. This PCB is mounted in a 3 mm thick plexiglass box of 150 x 100 x 30 mm. Every component exchanges heat through the thermal vias of the PCB (conductive) [17] and through the internal air (convective). Moreover, it is assumed that both mediums have a uniform temperature throughout their respective volumes. A lumped thermal network, shown in Fig. 3, that excludes thermal capacitances is used in order to eliminate transients and acquire the steady state with minimal computation time.

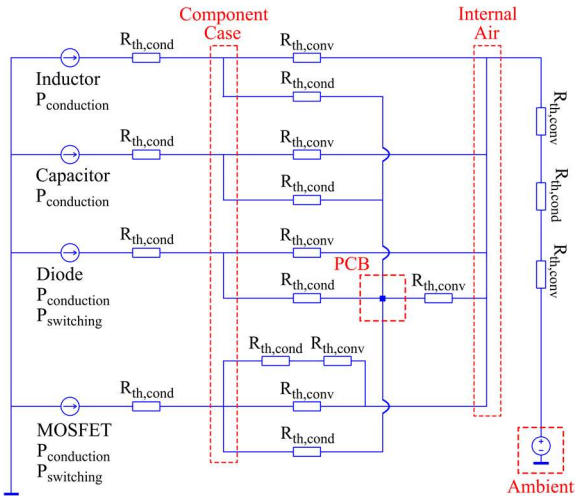

Fig. 3. Lumped thermal network for every component type used in the interleaved boost converter

The conductive thermal resistance $R_{th,cond}$ is either calculated by using the thermal conductivity of the material or extracted from the component datasheet. The convective thermal resistance $R_{th,conv}$ is calculated using the heat transfer coefficient of still air which has been over dimensioned from the generally accepted value of 10 W/m^{2}K to 11 W/m^{2}K to include radiative heat transfer effects [17]. Notably, the temperature-dependent behaviour of these values is not currently integrated into the model. Table 2 displays the respective thermal resistances calculated or extracted from the datasheet for every component's conductive and convective path as well as for the PCB and the housing.

Table 2
Thermal resistances for the heat transfer of the converter's components, PCB and housing calculated (c) from material parameters or extracted (e) from the respective datasheets

Thermal resistance	Value	Unit
MOSFET Junction to Case (e)	0.88	K/W
MOSFET Case to Internal Air (e)	49	K/W
MOSFET Case to Heat Sink (c)	1	K/W
MOSFET Heat Sink to Internal Air (e)	4	K/W
Rectifier Junction to Case (e)	1.7	K/W
Rectifier Case to Internal Air (c)	259	K/W
Inductor Core to Case (c)	1.2	K/W
Inductor Case to Internal Air (c)	56	K/W
Capacitor Hotspot to Case (c)	3.3	K/W
Capacitor Case to Internal Air (c)	254	K/W
Component to PCB (16 Vias) (c)	16.3	K/W
PCB to Internal Air (c)	3.3	K/W
Internal Air to Housing (c)	2	K/W
Housing to Ambient (c)	2.4	K/W

The heat exchanged in the thermal network is mainly generated by the conduction losses in the parasitic resistances of the converter's components. These include the inductor's DC resistance (DCR), the capacitor's equivalent series resistance (ESR), the rectifier's on-resistance (R_{on}) and the MOSFET's drain-source on-resistance ($R_{(ds)on}$). The latter two also generate heat in the form of switching losses which have been calculated using [18, 19] with the rise and fall times, t_{rise} and t_{fall}, of the MOSFET and the reverse recovery charge Q_{rr} of the rectifier.

3.3 Electro-thermal coupling

As discussed previously, the heat from the converter is generated by the electrical losses of its components from either switching or conduction through their parasitic resistances. These on-state resistances have, for the switching devices, the functionality in PLECS of becoming temperature-

dependent in the thermal domain. This means that their values will change according to the corresponding component's junction temperature. However, this functionality currently works only in one direction meaning that the electrical behaviour remains unaffected when a component's temperature changes. This can be implemented manually in PLECS by using a thermal feedback loop as shown in Fig. 4. The component's temperature is measured and sent into a 1D lookup table that contains its parasitic resistance's temperature-dependent behaviour. The resistance value is then interpolated or extrapolated and sent towards a variable series resistor. These feedback loops have been used for the conduction losses of every component and are evaluated for every switching period. The converter's capacitances and inductances can also be made temperature-dependent using the same methodology but a sensitivity analysis needs to be performed first to estimate their impact on the converter's performance and the model's computation time.

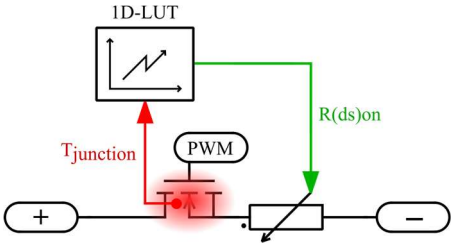

Fig. 4. Thermal feedback loop for a MOSFET's on-resistance in PLECS.

4. Steady state DC-DC converter lookup table

The electro-thermal model is then used to generate a lookup table in Simulink containing various component temperatures, voltages, currents and losses which can serve as boundary conditions in (sub)component degradation models. This lookup table approach allows the computation time to be reduced when converting a long-term mission profile to a stress profile but disables the implementation of parameter degradation.

A one-year mission profile from Denmark and Arizona as shown in Fig. 5a and in Fig. 5b respectively with a sampling rate of 5-min/sample is used as the input for this reliability assessment. It is then translated to the temperature of the converter's PCB, internal air and MOSFET case temperature, of which the latter is shown for both mission profiles in Fig. 5c and Fig. 5d respectively. The three temperature profiles will then form the boundary conditions of the finite element MOSFET model.

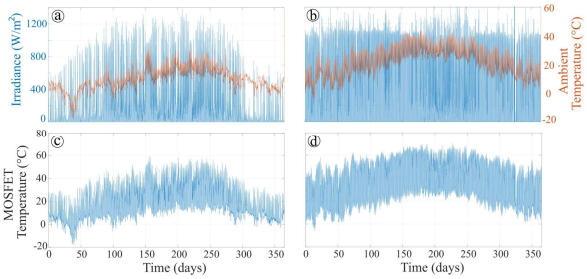

Fig. 5. Loading of the converter: one-year mission profile of (a) Denmark and (b) Arizona and the MOSFET case temperature of (c) Denmark and (d) Arizona.

5. Finite elements MOSFET solder joint model

5.1 Model structure

The finite element COMSOL model of the MOSFET, which is based on a commercially available device, is shown in Fig. 6. As mentioned previously, the MOSFET is placed on a 1.6-mm thick PCB consisting of FR-4 material and 16 copper thermal vias with a parasitic air layer in-between. The case is made of an epoxy resin with the bottom part consisting of a copper conduction pad. The leads are made of aluminium and are soldered to the PCB copper conduction paths with 60Sn-40Pb solder material. As seen in Fig. 6, only one-fourth of the MOSFET is modelled, as two symmetry planes are introduced to reduce the computation time.

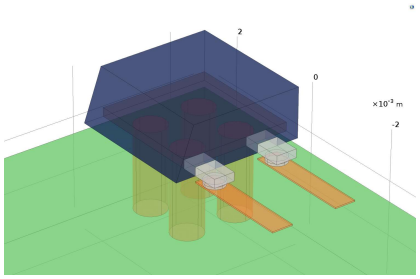

Fig. 6. Finite element MOSFET model in COMSOL.

The resultant thermal profiles are used to simulate the effect of the converter's housing and the surrounding components on the solder joint. Every connecting surface in the model is transferring heat conductively while every open surface of the model can transfer heat both convectively and radiatively. It was decided not to model the MOSFET's silicon die and bond wires, as the thermal resistance to the case was already available from its datasheet and used in the electro-thermal model. The silicon die can alternatively be modelled as a heat source consisting of the MOSFET's losses, but this will add more complexity to the model and consequently increase the computation time.

5.2 Fatigue modelling

A local stress profile is acquired after performing a time-dependent study of the model consisting of the combined influence of the temperature profiles of the internal air, the PCB and the MOSFET's case on the thermal expansion of the solder joint. This profile will used as an input for a fatigue study which will calculate the total damage caused on the solder joint by the one-year mission profile. This study applies COMSOL's fatigue module which includes several damage models. For mission profiles consisting of cycles with different amplitudes and mean values, the cumulative damage tool is often used [20]. This tool uses rainflow counting [21] to count the total amount of stress cycles that occur on the solder joint during the one-year mission profile with their respective amplitudes, mean values and durations. Afterwards, the solder joint's S-N curve, which represents the relation of a certain stress cycle amplitude with the number of cycles to failure, is extracted [22] and used to calculate the damage per cycle. This damage is then accumulated following the Palmgren-Miner rule [23] resulting in a number between 0 and 1 representing the amount of lifetime consumed during the one-year profiles.

5.3 Results

As seen in Fig. 7, the amount of lifetime consumed by the one-year profiles on the solder joint is displayed. A maximum lifetime consumption surface value of 11% in Fig. 7a and 23% in Fig. 7b is observed. These values translate to a remaining useful lifetime of 9.1 and 4.3 years for the mission profiles of Denmark and Arizona respectively. It should be noted that the stress created due to the CTE mismatch in the solder material is dependent on the geometry incorporated in the model. Discrete jumps in geometry can lead to overestimations of the local principal stress which in turn will affect the S-N curve's input. The final step of the methodology is therefore very dependent on the combination of the chosen S-N curve, which is geometry-dependent, and the dimensions of the solder joint model. The latter is not always provided which can lead to unrepresentative lifetimes. In future work, a more accurate result can be acquired by optimizing the mesh and the geometry of the solder joint to more closely resemble the practical S-N curve. This however will also significantly increase the computation time of the model. Alternatively, an S-N curve can be experimentally measured for a certain type and size of solder joint but this can become very time consuming. More methods to translate the local stress profile to the amount of lifetime consumed need to also be explored in the future in order to acquire a more accurate and representative result.

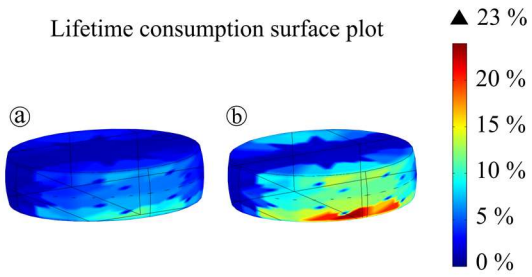

Fig. 7. One-year lifetime consumption surface plot of a 60Sn-40Pb solder joint from a MOSFET in a) Denmark and b) Arizona

6. Conclusion

The methodology of our reliability framework has been demonstrated on an isolated interleaved boost converter designed for BIPV applications. An electro-thermal model in PLECS and a finite element fatigue model in COMSOL were used to investigate the influence of two one-year mission profiles on the degradation of the MOSFET's solder joint. The resulting lifetimes were 9.1 and 4.3 years for the mission profiles of Denmark and Arizona respectively. However, the calculated lifetime is dependent on the combination of the chosen S-N curve and the geometry of the modelled solder joint. Alternative methods to translate the local stress profile of the solder joint to the consumed lifetime should be explored further to acquire a more representative result. Future work will include the implementation of electrical parameter degradation in the electro-thermal model and more accurate finite element models of different failure mechanisms and other components in order to better analyse the overall reliability of the DC-DC converter.

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