Verilog-A model of ferroelectric memristors dedicated to neuromorphic design

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***Abstract*— Artificial neural networks (ANN) are well known for performing Recognition, Data mining and Synthesis (RMS) tasks. However, the most famous ANNs are software implemented on computers that never take into account the power consumption management. Chip designers are aiming at low-power consumption by developing the neuromorphic engineering field. The goal is to design and produce neural-inspired architectures allowing energy-efficient computation systems. One decade ago, neuromorphic engineering had a renewal of interest, in particular due to the unveiled memristive devices. Indeed, memristors own all the features necessary in order to play the role of plastic synapses in ANNs. Among all memristive technologies, ferroelectric devices present an important advantage for low power systems: their high resistance which implies low current. In this paper, we will present a Verilog-A model of ferroelectric memristors. This model is based on measurements and therefore takes into account the variability of devices in terms of R_{ON}, R_{OFF} and switching characteristics. This realistic model will be helpful for designing neuromorphic systems based on these devices. Finally, we will present some Cadence simulations of learning in small neural networks composed of CMOS neurons and memristive synapses.**

Keywords—Verilog-A model, ferroelectric memristor, neuromorphic, spiking neural network.

I. INTRODUCTION

Since the publication of the "missing memristor found" in 2008 [1], the interest for memristive devices has strongly increased. This nanodevice is a non-volatile and non-linear resistor. The implementation of this nanocomponent for digital memory is now in the industrial phase [2]. However, it is even possible to vary the resistance of the device quasi-continuously. Many researchers investigate the analog feature of this technology to create memristive synapses for hardware neural networks [3]-[5].

Hardware neural network computation, also called neuromorphic engineering, is based on neuroscience principles such as the generation of spikes for the output neuron. Thus, the computation takes into account timing and allows the implementation of local learning rules without supervision. The most famous one is spike timing dependent plasticity (STDP) [6]. A causal link between the pre-neuron spike and the post-neuron one will increase the synaptic weight, whereas non-causality will decrease it. When using the technique of overlapping spikes, their shapes critically influence the STDP rule [7] and will thus determine the efficiency of the neural network for a dedicated task.

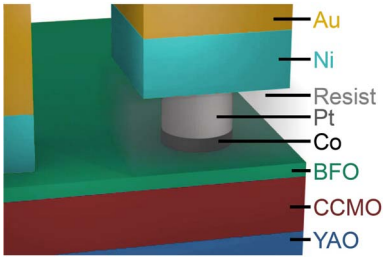

Figure 1: 3D representation of a ferroelectric tunnel junction. The junction stack, $Co/BiFeO_3/Ca_{0.96}Ce_{0.04}MnO_3$, is grown on $YAlO_3$ substrate. The junction is patterned by ebeam lithography (300, 400 and 500 nm in diameter) and the electrical contacts are patterned using standard optical lithography.

Hardware Spiking Neural Networks (SNNs) with an architecture composed of analog circuitry coupled with the aforementioned memristors open the possibility to build high-performance accelerators capable of tackling large computational tasks. Hardware implementation of memristive devices is time consuming. To avoid wrong implementations, hardware designers should investigate architectures of SNNs by simulations. Those simulations have to take into account the dispersion of their physical properties. The design of silicon neurons is facilitated thanks to efficient transistor models provided by integrated circuit founders. However, efficient models of memristor included in electronic design automation (EDA) software are not sufficiently spread.

Modelling memristive devices relies on the understanding of the physics of the nanocomponents. Memristive effects are present in different technologies. Thus, one model of memristor is dedicated to one kind of physics. In this paper, we focus on the "ferroelectric memristor" [8] shown in Fig. 1. The advantage of this memristive technology is that it is based on a purely electronic effect promising high speed and reliability. Moreover, the resistances of ferroelectric memristors are high (between 500 kΩ and 100 MΩ) and their switching voltages are around |1 V|. This component has the required features to be used with CMOS technologies.

The purpose of this paper is to present a ferroelectric memristor model based on measurements allowing to take into account device disparities and switching variabilities.

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Moreover this model is implemented in Verilog-A language, allowing simulations with usual EDA software. The ferroelectric memristor will be presented in Section II. The model will be described and compared to measurements in Section III. In Section IV, we will present the Verilog-A code allowing a free use of our work. Finally, we will use this model during a training of a small neural network.

II. Ferroelectric Memristors

The ferroelectric memristors has been patented in 2010 [9] and described in detail in [8]. We have used this component in previous neuromorphic projects as plastic synapse, i.e. a synapse allowing learning behavior.

A. Physics principle

The ferroelectric memristor is a tunnel junction with an ultrathin ferroelectric barrier. In this system, the resistance (or the current) strongly depends on the direction and the amplitude of the ferroelectric polarization of the barrier. This effect, called Tunnel Electro-Resistance, is a purely electronic phenomenon. To obtain the quasi-continuous analog resistance variation characteristic of a memristor, the ultrathin ferroelectric barrier will be chosen so that its polarization vs. electric field cycle is tilted. The ferroelectric memristor is therefore an "electronic type" Resistive RAM. Since it is not based on defect-mediated physical effects, it should also avoid reliability issues.

B. Memristor as plastic synapse

As shown in Fig. 2, we have demonstrated that the ferroelectric memristor allows the implementation of a learning rule called spike timing dependent plasticity [10]. This bio-inspired learning scheme is at the heart of unsupervised learning processes in SNNs. This important result demonstrates that the ferroelectric memristor is an excellent building block for developing neuromorphic electronics based on memristive synapses. Spike-Timing dependent plasticity has been demonstrated for different type of memristors [4]-[5] but the ferroelectric memristor is advantageous because of its speed (applied pulse duration of ~100 ns), large ON/OFF ratios, retention and cyclability [11].

III. Model

We have already proposed a physics-based model in [10]. However, this model did not take into account the behavioral variabilities. In this paper, we refine this model allowing use by neuromorphic designers. Thus, we introduce the ferroelectric memristor variability by behavior modeling. Variabilities could be characterized by 3 parameters: i) R_{ON} the minimum resistance value, ii) R_{OFF} the maximum resistance value and iii) the switching variability of resistance value.

A. R_{ON}: minimal value of resistance

The typical low resistance value of a ferroelectric memristor is around 250 kΩ. However, this value is different for each device. The distribution does not follow a Gaussian law. We empirically reproduce this distribution by two Gaussians sampled by a uniform distribution. This model will

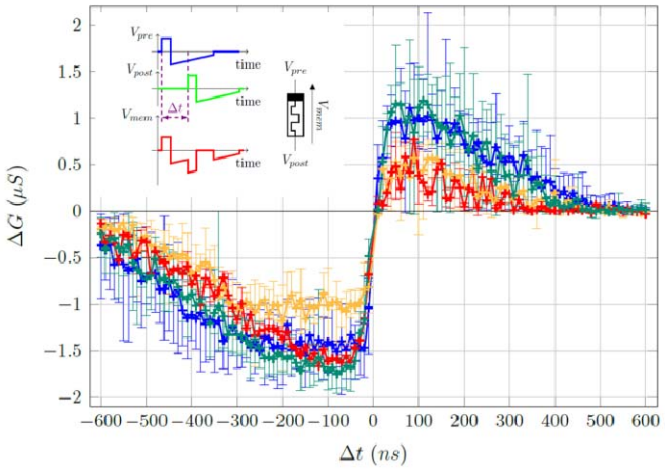

Figure 2: Spike timing dependent plasticity for four different BiFeO3 ferroelectric memristors (blue, green, orange and red lines), using the special waveforms for neural pulses developed by authors shown in inset. Bar graphs represent different set of measurements done for each memristive devices.

be used under Cadence environment. Neuromorphic designers will use Monte Carlo simulations to check their design. Thus, to make sure one has different parameters for each memristive device, we insert a *seed* parameter that represents the randomized R_{ON} of the device. The seed parameter will be detailed in Section IV. The implementation of this distribution in Verilog-A is as follows:

```
test = 0;
while (test = = 0)
    begin
        rnd= $rdist_uniform(seed,0,1);
        if (rnd<0.65)
            xrnd= $rdist_normal(seed,4.1,1.7);
        else
            xrnd= $rdist_normal(seed,7.77,2);
        Ron=89.126e3*exp(abs(xrnd)*ln(1.25));
        if ( ((xrnd<0)||(xrnd>12)) )
            test = 0;
        else
            test = 1;
    end
```

We draw the same number of trials as the 3,388 measurements. The comparison of both, Fig. 3-A, allows to validate our model for R_{ON}.

B. R_{OFF}: maximal value of resistance

The high resistance value follows the same kind of distribution. The Verilog-A code of its implementation is given below. Fig. 3-B shows the comparison to 33,800 measurements of R_{OFF}. The similar distributions allow us to validate the parameters.

```
test = 0;
while (test = = 0)
    begin
        rnd = $rdist_uniform(seed,0,1);
        if (rnd < 0.6)
```

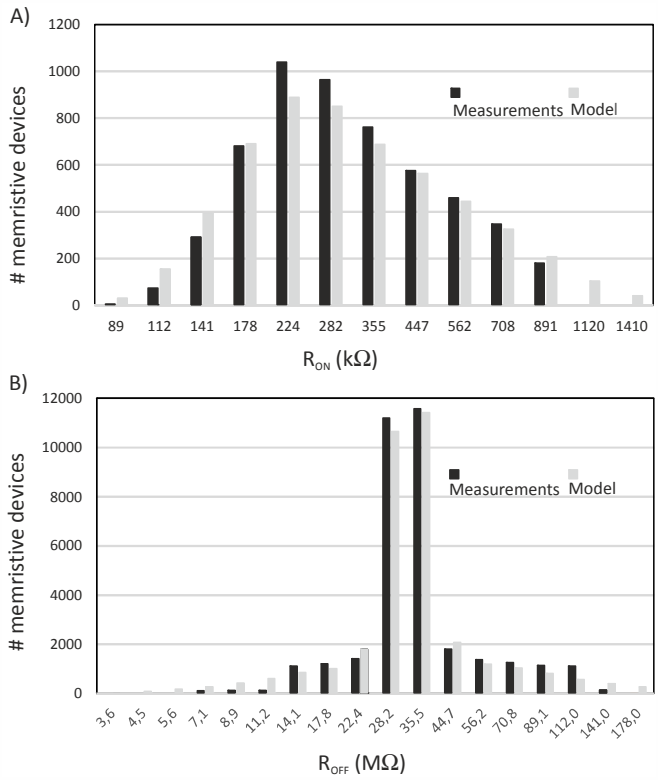

Figure 3: The resistance value on X-abs is the lower resistance value of the bin. A) Comparison of 3,388 measured R_{ON} with the same number of draws. B) Comparison of 33,800 measured R_{OFF} with the same number of draws.

```
        xrnd= $rdist_normal(seed,9.83,0.55);
    else
        xrnd= $rdist_normal(seed,10.2,4);
    Roff = 3.55e6*exp(abs(xrnd)*ln(1.259));
    if ((xrnd < 0) || (xrnd > 17))
        test = 0;
    else
        test = 1;
end
```

C. Switching variabilities

Fig. 2 shows a non-symmetrical behavior for the resistance increase and decrease. To model these different behaviors we have introduce a fictional R_{ON} that is the minimal value targeted. This fictional value called R_{ON_fict} is defined for each step down as long as the memristance value R_{MEM} is higher than 2 MΩ. R_{ON_fict} is always higher than R_{ON}. The corresponding code is:

```
Ron_fict = 0;
if (Rmem < 2e6)
    Ron_fict = Ron;
while (Ron_fict < Ron)
    Ron_fict = Ron*(1+Rmem/12e6) + (Rmem/45)*$rdist_
      normal(seed,0,1);
```

The update of R_{MEM} is computed at each time step. R_{MEM} is a combination of two parameters z1 and gamma. In this section we present the parameters to compute z1 and gamma depending on the voltage Vr applied to the memristor. The resistance increases when Vr is positive and decreases when it is negative.

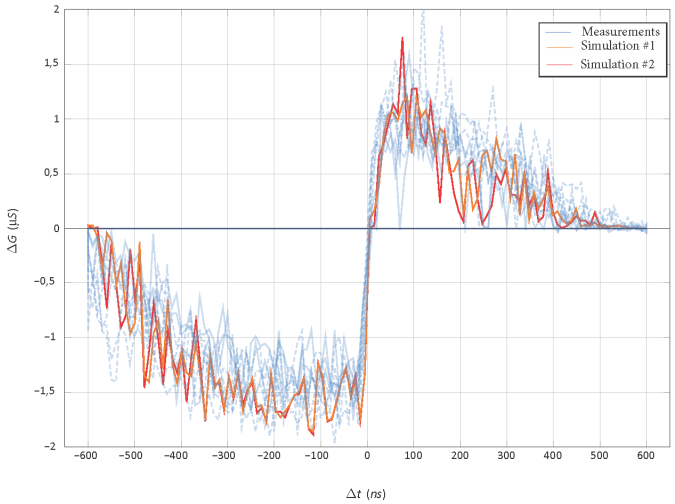

Figure 4: Comparison of STDP between measurements from Fig. 2 and simulations. We realized two simulations with two different seed values. The inset in Fig. 2 shows a negative result of Vr while Δt > 0. Vr negative implies the decreases of Rmem and thus the increase of the conductance as shown here.

```
if (Vr > 0)     // Rmem increases
    begin
        z1 = -27.55*pow(Vr,3) + 109.8*pow(Vr,2) - 151.75*Vr
          + 64.5 + 1.548*$rdist_normal(seed,0,1)*para_noise;
        gamma = 7.75*exp(-1.825*Vr);
    end
else          // Rmem decreases
    begin
        z1 = 123.397*pow(Vr,5) + 854.531*pow(Vr,4) +
          2357.19*pow(Vr,3) + 3242.05*pow(Vr,2) +
          2227.74*Vr + 609 +
          3.5e-6*pow($rdist_normal(seed,0,1),1)*para_noise;
        gamma = 0.0021*exp(0.74*Vr)-0.42e-3;
    end
```

IV. Verilog-A code

Monte-Carlo simulations under Cadence environment generate a randomized real number called mc_seed. To use it as an integer and avoid the null value, we implement the lines below at the beginning of the code:

```
(*cds_inherited_parameter*) parameter real mc_seed = 0;
localparam integer RANDNUM = (1+mc_seed)*1000000;
seed = RANDNUM;
```

The last computation is dedicated to the Rmem value. This memristance value is the result of ferroelectric domain changes as described in [11]. The implementation gives us:

```
if (Vr < 0)
    S = 1-1/PI*(PI/2-atan((z1-z0)/gamma));
else
    S = 1/PI*(PI/2-atan((z1-z0)/gamma));
Rmem = 1/( S*( 1/Roff-1/Ron_fict ) + 1/Ron_fict);
```

with z0 being the cumulated time as a result of consecutive applied pulses.

The whole Verilog-A code has been used to reproduce the STDP behavior. In Fig. 4, we compare two trials with two different seeds with the measurements from Fig. 2. The reproducibility and the global behavior allow us to validate this code for neuromorphic design under Cadence environment.

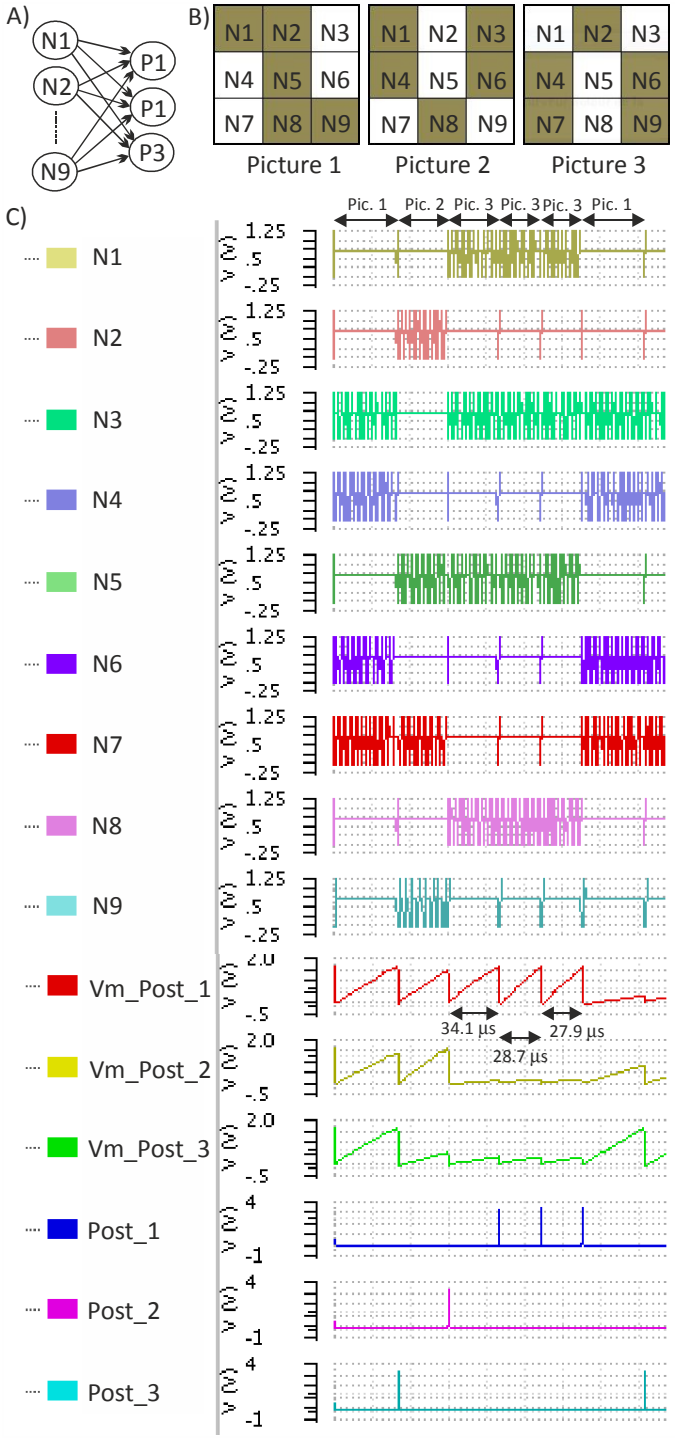

Figure 5: A) All-to-all connected network composed of 9 presynaptic neurons (N1-N9) and 3 postsynaptic neurons (P1-P3). B) 3 different pictures applied to input neurons (N1-N9). White and dark colors are coded by a spike frequency of 255 kHz and 0 Hz respectively. C) Vm_post_X are the membrane voltage of the postsynaptic neurons (P1-P3); Post_X are the digital output of postsynaptic neurons; NX are the spikes encoding the color applied to the input neurons.

V. Simulations

We use this model for a Cadence simulation of a small neural network. The network is composed of 9 presynaptic and 3 postsynaptic neurons all-to-all connected (Fig. 5-A). We apply 3 different types of images (Fig. 5-B). White and dark colors are coded by a spike frequency of 255 kHz and 0 Hz, respectively. The memristive synapses are simulated using the Verilog-A model presented in this paper. The neurons are simulated using transistor level model.

Fig. 5-C shows the simulation results. We start with Picture 1, in which N3, N4, N6 and N7 are white and thus spike at 250 kHz. The membrane voltage Vm_Post_X of all postsynaptic neurons increases. In this case, Vm_Post_3 reaches its threshold value and thus spikes (see Post_3 signal). We then present Picture_2 and as a result Post_2 spikes. Then Picture_3 is presented three times and as a result Post_1 spikes every time. However, Post_1 spikes earlier at the second and third than at the first presentation of Picture 1. This shows that the network learnt this picture. The Verilog-A model is efficient for neural network simulations.

VI. Conclusion

Based on numerous measurements of ferroelectric memristors, we propose in this paper an open access Verilog-A model of this device. The model includes all behavioral variabilities: R_{ON}, R_{OFF} and switching characteristics. Those variabilities will be helpful for neuromorphic designers allowing full Monte-Carlo simulations. Our next work will be the design of presynaptic and postsynaptic analog neurons for a large neural network dedicated to visual data processing under the EU ULPEC project.

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