Low-Cost Fully Autonomous Piezoelectric Energy Harvesting Interface Circuit with up to 6.14x Power Capacity Gain

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***Abstract*—This paper presents a novel self-powered and fully autonomous interface circuit to extract piezoelectric energy from vibrations available in the environment for supplying DC voltage to electronic loads. A new energy extraction technique called Synchronized Switch Harvesting on Capacitor-Inductor (SSHCI) is utilized, which reduces system cost through a downsized inductor in the range of tens of µH's, while achieving as high voltage flipping efficiency as conventional SSHI circuits. Fabricated in 180 nm standard CMOS technology, the interface circuit has been tested on a MEMS piezoelectric energy harvester with 2 nF intrinsic capacitance in presence of vibrations at 415 Hz resonant frequency. SSHCI circuit provides 6.14x relative improvement over maximum output power of an ideal full-bridge rectifier (FBR) by utilizing a 68 µH inductor to charge a 453 nF storage capacitance. A maximum power conversion efficiency of 90.1% has been measured for SSHCI operation due to low power design techniques and optimized switching time for charge flipping.**

Keywords—Self-powered, autonomous, low-profile, piezoelectric energy harvester, IC, SSHCI, charge flipping time detection.

I. Introduction

Proliferation of wireless sensor networks (WNSs) in daily life applications evokes the problem of maintaining the power they need for proper operation. Since batteries do not shrink at the same rate as sensor electronics, their use results in bulky sensor systems [1]. Furthermore, in some embedded WSN applications, replacement of batteries is problematic. An alternative power supply for WSNs can be obtained by harvesting energy from environment.

Piezoelectric energy harvesters (PEHs) are highly popular vibration transducers due to their relatively high output voltage levels and ease of integration. As PEHs generate AC voltage, a rectification circuit is needed to maintain stable DC voltage required for proper operation of electronic loads. The well-known interface circuit for AC-DC conversion is the full-bridge rectifier, which is adversely affected by the small inherent capacitance of PEH [2]. Therefore, nonlinear energy extraction approaches have been developed to increase the extracted power from PEHs [3]–[7]. Energy investment [3] and Synchronous Electric Charge Extraction (SECE) [4]–[6] techniques can provide load independent operation; however, their performance regarding extracted power level is inferior compared to Synchronized-Switch Harvesting on Inductor (SSHI) technique [7]. Nevertheless, all of these methods require large external inductors to attain high levels of efficiency and power extraction gain. Large inductors increase overall system volume and cost. Inductorless designs presented in [8] and [9] utilize charge flipping capacitors instead of inductors to flip voltages, which reduces the system volume significantly. However, numerous switches required by such approaches curtail power conversion efficiency and extracted output power severely due to high switching losses. Moreover, interface circuits in [7]–[9] need external calibration of charge flipping time to obtain maximum output power for each PEH type and environmental conditions.

In this paper, a fully autonomous energy harvesting interface circuit is presented based on a new Synchronized Switch Harvesting on Capacitor-Inductor (SSHCI) technique to extract power from PEHs while utilizing a low-profile external inductor. In the following section, the operation of SSHCI is explained together with circuit design specifics. Measurement results from the fabricated chip are presented in Section III. Finally, Section IV concludes the paper.

II. Interface Circuit Design

SSHCI circuit depicted in Fig. 1(a) utilizes a low-profile external inductor, L_{EXT}, in the range of tens of µH's to achieve voltage flipping through LC resonance between this inductor, the PEH capacitance C_{PZ}, and external capacitance C_{EXT}. A series capacitor is employed to limit the maximum resonating current. This leads to two-step flipping process to successfully invert charge of C_{PZ}. SSHCI interface can achieve high power conversion efficiency and improved power capacity with low-profile external components. The design can charge the storage capacitance C_{STOR} from 0 V through a negative voltage converter (NVC) and an on-chip diode D_S. After the charge conduction to C_{STOR}, the remaining charge on C_{PZ} is flipped with the resonance circuit established by C_{PZ}, external capacitor C_{EXT}, and external inductor L_{EXT}. Unlike [7]–[9], optimum charge flipping instants are detected automatically using sensing comparators during charge flipping process. Utilizing conventional SSHI structure associated with capacitor-inductor flipping method, the circuit can deliver power conversion

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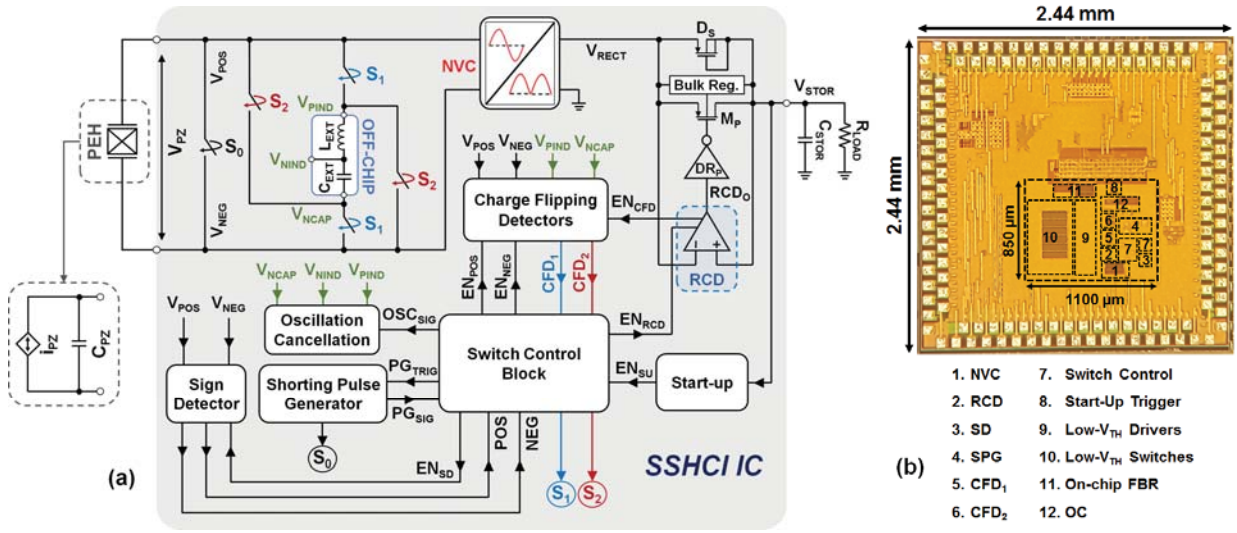

Fig. 1. (a) Synchronized Switch Harvesting on Capacitor-Inductor (SSHCI) interface circuit, and (b) die micrograph of the implemented SSHCI chip.

efficiency as high as 90.1% and 6.14x higher power than maximum output power of an ideal full-bridge rectifier (FBR).

A. Operation Phases

SSHCI circuit is composed of eight units as depicted in Fig. 1(a): Start-up trigger, NVC, reverse current detector (RCD), charge flipping detectors (CFDs), oscillation cancellation (OC), shorting pulse generator (SPG), sign detector (SD), and switch control block. Die micrograph of the SSHCI chip fabricated with 180 nm CMOS technology is shown in Fig. 1(b).

The enable trigger generated by the start-up unit indicates that there exists sufficient charge on C_{STOR} to maintain proper operation of the SSHCI circuit. The interface has five operational phases illustrated with the equivalent circuits established in Fig. 2. As the PEH output swings, some amount of electrical charge is accumulated on C_{PZ} due to the stress applied on the piezoelectric material (Phase I). The generated AC voltage is rectified through NVC. When the output of NVC, V_{RECT}, exceeds storage voltage V_{STOR}, RCD allows C_{STOR} to be charged through the swing of PEH (Phase II). Charging process continues until $V_{RECT} < V_{STOR}$ and then, RCD stops conduction by turning M_P OFF. In addition, RCD enables CFD and turns S_1 switches ON. During phase III, energy left on C_{PZ} is transferred to the external capacitance C_{EXT} through S_1 switches. C_{EXT} is chosen to be equal to C_{PZ} in order to achieve matched impedance for maximum power transfer. Considering the sign of piezoelectric voltage (V_{PZ}) detected with SD, CFD is activated to find the instant at which maximum amount of energy is transferred from C_{PZ} to C_{EXT}. Following the energy transfer from C_{PZ} to C_{EXT}, C_{PZ} is shorted in phase IV to discard the possible residual charge. The energy on C_{EXT} is transferred back to C_{PZ} in the reverse polarity by means of S_2 switches in phase V to complete the charge flipping process. CFD again monitors the moment that the maximum energy transfer from C_{EXT} to C_{PZ} is attained. Finally, system turns back to phase I in which all switches are OFF, and nodes V_{PIND}, V_{NIND}, and V_{NCAP} are shorted to ground to eliminate any residual charge on C_{EXT} and L_{EXT}, hence preventing oscillation. Measured waveforms of V_{PZ} reverse current detector output RCD_O, and inductor current i_{IND} during operation phases are shown in Fig. 3.

B. Negative Voltage Converter

Rectification of the AC voltage coming from PEH is conducted by NVC presented in Fig. 4(a). Two NMOS switches

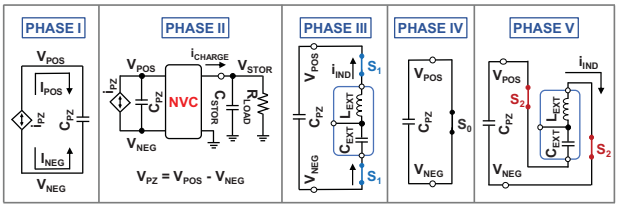

Fig. 2. Summary of the operation phases for proposed interface circuit.

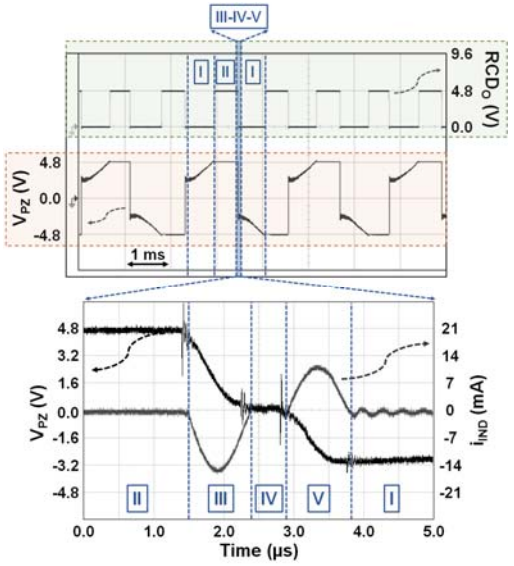

Fig. 3. Measured waveforms of piezoelectric voltage V_{PZ}, reverse current detector output RCD_O, and inductor current i_{IND} during operation phases.

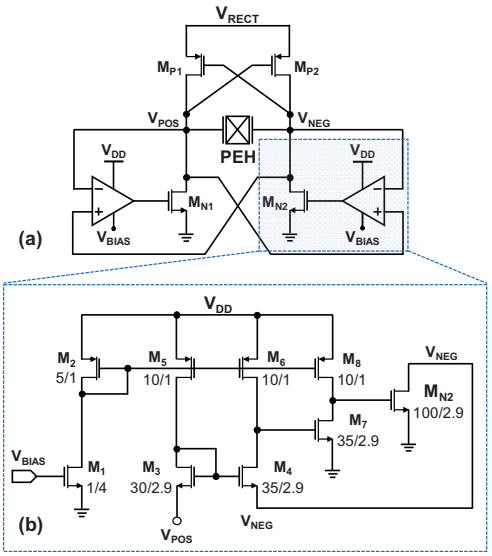

Fig. 4. (a) Implementation of negative voltage converter (NVC) and (b) the comparator utilized inside NVC circuit.

M_{N1} and M_{N2} are controlled by two comparators shown in Fig. 4(b). Comparators have current-follower input stages to monitor PEH terminal voltages V_{POS} and V_{NEG}. They decide which terminal is connected to ground for rectification purposes. Cross-coupled PMOS switches M_{P1} and M_{P2} driven by PEH terminals help governing the charge flow path to supply a positive voltage. Mismatching created by different aspect ratios of M_3 and M_4 provides a more stable operation by preventing oscillation during transitions.

C. Charge Flipping Detectors

Flipping time monitoring configurations for the autonomous flipping operations conducted by S_1 and S_2 switches are depicted in Fig. 5. In addition, Fig. 6 illustrates the details of the charge flipping detector circuits. For the detection of maximum energy transfer point from C_{PZ} to C_{EXT} in phase III, PMOS input pairs were used, since compared voltage levels are below half of the supply voltage level (V_{STOR}=V_{DD}), which better fits to common mode range of PMOS input pairs. Similarly, NMOS input pairs were utilized in phase V to find the maximum energy transfer instant from C_{EXT} back to C_{PZ}, as compared voltage levels are above the half of V_{STOR}. MOSFETs M_{11} in CFD_1 and M_{10} in CFD_2 are of low threshold type (V_{TH}≈300 mV). This extends the common mode voltage range, and increases the bandwidth. To avoid waste of power, both circuits are completely disabled during the phases they are not used.

III. Experimental Results

A custom-made MEMS PEH with C_{PZ}=2 nF was utilized to validate the performance of the interface. A 453 nF capacitor was utilized for C_{STOR}, and three different SMD inductors (68, 47, and 27 µH) were employed as L_{EXT} together with C_{EXT}=C_{PZ}. Fig. 7 depicts the measured waveforms of V_{PZ}, V_{RECT}, V_{STOR}, and overall enable signal for charging from V_{STOR}=0 V after start-up. RCD operation is initiated before the overall enabling signal to speed up the start-up operation. Charging of V_{STOR} with aforementioned SSHCI operation phases through optimum

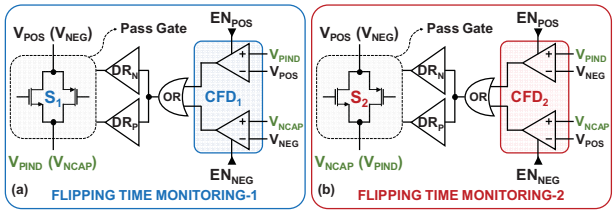

Fig. 5. Flipping time monitoring configurations established for (a) S_1 and (b) S_2 switching operations.

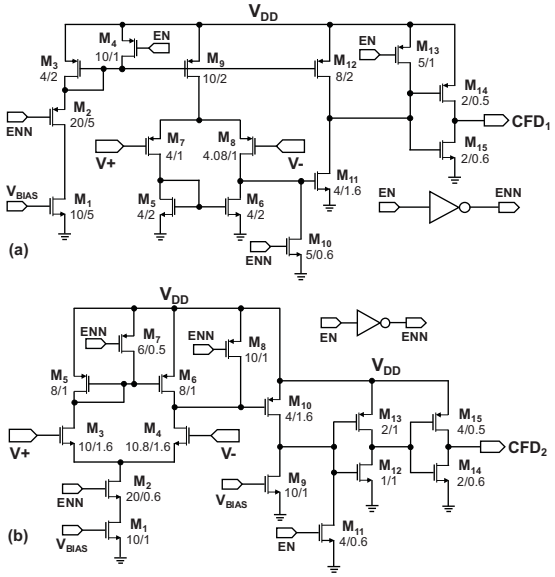

Fig. 6. Schematics of (a) charge flipping detector-1 (CFD_1) and (b) charge flipping detector-2 (CFD_2).

charge flipping detection is also illustrated in the Fig. 7. Fig. 8 shows measured output power of SSHCI circuit for different piezoelectric open circuit voltage ($V_{PZ,OC}$) amplitudes. During these measurements, the shaker table was excited with 415 Hz which is the resonant frequency of the MEMS PEH. SSHCI is able to provide 6.14x relative performance improvement over maximum output power of an ideal FBR for $V_{PZ,OC}$=0.95 V. For larger $V_{PZ,OC}$ levels, relative performance improvement reduces due to larger damping and lower displacements of the transducer. Measured power conversion efficiency (η=P_{OUT}/P_{IN}) for different L_{EXT} values given in Fig. 8(d) reveals that the circuit achieves around 90.1% conversion efficiency for L_{EXT}=68 µH, which is higher than the efficiency reported by previous designs with large inductors [2]–[7]. Table I provides comparison of the SSHCI test chip performance against the state of the art. Although flipping capacitor rectifier (FCR) in [8] provides an inductorless design, its figure of merit (FOM), which is defined as FOM=P_{OUT}/$f_{EX}V_{PZ,OC}^2C_{PZ}$, and power conversion efficiency are inferior to SSHCI. Besides, compared to the literature, SSHCI circuit, which has a fully autonomous charge flipping time detection, can achieve higher efficiency and FOM by utilizing low-profile inductors.

IV. Conclusion

A low-profile fully autonomous interface circuit has been presented in this paper. A new SSHCI technique with automatic

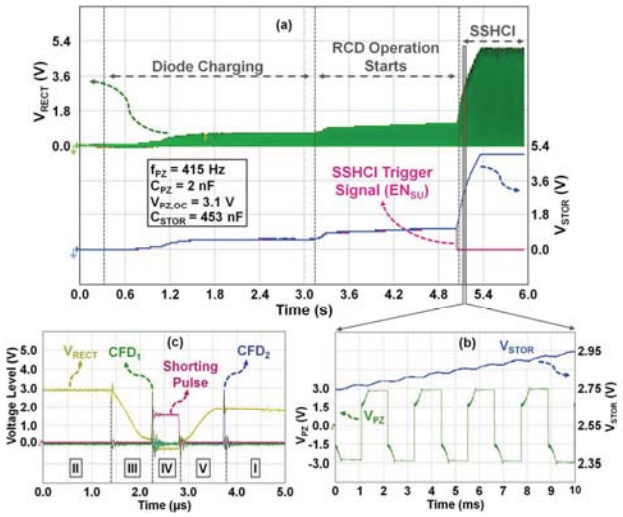

Fig. 7: Measured waveforms of SSHCI circuit illustrating (a) start-up, (b) charging, and (c) control signals generated during voltage flip operations.

charge flipping detection has been introduced to attain high power conversion efficiency and output power by utilizing inductors in the range of tens of µH's. The fabricated IC yields a maximum of 6.14x relative performance improvement over maximum output power of an ideal FBR, and 90.1% power conversion efficiency. SSHCI circuit supplies energy to microelectronic devices while downsizing the volume (cost) of the external components compared to alternatives.

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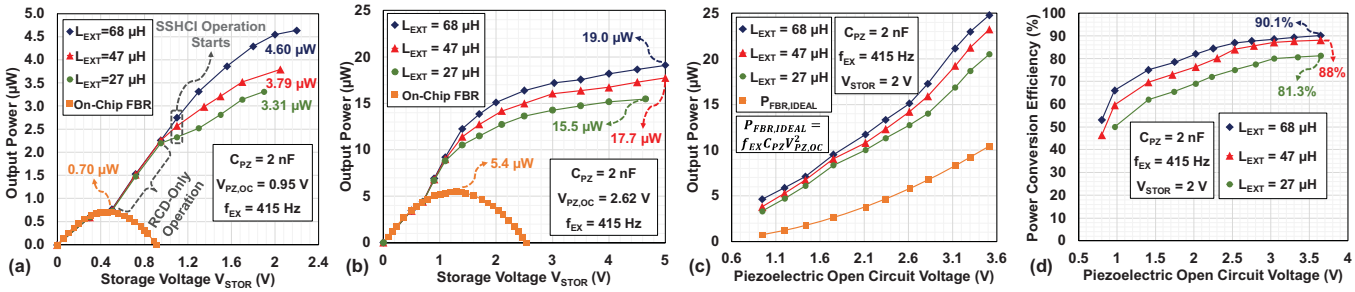

Fig. 8: (a, b) Measured output power by SSHCI circuit compared to on-chip full-bridge rectifier (FBR) with different piezoelectric open circuit voltage levels $V_{PZ,OC}$, and (c) ideal FBR, and (d) power conversion efficiency of the operation.

TABLE I
COMPARISON OF THE IMPLEMENTED IC WITH STATE OF THE ART

Ref.	Tech.	Scheme Type	C_{PZ}	Excitation Frequency	Inductor (Volume)	Flipping Time Detection	Cold Start-up	Peak Conversion Efficiency	Power Extraction Improvement (FOM[1]x100)	Chip Size
[2]	350 nm	SSHI	12 nF	225 Hz	820-22 µH (NA)	External Adjustment	NO	85[2]% (47 µH) 87[2]% (22µH)	420[5]% (820 µH) 257[5]% (22 µH)	4.25 mm^2
[3]	350 nm	Energy Investment	15 nF	143 Hz	330 µH (126 mm^3)	NA	NO	69.2%	360%	2.34 mm^2
[6]	320 nm	SECE	52 nF	60 Hz	10 mH (NA)	NA	YES	85.3[3]%	351%	0.95 mm^2
[7]	350 nm	SSHI	26 nF	225 Hz	3.3 mH (20.14 cm^3)	External Adjustment	YES	88[4]%	440%	0.72 mm^2
[8]	180 nm	FCR	80 pF	110 kHz	NO	External Adjustment	YES	NA	483[6]%	1.70 mm^2
This Work	**180 nm**	**SSHCI**	**2 nF**	**415 Hz**	**68-27 µH (18 mm^3)**	**Autonomous Adjustment**	**YES**	**90.1% (68 µH) 88% (47 µH) 81.3% (27 µH)**	**614% (68 µH) 506% (47 µH) 441% (27 µH)**	**0.94 mm^2**

(1) FOM = $P_{OUT}/f_{EX}V_{PZ,OC}^2C_{PZ}$
(2) It is only for DC-DC converter.
(3) External supply was used.
(4) Calculated from paper.
(5) Calculated with respect to off-chip FBR.
(6) Calculated with respect to on-chip FBR.