A Novel FIFO Design for Data transfer In Mixed Timing Systems

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Abstract : In the current scenario, with the increasing integration densities, most system-on-chip designs are partitioned into multiple clock domains .In this paper an asynchronous FIFO (First-in First-out pipeline) design is employed as a data transfer interface between two independent clock domains .Since the clocks on the either sides of the FIFO run at a different speed, the task to ensure the correct data transmission through this FIFO is manually performed. Firstly an existing asynchronous FIFO design is discussed and simulated. Gate-level simulation results depicted the flaw in existing design. In order to solve this problem, a novel modified asynchronous FIFO design is proposed. The results obtained from proposed design are in perfect accordance with theoretical expectations. The proposed asynchronous FIFO design outperforms the existing design in terms of accuracy and speed. In order to evaluate the performance of the FIFO designs presented in this paper, the circuits were implemented in 0.24µ TSMC CMOS technology and simulated at 2.5V using HSpice (© Avant ! Corporation).The layout design of the proposed FIFO is also presented.