High Efficiency Hetero-Junction: From Pilot Line To Industrial Production

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Abstract **— Combination of silicon heterojunction cell technology (SHJ) with bifacial module architecture is an appealing solution for manufactures who are focused on PV system performances. In this paper, we will present a study with an industrial perspective, initiated to address specific challenges of producing SHJ cells and modules in Europe. The impact of incoming wafer quality has been studied by analyzing at full ingot scale the efficiency performances of SHJ cells. The impact of long queue time prior to deposition is also reported. Finally, results of full size modules with 72 cells are presented.**

Index Terms — photovoltaic cells, silicon, amorphous materials, optimized production technology

I. INTRODUCTION

Silicon-based heterojunction solar cells (SHJ) are focusing the attention within crystalline silicon (c-Si) photovoltaic (PV) community as this technology allowed to reach an efficiency of 26% i.e. the highest value ever reported for a PV cell with a c-Si absorber without concentration [1].

A key point of SHJ is the passivation of highly recombination-active centers at the c-Si surface with hydrogen rich wide bandgap thin film such as hydrogenated amorphous silicon (a-Si:H). These films can be doped relatively easily, either n- or p-type, allowing both junction formation and contacts with record-low values for the saturation-current density that enables single junction open-circuit voltage as high as 750 mV [2]. SHJ technology is then very promising to enhance annual energy generation in PV fields owing to possibly high efficiency and bifaciality ratio, and low thermal coefficient.

In last years, the development of SHJ has been subject to extensive investigation in Europe with the implementation of few pilot lines [3-5]. Recently, actors that were previously focused on thin-films modules found in SHJ a way to convert their existing production capacity with limited CAPEX maintaining their position in the PV manufacturing [6-8].

Enel Green Power (EGP) is one of them, which has so far produced more than 6 million of thin film silicon PV modules in its subsidiary company 3SUN with an annual capacity of 200MWp/y. The pre-existing thin film silicon PV fab is being upgraded to manufacture high efficiency SHJ cells and modules. The new cell line will include incoming wafer sorter, wet bench for wafer texturization and cleaning, Plasma Enhanced Chemical Vapor Deposition (PECVD) reactor for a-Si:H layers deposition, Physical Vapor Deposition (PVD) reactor for Transparent Conductive Oxide (TCO) layer deposition and a screen-printing line for metallization.

Industries and research institutes collaboration should aim to not only achieve cell and module excellence in conversion efficiency but also to anticipate, face and solve, potential problems that can occur during the industrial production, leveraging the technical expertise of the research institute with the industrial experience of the manufacturer.

Well before the installation of the production lines, since more than two year, EGP has established a fruitful collaboration with CEA-INES to accelerate the development of SHJ cell and module technology. HETNA project (as both parties have defined this collaboration) has produced interesting results, part of that will be presented hereafter.

II. MATERIAL SELECTION AND PRE-PRODUCTION

Crystalline silicon material selection is crucial for SHJ manufacturing in order to limit production costs and assure high efficiencies. As this c-Si technology is all processed at low temperature (T<230°C), it is not possible to remove bulk c-Si impurities as performed for conventional homo-junction technologies using as-called “gettering” and cleaning [9-10]. For this reason, high quality Czochralski (Cz) wafers are used as substrates, which account for about 70 % of the cell production material costs. Efficiency record results are generally obtained after a severe selection of materials and wafer quality in particular. For this purpose, wafer manufacturers may ‘select’ R&D wafers that will not provide a full picture of the material that will be available in a production environment.

Detailed studies have been performed at CEA-INES pilot line to evaluate the impact of wafers properties on cell efficiencies and its parameters. Evaluations at the full ingot scale, for several suppliers has been performed showing that high oxygen content can lead to efficiency limitation in Cz ingot seed-end while metallic impurities may affect cells made with ingot tail-end wafers [10-11].

Such studies have been carried out on two ingots from a given supplier selected by 3SUN to cover a wide range of resistivity and lifetime. This aims to mimic as much as possible the type of material that will be used in real production environment.

Ingot A and B were declared by the supplier to have respectively resistivity in the range of 0.2 - 2 Ω.cm with lifetime higher than 500 µs (found to be > 2.4 ms) and 1 – 7 Ω.cm with lifetime >2 ms (found to be > 2.7ms). Groups of 100 wafers taken homogeneously along the two ingots were processed in CEA-INES pilot line in similar conditions to what will be in 3SUN production. A metallization design with 4 busbars was used for this study.

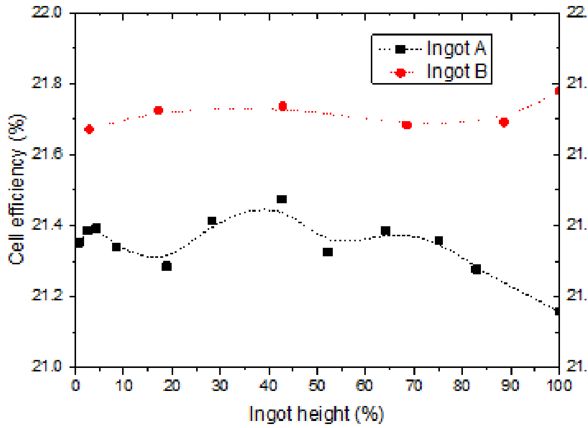

Fig. 1. SHJ cells efficiency over ingot height for two different silicon ingots material bulk properties. Each point is the average value over 100 cells.

On Fig. 1, we find that cells efficiencies are respectively equal to 21.3% and 21.7% and quite stable over all the height for both ingots A and B. In addition, we observe a clear step in the abs. efficiency of ~0.35% going from ingot A to B attributed to different bulk material properties. Further investigations are on going to identify the main bulk parameters to be considered for optimal material choice for the production line.

II. MANUFACTURING ASPECTS TOWARDS HIGH EFFICIENCY CELL LINE PRODUCTION

One important aspect is the effect of the waiting time (also referred as q-time) after wafer preparation and prior to a-Si:H deposition. Indeed, since the interfaces between c-Si and a-Si:H layers are the critical points of the junction, it is fundamental to limit surface damages and presence of impurities to ensure high device performance.

It is well known that HF last step removes the surface oxide layer and promotes a weak H_2 passivation. Unfortunately, Si-H bond is weak (298 kJ/mol) compared to Si-O bond (798 kJ/mol) so O_2 from atmosphere can easily replace H_2 creating a recombination site. In a manufacturing condition, the control of the q-time must be integrated in the material flow timing and the design of the automation system between different process steps must consider.

In our studies, we observed that lifetime measured on flat silicon just after the HF-last treatment has a clear and measurable decay with time. In Fig.2, we show typical lifetime decay of two different flat silicon samples measured at CEA-INES and 3SUN. From the picture, it is evident that modification of surface is happening after 20-30 min from the HF last and perfect stability is not completely reached after 60 min.

Considering the extremely reactive surface 3SUN SHJ line will limit the carrier transfer from wet bench to PECVD to a maximum of 20 min. In case this maximum q-time cannot be respected, for example due to unavailability of the PECVD, the carrier will be automatically redirected to a N_2 buffer to prevent air oxidation.

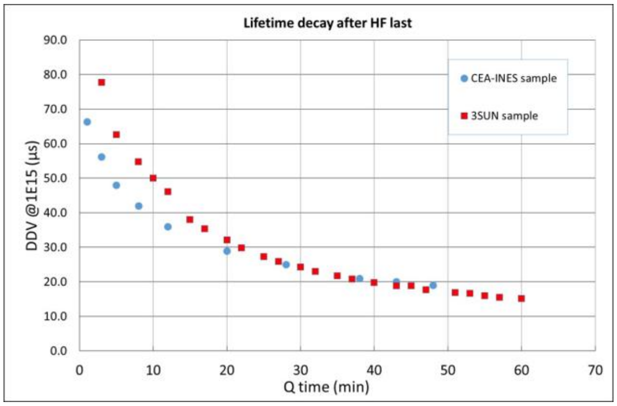

Fig. 2. Lifetime decay after HF last treatment measured on flat double side polished silicon.

Q-time between PECVD and PVD can degrade cell performances as well even if it less critical. Using CEA-INES pilot line we verified that air exposure up to 6 days under clean air environment do not affect the cell performance.

Automation and handling systems are also critical elements in the manufacturing line that can affect the cell efficiency of the fab. Pick-up, belt marks or rubbing of wafers during handling in the tray are interesting areas of investigation. For example, a specific study on the effect of cleanliness, samples transportation and PECVD tray design can be found in ref. [8]. In order to monitor surface condition after cleaning and deposition processes on line PL equipment will be used in 3SUN line. This will allow capturing early failures of the cells affecting the scrap rate and improving the fab efficiency.

On this topic, CEA-INES developed a method described in details in ref. [12] showing good correlation with Fill Factor (FF) losses and J_{02} when applied to SHJ devices.

III. CELLS AND MODULES EFFICIENCY

Full bifacial SHJ modules have been fabricated at CEA-INES to evaluate module efficiency and start with material selection for modules manufacturing aiming to: maximize the cell to module ratio, evaluate materials by extensive reliability testing and choose the best compromise between performances and costs [13].

Here below, we report on the best module results produced at CEA-INES with this design in 2017. The module picture and EL image are presented on

Fig. 3. No apparent defects (no crack, no dark spots) are visible. The IV parameters are given for the two sides of the module in Tab.I.

We underline that these measurements have been performed using a dark background (no illumination at the non-illuminated side) and thus do not take into account additional benefit from bifaciality. The peak power for the module have been determined at 380.7W respectively, with 4 busbars cells configuration. The GE20 method, considering bifaciality aspects, have been applied to this module and presented elsewhere [13].

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TABLE I
IV PARAMETERS OBTAINED FROM FLASH TEST MEASUREMENT OF 72 SHJ CELLS GLASS-GLASS MODULE PRODUCED IN 2017 WITH 22% CELLS AT CEA-INES.

Side	P_{max} (W_c)	V_{oc} (V)	I_{sc} (A)	FF (%)
Front side	380.7	53.4	9.15	77.9
Back side	331.5	53.3	7.95	78.2

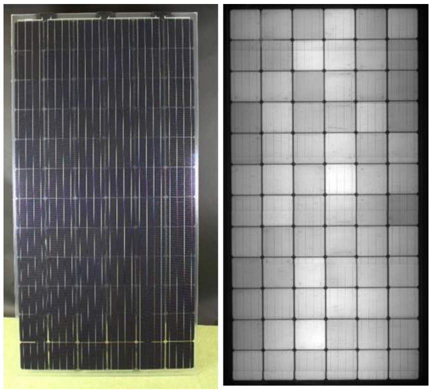

Fig. 3. (Left) Picture (Right) EL image of high efficiency 72 SHJ cells glass-glass modules produced in 2017.

As SHJ technology is aiming to very high efficiency PV cells, extensive studies are in place to increase cell efficiency. Tab.II. gives IV parameters of cells measured under Standard Testing Condition (STC) at Fraunhofer CalLab (independent). Process improvements all over the pilot line enabled to increase the absolute efficiency by 1%, including a new design for the metallization grid going from 4 to 6 busbars.

TABLE II
IV PARAMETERS OBTAINED FOR SHJ CELLS PRODUCED AT CEA-INES UNDER STC AT FRAUNHOFER CALLAB.

Cell	Area (cm²)	Voc (mV)	Jsc (mA/cm²)	FF (%)	η (%)
BB4	244.3	732.4	37.5	80.0	22.0
BB6	244.3	738.3	38.6	80.6	23.0

IV. CONCLUSION

In this work, we reported experimental results at cell and module levels obtained within a strong collaboration between 3SUN and CEA-INES on the deployment of silicon heterojunction technology at large production scale.

Some of the manufacturing criticalities analyzed during the production line design have been discussed. Anticipate, face and solve potential problems can occur during the industrial production is fundamental to aim high efficiency target.

Pre-production tests to evaluate the impact of wafers properties on cell efficiencies have been performed at CEA-INES pilot line. Results demonstrates the significant impact the material quality has on cell efficiency.

Finally, state-of-the-art SHJ cell efficiency and 72 cells bifacial modules have been presented. Results demonstrates once again that gap between hetero-junction and homo-junction is being reduced year by year and that SHJ technology is now mature to aim efficiencies above 22% at industrial level.

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