A novel, multi-frequency EIT System Architecture with Active Electrodes and early Digitalization at the Electrodes

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Abstract— **Electrical Impedance Tomography (EIT) is a functional real-time imaging modality based on measurement and reconstruction of spatial impedance distributions inside an object under test. The measurements are based on the injection of small well known alternating currents (AC) and the measurement of the developing voltages on the objects surface. The known currents and the measured voltages are used to calculate transfer impedances which are input data for the subsequent image reconstruction.**

In biomedical applications EIT is painless and has no known hazards. Currently, it is increasingly used in clinical applications, e. g. for lung ventilation monitoring. For that purpose a set of electrodes - normally arranged on a belt - is placed around the human chest. A shortcoming in present EIT systems is the need of long cables, which are connecting the analog signals from the electrodes to the data acquisition system. Due to the high impedance nature of the signal, they are highly afflicted by noise. To overcome this problem sophisticated shielding is necessary. Another problem arising with shielded cables are the stray capacitances, which even in driven shield settings are not negligible. Additional to possible stability problems in the cable shield driver also cable movements can change the stray capacitances and therefore falsify measurement results.

This work presents a novel, multi-frequency EIT system architecture with an early voltage digitalization direct at the electrodes to overcome the need of long shielded cables. The system is designed to work with a flexible number of electrodes in a frequency range of 10 kHz to 250 kHz. The system can be logically divided in the active electrodes, a control unit and a reconstruction computer. The active electrodes, as well as the control unit are based on a Field Programmable Gate Array (FPGA) Systems on Chips (SoC). The different SoC control data acquisition, data preprocessing and data transmission to the reconstruction computer and allow therefore a flexible system development.

Keywords—**Field-Programmable-Gate-Array (FPGA), System on Chip (SoC), Direct Digital Synthesis (DDS)**

I. Introduction

Electrical Impedance Tomography (EIT) is a functional real-time imaging modality based on measurement and reconstruction of spatial impedance distributions inside an object under test. The measurements are based on the injection of small well known alternating currents (AC) and the measurement of the developing voltages on the objects surface. The known currents and the measured voltages are used to calculate transfer impedances which are the input data for the subsequent image reconstruction [1-7].

Different EIT applications in geophysics, industry and live sciences have been proposed, e. g. rock investigations, pipeline monitoring or spectroscopic measurement of tissue. EIT can even be used, where other methods based on optical technologies or x-rays are not applicable, due to opaque mediums or too bulky or dangerous setups [7].

In biomedical applications EIT is cost effective, painless and has no known hazards. Currently, it is increasingly used in clinical applications, e.g. for lung ventilation monitoring. For that purpose a set of electrodes - normally arranged on a belt - is placed around the human chest [1, 3, 4]. A shortcoming in present EIT systems is the need of long cables, which are connecting the electrodes to the data acquisition system. This connection is due to the high impedance nature of the signals highly afflicted by noise. To overcome this problematic sophisticated shielding techniques are necessary. Another problem introduced by shielded cables is stray capacitance, which is even in driven shield settings not negligible. Additional to possible stability problems of the shield driver, also cable movements can change the stray capacitances and therefore falsify measurement results [7].

This work presents a novel, multi-frequency EIT system architecture with an early voltage digitalization direct at the electrodes to overcome the need of long shielded cables. The developed system is designed to work with a flexible number of electrodes in a frequency range of 10 kHz to 250 kHz. The system can be logically divided in the active electrodes, a control unit and a reconstruction computer. The active electrodes, as well as the control unit are based on a Field Programmable Gate Array (FPGA) System on Chip (SoC). Figure 1 shows an overview of the system architecture.

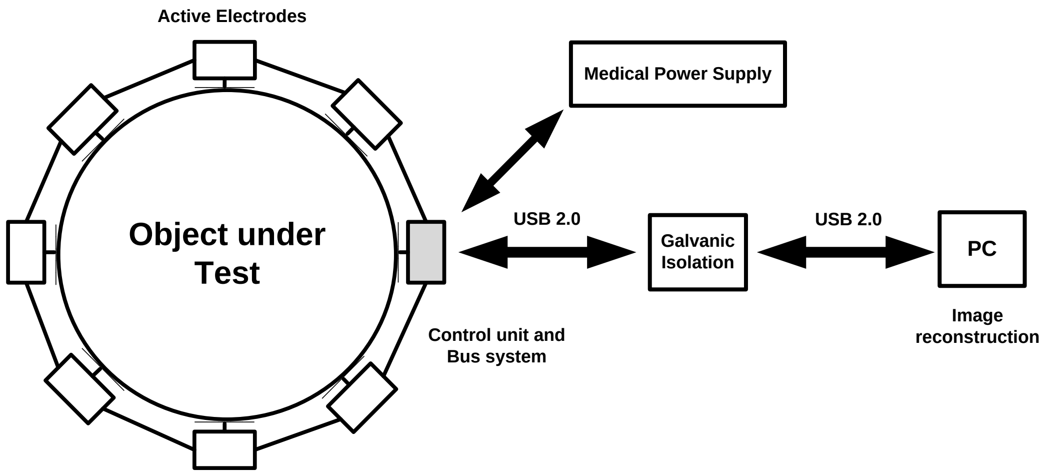

Fig. 1 – Overview of the architecture of the developed multi-frequency EIT system. The system consists of different logically units: the active electrodes arranged in a circle around the object under test, the control unit and the galvanic isolated reconstruction computer.

The active electrodes are placed around the object under test and are interconnected via short Flat Flex Cables (FPC) arranged as a bus system with the control unit. The active electrodes handle current generation and voltage measurements and are controlled by the control unit, which is connected via USB 2.0 to a host PC for further data processing and the subsequent image reconstruction. For electrical safety issues the USB link is galvanic isolated and the system is powered by a medical power supply.

II. HARDWARE

As already mentioned the developed hardware of the active electrodes is based on a SoC FPGA architecture. The FPGA (LFXP2 from Lattice Semiconductor) controls data acquisition, pre-processing and transmission in real-time. Figure 2 shows a detailed block diagram of the active electrodes.

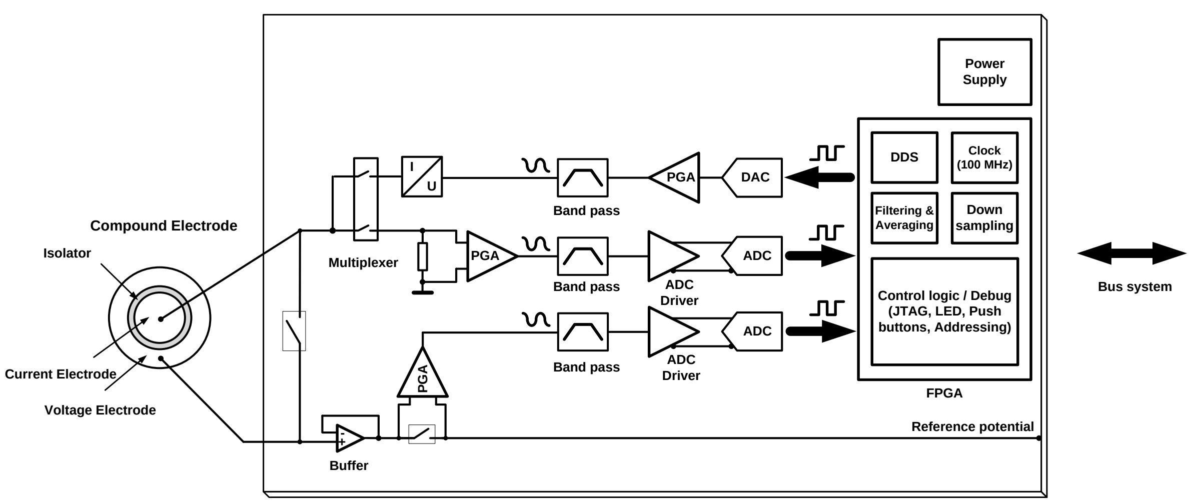

Fig. 2 – Block diagram of the active electrodes. Each active electrode can be operated in four different states and is connected to a compound electrode consisting of individual voltage and current electrodes on one side and on the other to the bus system.

Each active electrode is connected to a compound electrode consisting of a voltage electrode and a current electrode and to the bus system interconnecting the active electrode with the control unit. The active electrodes can be operated in four different states: voltage measurement, reference potential building, current sourcing and current sinking.

When operated in voltage measurement mode, the digitalization is realized by a fast, high-resolution Analog to Digital converter (ADC) against a reference potential. The ADC (LTC2296, Linear Technology) has a resolution of 14 bit and a maximum sampling rate of 25 Mega Samples Per Second (MSPS). To ensure the full scale use of the input voltage range, a Programmable Gain Instrumentation Amplifier (PGA, AD8250 from Analog Devices) is employed for adaptive signal amplification. The reference potential is built by another active electrode operated in the reference potential building state.

In current source mode the excitation signal is generated with a Digital to Analog Converter (DAC, LTC1668 from Linear Technology) with Direct Digital Synthesis (DDS) techniques implemented in the FPGA. The output voltage of the DAC is amplified by a PGA to allow adaptive output currents and afterwards filtered and fed to Voltage Controlled Current Source (VCCS). The VCCS is based on differential receiver amplifier (AD8130 from Analog Devices) and maintains a high output-impedance over a broad frequency range. Excitation signal wave form and frequency are arbitrary adjustable in a frequency range of 10 kHz to 250 kHz. Possible excitation waveforms, besides conventional sinusoidal signals are e. g. linear chirps, rectangular, triangle or signal-overlays. The advantage of linear chirps is a minimization of the data acquisition time within broadband impedance measurements [7]. Due to the system architecture multi-source current injection is also possible. To increase the current accuracy the current is additionally measured at the foot point via a shunt resistor.

After the measurement data is acquired via the ADC further signal filtering and conditioning is done on the active electrode e. g. averaging and down sampling. Afterward the data is transmitted to the control unit. Figure 3 shows a block diagram of the control unit.

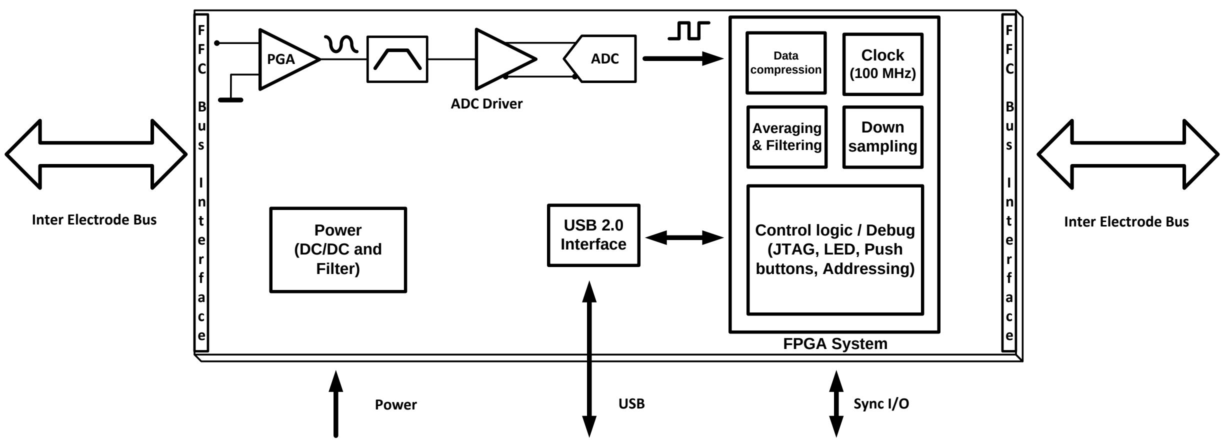

Fig. 3 - Block diagram of the control unit. The control unit acts as state controller for the active electrodes and is used as communication hub to the reconstruction computer.

The control units, as well as the active electrodes, are based on an embedded FPGA SoC. The SoC is used for the further data compression and as state controller for the active electrodes. The control unit is connected via a USB 2.0 interface, with a throughput of up to 40 Mbytes / s to the reconstruction computer. The USB link is bidirectional to allow a flexible system configuration by the reconstruction computer.

An ADC on the control unit allows the measurement of the reference potential to enable the detection of bad connected electrodes and the monitoring of the common mode voltage present in the system.

III. Software and image reconstruction

The FPGA of the active electrodes and the control unit are programmed in VHDL in connection with C. Whereby the interface modules are written in VHDL the main state machines are implemented with LatticeMico soft-microcontrollers in C. This divide allows a powerful system management and a high maintainability in connection with a quick software development.

The measurement demodulation is done digitally with a Fast Fourier Transform (FFT) based approach. This demodulation allows an evaluation of the impedance magnitude, as well as the impedance phase.

After the measurement data is preprocessed on the embedded hardware and transmitted to the reconstruction PC, the actual image reconstruction is done in MathWorks MATLAB in connection with EIDORS [5].

IV. SUMMARY AND OUTLOOK

This work presented a novel, multi-frequency EIT system architecture with active electrodes and early digitalization direct at the electrodes. The system is based on different FPGA SoC and allows multi-dimensional EIT measurements with a flexible number of electrodes. The system is designed to work in a frequency range of 10 kHz to 250 kHz and allow arbitrary wave forms. Due to the powerful FPGA architecture sophisticated DSP techniques can be directly used on the embedded system to increase measurement quality. Because of the digitalization direct at the electrode no shielded cables are necessary and therefore a minimization of stray capacitances is achieved.

After first tests and estimations of the needed data transmission rates a wireless data transmission is planned to eliminate any cables from the embedded system to the reconstruction computer. This expansion allows a further comfort increment of the usage of EIT and additional allows measurements outside of lab facilities.

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REFERENCES

1. Holder, D. S. (editor.), Electrical Impedance Tomography. Methods, History and Applications. Institute of Physics Publishing, 2005
2. Thiel, F., Bioimpedanz-Analysator zur nichtinvasiven Funktions und Zustandsanalyse von Geweben und Organen, PhD thesis, University of Hannover, Germany, 2003
3. Kaufmann S, Marquina-Sanchez R, Ryschka M, An Active Electrode-system for Electrical Impedance Tomography, In: Biomedical Engineering (2011), Vol. 56, ISSN 0939-4990
4. Gaggero P. O. Miniaturization and Distinguishability, Limits of Electrical Impedance Tomography of Biomedical Application. University of Neuchâtel, Dissertation, 2011 Switzerland
5. Frerichs I, Schiffmann H, Hahn G, .Dudykevych T, .Just A, Hellige G, Funktionelle elektrische Impedanztomographie (2005) Eine Methode zur bettseitigen Überwachung der regionalen Lungenfunktion Med 42:66-73 (2005)
6. Adler A., Lionheart W. R. B., Uses and abuses of EIDORS: an extensible software base for EIT. In: J. Physiological Measurement (27) 2006, p. 25-42
7. Brown B. H., Medical impedance tomography and process impedance tomography: a brief review, Measurement Science and Technology, 2001 (12), p.991-996
8. Min M., Land R., Paavle T., Parve T, Annus P, Trebbels D., (2011) Broadband spectroscopy of dynamic impedances with short chirp pulses. In: J. Physiological Measurement (32) 2011, p. 945-958