Invited Paper

Recent Trends and Considerations for High Speed Data in Chips and System Interconnects

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***Abstract*—This paper discusses key issues related to the design of large processing volume chip architectures and high speed system interconnects. Design methodologies and techniques are discussed, where recent trends and considerations are highlighted.**

***Keywords*—VLSI, chip architecture, interconnects, antennas, optics, access, coding.**

I. Introduction

Increased computational capability requires high speed data transmission and efficient in-chip processing. This paper covers key issues related to overall system design, starting with a review on Very Large Scale Integration (VLSI) methodologies, followed with current VLSI design challenges, these topics are presented in section II. System interconnects are covered in section III, highlighting the issues related to interconnect size and the losses for both Integrated Circuit (IC) or printed circuit board (PCB) designs. Section IV deals with new challenges related to high speed data applications within a chip or between multiple chips; it describes the Wireless-Optical Network on Chip (WONoC) approach to achieve the throughputs needed for high speed data applications, like 5G. The WONoC architecture requires chip antennas, optical interconnects, low-complex error correcting schemes, and efficient access techniques. Overall, this paper provides insight into the challenges that emerging high speed data applications present to the designer, as well as implementations and techniques that can trigger new hardware and software for next generation devices.

II. Efficient Chip Architectures and VLSI Design Methodology

VLSI design is gradually moving towards higher levels of abstraction in order to take advantage of its numerous benefits over traditional register transfer level (RTL) design approaches. It has taken three generations and over one decade to behavioral synthesis before being seriously considered at the commercial level.

Increase design complexity is forcing designers to shift their design methodology from RTL to Electronic System Level (ESL). The main driving force behind the adoption of ESL is the level of maturity of the commercial tools and their capability to deal with system level design issues. This is also the main difference between traditional High Level Synthesis (HLS) and new generation ESL synthesis tools. HLS solves the problems of synthesizing single processes and is still a core part of modern ESL, but the main advantage of ESL is its capability to deal with complete systems. These capabilities include: system level verification, Hardware (HW)/Software (SW) co-simulation, automatic bus interface generation, and automatic design space exploration to name a few.

This increasing design complexity leads to new challenges which behavioral level VLSI design can address more efficiently than lower levels of abstraction. In many cases, the design specifications are unstable and any changes in them can lead to different architectural considerations (e.g. on-die memory or external memory, bus hierarchies, etc.). At the RTL, this requires major re-design cycles, while at the behavioral level these changes can be absorbed easier. Another important advantage of raising the level of abstraction over traditional design flows is that it allows software and hardware designers to 'speak' the same language. Applications to be implemented in custom hardware are getting extremely complex and are based on complex mathematical models that in many cases are difficult to understand by the hardware designer. Using the same behavioral description language allows both hardware and

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software designers to communicate at the same abstraction level using the same language. Some examples of complex applications include dedicated hardware security engines based on complex encryption and decryption algorithms [1]. Moreover these complex algorithms need to be modified by the hardware designer in order to obtain a more efficient architecture e.g. reduced memory, split memory, elimination of recursion, improvement of throughput and latency, and data types' refinement. These manual modifications can be hard to achieve and might lead to the implementation of a design with the wrong functionality. One last advantage of increasing the level of abstraction is the acceleration of time consuming simulations. RTL simulations are slow and do not allow to simulate entire System-on-a-Chip (SoC) architectures. Behavioral simulation models accelerate the simulation and enable the simulation of larger designs. HLS has been widely studied in academia for numerous years and there are multiple commercial and academic HLS tools available. Some commercial ones include CyberWorkBench [2], CatapultC [3], Stratus [4], while an academic example can be. LegUp [5] (open source). The main differentiation factors between all these tools are the input language support (ANSI-C, C++ and/or SystemC), target technology (FPGA, ASICs or both), and more importantly, the system level design and verification capabilities, as all of these tools are built around a traditional HLS engine. In [6], a good survey of current HLS tools and the history of HLS are covered.

A. VLSI Design Challenges

In order to synthesize complete C-based SoCs there are some features that any ESL synthesis tool should support. Firstly, it should allow the synthesis of any digital application. HLS has traditionally synthesized effortlessly data-dominated applications (i.e. designs that have many arithmetic operations and less control structures) e.g. FIR filters, FFTs, graphic decoding, but could not handle intensive control and interfaces where timing information is needed. Secondly, it needs to provide a path for interconnecting different processes together in different ways, e.g. point to point, bus, bus-hierarchies and allowing the simulation of these configurations quicker than RTL. Thirdly, most of the new SoC designs are incremental designs based on previous designs. As these SoCs have normally all been developed at the RT-level, a way to integrate these legacy RTL blocks or RTL Intellectual Property (IP) should be considered. Moreover, there should be a way to verify the SoC at different levels ranging from single processes, multiple processes, C/SC processes combined with legacy RTL blocks and HW/SW co-simulation. Lastly, at the deep-submicron level, physical design needs to be accounted in order to achieve the design closure. E.g. Wire-delay is becoming the dominant delay, but it cannot be determined until the design has been synthesized, placed and routed. Other factors of extreme significance are power and thermal-related issues. Smaller size transistors allow higher logic densities but involve also that the leakage power is now becoming a significant design factor and is reaching a point where it equals the dynamic power consumed in the chip [7]. Low-K dielectrics, triple-oxides, improved design tools and power efficient architectures have avoided so far the most pessimistic forecasts, but extreme power consuming devices are generating great amounts of heat. State of the art microprocessors like the Intel's new Itanium processor now incorporate power controllers on the same die [8] and the new Field-Programmable Gate Arrays (FPGAs), like Xilinx's Virtex 5 [9] incorporate on-chip power supply and thermal monitoring capabilities. Reducing temperature increase is becoming a major issue of concern for highly integrated circuit designs that should be addressed in the overall design process in order to keep the chip temperature as low as possible [10].

Temperature has an adverse effect on multiple aspects. It affects the lifetime of the integrated circuit by accelerating the chemical process taking place inside of the chip following Arrhenius equation. Studies show that the mean time between failures (MTBF) of an IC is multiplied by a factor 10 for every 30^{o}C rise in the junction temperature [11]. Secondly, leakage power is becoming the dominant source of power consumption for new process technologies, which grows exponentially with temperature. Moreover, temperature has a negative effect on carrier mobility and therefore affects the switching speed of the transistors and, thus, the overall timing of the circuit [12]. Consequently, it is highly desirable to have an even temperature distribution on the chip in order to avoid costly re-design due to timing/temperature and simplify the verification phase. Furthermore, expensive heat sinks are required to maintain the chip at a reasonable temperature or could not be used in case of embedded systems. Studies have reported that above 30-40 Watts (W), additional power dissipation increases the total cost per chip by more than $1/W [13]. It is therefore extremely important to consider the physical effects at the earliest possible design stages. Design flow for complex SoCs, should tightly integrate the main design steps from HLS, logic synthesis until the physical design. Once the design is placed and routed, detailed information regarding area, delay, power and temperature can be extracted and fed back to the HLS tool to perform new optimizations in order to meet the design constraints. One of the optimizations that the HLS can do to meet the design constraints is to re-schedule the operations or rebind them in order to reduce the peak temperature in the design.

III. HIGH SPEED INTERCONNECTS ON AN ELECTRONIC SYSTEM

This section of the paper points out aspects to consider when designing interconnects at the different levels of a system. While shrinking a transistor enhances its performance, scaling down the interconnections that carry the signals within and outside the chips negatively affects the performance of the system. In fact, the limits imposed by interconnects to the evolution of high-speed electronics was identified more than ten years ago when Radio Frequency Complementary Metal–Oxide–Semiconductor (RF-CMOS) emerged [14]. Signals travel between gates at a micrometer level, but also between different Printed Circuit Boards (PCBs) through large connectors. Many levels are found between these two cases [15]. At each one of these levels, effects that degrade the

signals become apparent, and are related to two characteristics of a wired channel: its distributed nature (which introduces delay and losses) [16], and mismatch [17]. Here, the first point is discussed.

Along its way between stages, the signal magnitude is reduced mainly due to three effects: i) the resistance of the metal forming the interconnects, ii) the polarization of the dielectric due to the alternating fields, and iii) undesired Electro Magnetic (EM) coupling. When neglecting the latter, the associated attenuation (α) is the sum of the metal (αc) and dielectric (αd) losses. Thus, for a generic interconnect, a cascaded RLGC lumped element model can be used to represent its distributed nature, where the per-unit-length resistance (R) and conductance (G) are associated with αc and αd, respectively. Thus, for a design-oriented model, the number of RLGC stages to represent an interconnect of a given length (l) up to certain frequency (f) can be determined as: $n = 2\pi f(\mathrm{LC})^{0.5}/\Delta$, where Δ is a fitting parameter [18].

At the PCB level, interconnects present lengths in the order of centimeters. Thus, considering typical values for L and C, hundreds of blocks are required to represent an interconnection up to some gigahertz. In contrast, few blocks are needed for lines used at Integrated Circuit (IC) level. This does not mean that losses and delay are not significant on IC interconnects, but just that the corresponding effect is more concentrated. In fact, the losses occurring on PCB are considerably lower than those related to ICs since the cross section of the metals is larger. In this regard, when plotting α and the phase delay (β) versus frequency curves for an interconnect on PCB, different regions of operation are identified through the slope that the data presents [19]. Thus, within each one of these regions the RLGC circuit can be simplified, for instance to a simpler RC.

The dependence on frequency of the series resistance of the line can be ignored at frequencies where the metal skin depth is larger than the cross section of the interconnect, whereas the dielectric losses can be neglected at all (i.e., G ≈ 0) provided that the polarization current is negligible. Details about the limits defining acceptable representations for interconnects operating at high frequencies can be found in [19] and [20]. Bear in mind, however, that scaling down interconnects substantially increases the losses. In fact, in an actual interconnect with cross section scaled down by a factor k, R increases in the same proportion whereas the dielectric losses remain constant. This is because the distribution of the EM fields through the line remains the same provided that the propagation mode does not vary [21].

Notice that for interconnects with large cross section such as those found in PCB technology (e.g., k = 1) the metal losses are smaller than those associated with the dielectric. Conversely, as the cross section is made smaller such as in the case of interconnects on high density packages (e.g., k = 5), the metal losses double those associated with the dielectric. The problem becomes even more accentuated on ICs. Thus, system on package (SoP) technologies represent a viable alternative to move the longest interconnects outside the chip (e.g., the clock network).

IV. Wireless – Optical Network on Chip

Network-on-Chip (NoC) is the paradigmatic architecture to interconnect multiple functional units in a chip with the minimum latency. However, although NoC can achieve a high throughput, its current architecture could be not enough for meeting the data rates of the 5G communications. Indeed, 5G PPP predicts a raise up to 1000 times of data requirement by 2020 due to the presence of M2M communications [22][23]. Moreover, International Technology Roadmap for Semiconductors (ITRS) has anticipated that the integration technology from FETs will move from current 24nm to 7.5nm in 2025 which will shrinkage the bus lines increasing the cross-talk effects [24]. For these tokens, the next generation of NoC will have to modify its architecture. In particular, they will use multiple physical layers. This is the so-called Wireless-Optical Network-on-Chip (WONoC) which presents a more challenging architecture compared to its classical counterpart. In particular, it combines chip antennas, optical interconnects, low-complex error correcting schemes, and efficient access techniques. All these concepts are revisited in the following sections with further detail.

A. Architecture

WONoC emerges as a promising solution for overcoming the scalability problem of NoC. In order to increase the data-rate, it is necessary to introduce a larger number of cores that run in parallel. However, when it is necessary to communicate distant cores, large delays are introduced. In order to cope with this drawback, chip antennas are used to broadcast RF transmissions in a single hop to a large number of cores. Simultaneously, optical links communicate close cores at high-data rates. Nonetheless, larger data rates generally claim for larger bandwidths which demand higher frequencies. However, the increase of the frequency implies to have larger propagation losses. This fact is critical in the RF transmissions since the antenna and the wireless channel impairments introduce fluctuations in the RF cannel [25], [26]. Additional techniques such as ultra-low power coding schemes and smart access methods have to be used for improving the performance of WONoC [27], [28]

B. On Chip Antenna

Wireless data transceivers require integrated chip antennas, linked to the interconnections described in section III. Traditionally, antennas are off-chip due to their size and because CMOS grade Si substrates are highly conductive. In contrast, on chip antennas result in fully integrated, low cost wireless links with no bond wires and off-chip components. System-on-chip (SoC) integrates digital baseband and complete RF front-ends, on a single chip. At the same time, by using millimeter-waves, the antenna has a reduced size, and large bandwidths can be obtained with an adequate design. There are four fundamental types of antennas that have been used as on-chip antennas: monopole, dipole, loop, and Yagi-Uda antennas. The choice for a particular application is dependent on the requirements of gain, impedance, radiation, and the available chip area [29-30].

One of the major challenges involved with chip antennas is the poor radiation efficiency due to lossy CMOS grade Si substrates, some common techniques involve adding low loss dielectric layers to avoid substrate losses and enhance antenna bandwidth [29-31]; in the following paragraphs, a review of highly integrated on-chip antennas is provided.

In [32], an inverted-F and a quasi-Yagi antenna on a standard low resistivity substrate (10 Ωcm) are presented. These antennas were implemented with a specialized BEOL technology where proton implantation in the substrate is used to increase the resistivity, reduce substrate losses, and improve performance. In [33], dipole, Yagi, rhombic, and loop antennas using CMOS technologies for millimeter wave operation are demonstrated. In [34], a planar triangular-60-GHz millimeter-wave RFIC-on-chip triangular monopole antenna is presented. The antenna is fabricated using a 0.18-μm CMOS process. In [35], a 60-GHz artificial magnetic conductor (AMC)-based circularly polarized (CP) on-chip antenna designed and fabricated using standard 0.18-μm six metal-layer CMOS technology is presented. The design consists of a wideband circularly polarized loop antenna. In [36], a planar tab monopole antenna structure has been achieved. The chip antenna was realized with the back-end-of-line process of standard CMOS silicon. In [37], an antenna fabricated using multilayer LTCC is presented. This technology allows design flexibility and low loss due to its metal and dielectric stacked layer design. In [38], a dual band antenna consisting of a radiating slot and an air-filled cavity is presented. The antenna is fabricated using the CMOS and IPD processes with flip-chip technology.

C. Optical interconnects

Optics can address key issues for dense, low-power interconnects [39]. Typically, optical interconnects implement an on-off keying (OOK) intensity modulation, as it reduces the complexity of the associated subsystems. The following paragraphs introduce the different parts of a transmission system for optical interconnects based on OOK, including transmitter, channel and receiver.

Regarding the transmitter, we can distinguish two approaches: a directly modulated optical source or an on-chip optical modulator excited by an off-chip light source. Lasers constitute the most popular light source in telecommunications and are made from III-V materials. However, crystal defects arise when epitaxial growing III-V compounds on silicon, degrading the performance of the devices. Instead of modulating the laser directly, one could use an external (off-chip) laser whose output would be coupled to the chip, feeding on-chip optical modulators. This approach has the advantage that source power dissipation is removed from the chip. Interestingly, a multiple wavelength off-chip light source is possible, enabling on-chip wavelength division multiplexed (WDM) systems. As for the modulators, they can be either refractive or absorptive.

Refractive components are only able to change the refractive index of the material by applying a voltage. So, an interferometer structure is essential for transforming this refractive index variation into an optical intensity variation [40]. However, the refraction index change in silicon is relatively weak, requiring high power consumption. An alternative approach is to use resonators, e.g. silicon micro-ring resonators [41]. These devices can be efficient and small; even they have very small resonances that have to be precisely tuned. This effect can be turned into an advantage, as tuned micro-ring resonators could be able perform WDM switching functions [42]. Electro-absorption modulators work by changing the optical absorption in a semiconductor by applying a voltage to it [43]. These mechanisms are very strong and low operating energies are possible with no electrical amplifiers [44].

Regarding the channel, one can distinguish two possibilities: optical waveguides or free space optics. Optical waveguides in silicon are an interesting and promising approach [45]. Silicon is transparent for the wavelengths typically used in telecommunications. So, silicon waveguides feature low propagation loss at chip scales [46]. Alternatively, free space optics can also be used as a channel for establishing connections within a chip. As free space interconnects suit regular connection patterns, it is particularly interesting for regular on-chip networks [47].

The receiver converts the optical signal into a current that is turned into a suitable logic-level signal. In terms of the on-chip power dissipation, the photodetector efficiency is an irrelevant quantity. A key parameter is the capacitance of the receiver, restricting the circuit topologies [48]. Photodetectors can be easily fabricated with enough low capacitance [49]. However, they are usually integrated with a transistor for providing enough output signal amplitude, increasing the total capacitance of the receiver [50].

In summary, optics has significant benefits for on-chip interconnects. An interesting approach is when employing WDM, as it opens the door to novel architectures for on-chip networks [50]. Then, more information density would be possible and the on-chip network could be easily scalable by performing simple wavelength add/drop operations.

D. Coding

In order to provide a higher reliability to the WONoC interconnections, it is possible to resort to the same strategies used in classic communication networks. On this subject, the works of [51]1-[54] review the classic error control techniques in NoC such as Error Control Coding (ECC), Automatic Repetition request (ARQ), or Hybrid ARQ. Both works conclude that, when time constraints are tight and link distances are short, it is preferable to use multibit-ECC techniques. However, given the inherent difficulty of decoding multi-bit error correction, the works of [55-56] combine single error correction with ARQ techniques for NoC interconnects. This solution, although also it is able of ensuring the reliability of the transmitted data as well augments the bus size and so the area to integrate raise. Fortunately, recent advances in multi-bit error correction capability have considerably reduced the decoding time. This fact has motivated that coding schemes initially devised for wireless networks start to be applied in the sub-micron domain

[57-[58]. This is the case of BCH codes, which algebraic definition even permits to obtain the closed-solution to the position of the erroneous bits [59]. This occurs for the case of one and two errors whereas for the case of correcting three errors it is necessary to pre-save any data in memory [60]. For larger number of errors BCH codes still need to use an iterative decoder. The reason is that BCH decoders need to obtain a polynomial defined in the Galois Field which roots correspond to the number of errors in the received codeword. The largest is the degree of the GF and the number of errors in the received codeword the highest is the complexity for solving it. Nonetheless, BCH codes attain hard-decoding bound with small complexity which it is quite interesting for ensuring the reliability in low-complex system with a high data-rate.

E. Access

WONoC has an architecture that overcomes the shrinkage of the bus lines and the high latency among distant cores. Initial WONoC implementations experimented with traditional MAC channelization of available resources such as FDMA and TDMA [61], Sec V.A. Furthermore, CDMA-based solutions are proposed to reduce access delay enabling multiple simultaneous transmissions using spreading codes such as Walsh sequences [62].

The main drawback of these schemes is that their complexity does not scale well with increase of number of cores. As a solution, [63] and [64] propose a robust token management scheme and a Slotted ALOHA and Carrier-Sense Multiple-Access (CSMA) to mm-wave WNoC respectively.

Collisions among neighboring cores could be avoided by employing specific WNoC architectures. For example [65] divides the WNoC in a hierarchical way. Thus it is reduced the packet latency and the power consumption a 16% and 14% respectively in comparison with the non-wireless NoC. Instead of avoiding collisions, recent work demonstrates that, using successive interference cancellation (SIC) for resolving the collisions in slotted ALOHA could be exploited [66]. Specifically, it is possible to resolve collisions if multiple packet replicas are transmitted across different time slots and clean packet replicas in certain slots are detected and removed from collisions in other slots [66].

Following this idea, slotted ALOHA schemes outperform CSMA-based [67]. In particular, in scenarios with large density of transmitting and receiving antennas such as WNoC, cooperative slotted-ALOHA with SIC could provide simple, efficient and scalable solution [68].

V. CONCLUSIONS

Highly efficient chip architectures should account for avoidance of hot spots, by distributing or reconfiguring processing and storing functions in the available chip area during the design stage.

High performance interconnect design requires accurate parasitic avoidance for good impedance matching. Interconnect size and the materials used to implement them play an important role on signal losses.

WONoC can provide the high throughput required for new high data rate applications. Wireless links can be used to broadcast signals to diverse cores or to distant cores, while optical links connect adjacent cores with high data links. Coding schemes and smart access methods play a crucial role in high performance WONoCs.

REFERENCES

[1] S. Morioka, K. Wakabayashi, B. Carrion Schafer, "Complex Security Engine Design with High Level Synthesis". MPSoC, 2009.

[2] CyberWorkBench, "http://www.cyberworkbench.com"

[3] Calypto. 2012. http://www.calypto.com/catapult c synthesis.php.

[4] Cadence. 2011. http://www.cadence.com/products/sd/stratus.

[5] LegUP. 2011. http://legup.eecg.utoronto.ca

[6] J. Cong, et al, "High-Level Synthesis for FPGAs: From Prototyping to Deployment", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol 30, Issue 4, pp 473-491, 2011

[7] F. Fallah and M. Pedram, "Standby and Active Leakage Current Control and Minimization CMOS VLSI Circuits," IEICE Transactions on Electronics, Vol. 88, pp. 509-519, 2005.

[8] T. Fischer, et al, "A 90-nm Variable Frequency Clock System for a Power-Managed Itanium Architecture Processor," IEE Journal of Solid-State Circuits, Vol.41, No.1, January 2006.

[9] Xilinx, "Xilinx datasheet," wwww.xilinx.com.

[10] K. Banerjee and A. Mehrotra, "Global (Interconnect) Warming," Circuit & Devices, Vol. 17, pp. 16-32, September 2001

[11] National Semiconductor, USA, Understanding Integrated Circuit Package Power Capabilities, www.national.com, April 2000.

[12] A.H. Ajami, et al, "Effects of none-uniform substrate temperature on the clock signal integrity in high performance designs," Proc. CICC,pp. 223-236, 2001.

[13] S. Borkar, "Design Challenges of Technology Scaling," IEEE Micro, Jul-Aug. 1999.

[14] J. Davis, et al, "Interconnect limits on gigascale integration (GSI) in the 21st century," Proc. IEEE, vol. 89, no. 3, pp. 305-324, Mar. 2001.

[15] W.J. Greig, Integrated Circuit Packaging, Assembly and Interconnections, New York: Springer, 2007.

[16] A. Djordjevic, et al, "A note on the modeling of transmission-line losses," IEEE Tran. Microw. Theory Tech., vol. 51, no. 2, pp. 483-486, Feb. 2003.

[17] G. Hernández-Sosa, et al, "Impedance matching of traces and multilayer via transitions for on-package links," IEEE Microw. Wireless Comp. Lett., vol. 21, no. 11, pp. 595-597, Nov. 2011.

[18] O. González-Díaz, et al, "A design-oriented methodology for accurate modeling of on-chip interconnects," Analog Integrat. Circ. Signal Proc., vol. 71, no. 2, pp. 221-230, May 2012.

[19] H. Johnson and M. Graham, High Speed Signal Propagation: Advanced Black Magic. Englewood Cliffs, NJ: Prentice-Hall, 2003.

[20] R. Torres-Torres and V.H. Vega-González, "An approach for quantifying the conductor and dielectric losses in PCB transmission lines," in Proc. IEEE EPEPS, Tigard, OR, Nov. 2009, pp. 235-238.

[21] V. Vega-González, et al, "Analysis of the electrical performance of multi-coupled high-speed interconnects for SoP," in Proc. IEEE Int. Midwest Symp. Circ. Syst., Cancun, Mexico, Aug. 2009, pp.1030-1033.

[22] http://networld2020.eu/wp-content/uploads/2014/02/NetWorld2 020_Joint-Whitepaper-V8_public-consultation.pdf.

[23] Cisco Visual Networking Index: Global Mobile Data Traffic Forecast Update, 2010 - 2015

[24] Int. Technology Roadmap for Semiconductors [Online]. http://www.itrs.net/links/2013ITRS/Summary2013.htm

[25] Z.Chen,Y.Zhang,"Inter-Chip Wireless Communication Channel: Measurememt, Characterization, and Modeling", In Proc. IEEE Trans. On Antennas And Propagation, vol.55,nº3,pp.978-986, March 2007.

[26] Y.P.Zhang,"Bit-Error-Rate Performance of Intra-Chip Wireless Interconnect Systems", In Proc. IEEE Communication Letters, vol.8,nº1, pp.39-41,January 2004.

[27] N.Mansoor, et al, "An Energy-Efficient and Robust Millimeter-Wave Wireless Network-on-Chip Architecture", In Proc. Of IEEE Int. Symp. On Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT),2013, pp.19-24.

[28] A.Rezai, et al, "HiWA: A Hierarchical Wireless Network-on-Chip Architecture", In Proc. Of Int. Conf. On High Performance Computing & Simulation (HPCS), 2014,pp.499-505.

IEEE Conference Publications

[29] Hammad M, et al, "The Last Barrier: On Chip Antennas," IEEE Microwave Magazine, Vol. 14, No. 1, pp. 79-91, January 2013.

[30] A.Shamin, et al, "On-chip Antenna: Practical Design and Characterization Considerations," 14th International Symposium on Antenna Technology and Applied Elecromagnetics and the American Electromagnetics Conference, 2010.

[31] K. Takahagi, et al, "Ultra-wideband silicon on-chip antennas with artificial dielectric layer," presented at the Int. Symp. on Intelligent Signal Processing and Communication Systems,Dec. 7–9, 2009.

[32] Y. Zhang, et al, "On-chip antennas for 60-GHz radios in silicon technology," IEEE Trans. Electron Devices, vol. 52, no. 7, pp.1664-1668, July 2005

[33] F. Gutierrez, et al, "On-Chip Integrated Antenna Structures in CMOS for 60 GHz WPAN Systems," IEEE JOURNAL ON SELECTED AREAS IN COMMUNICATIONS, VOL. 27, NO. 8, OCTOBER 2009.

[34] C.-C. Lin, et al, "A 60-GHz millimeter-wave CMOS RFIC-on-chip triangular monopole antenna for WPAN applications," IEEE Antennas Propag. Soc. Int. Symp., Jun. 9- 15, 2007, pp. 2522-2525.

[35] X.-Y. bao, et al, " 60-GHz AMC-Based Circularly Polarized on-Chip Antenna using Standard 0.18-?m CMOS Technology," IEEE Transactions on Antennas and Propagation, Page(s): 2234 - 2241, 2012.

[36] Wanlan Yang, et al, "A 60GHz On-Chip Antenna in Standard CMOS Silicon Technology" .Circuits and Systems (APCCAS), 2012 IEEE Asia Pacific Conference on, Issue Date: 2-5 Dec. 2012

[37] S. Y. Park et al, "Compact UWB chip antenna design," Proceedings of Asia-Pacific Conference, pp.730-733, 2010.

[38] Ta-Yeh Lin, et al, "Design of Dual-Band Millimeter-Wave Antenna-in-Package Using Flip-Chip Assembly Components", Packaging and Manufacturing Technology, IEEE Transactions on Volume: 4, Issue: 3 DOI: 10.1109/TCPMT.2014.2300166 Publication Year: 2014 , Page(s): 385- 391.

[39] D. A. B. Miller, "Device Requirements for Optical Interconnects to Silicon Chips," Proceedings of the IEEE, Vol. 97, no. 7, pp. 1166-1185, 2009

[40] A. Liu, et al. "Recent development in a high-speed silicon optical modulator based on reverse-biased pn diode in a silicon waveguide," Semicond. Sci. Technol., vol. 23, p. 064001, 2008.

[41] Y. Luo, et al, "40 GHz AlGaInAs multiple-quantum-well integrated electroabsorption modulator/distributed feedback laser based on identical epitaxial layer scheme," Jpn. J. Appl. Phys., vol. 45, Express Lett., pt. 2, pp. L1071-L1073, 2006.

[42] S. Zheng, et al, "Microring-resonator cross-connect filters in silicon nitride: Rib waveguide dimensions dependence," IEEE J. Sel. Topics Quantum Electron., vol. 12, pp. 1380-1387, 2006.

[43] B. E. A. Saleh and M. C. Teich, Fundamentals of Photonics, John Wiley & Sons, 2007

[44] J. E. Roth et al, "BC-band side-entry Ge quantum-well electroabsorption modulator on SOI operating at 1 V swing," Electron. Lett., vol. 44, pp. 49-50, 2008.

[45] H. Yamada, et al, "Si photonic wire waveguide devices," IEEE J. Sel. Topics Quantum Electron., vol. 12, pp. 1371-1379, 2006.

[46] D. K. Sparacin, et al, "Silicon waveguide sidewall smoothing by wet chemical oxidation,"J. Lightw. Technol., vol. 23, pp. 2455-2461, 2005.

[47] D. A. B. Miller, et al, "Opportunities for optics in integrated circuits applications," in Proc. IEEE (ISSCC) Dig. Tech. Papers, vol. 1, San Francisco, CA, Feb. 6-10, 2005, pp. 86-87.

[48] M. Georgas, et al, "A monolithically-integrated optical receiver in standard 45-nm SOI," In Proc. ESSCIRC 2011, pp. 407-410.

[49] C. T. DeRose, et al. "Ultra compact 45 GHz CMOS compatible germanium waveguide photodetectors with low dark current," Optics Express vol. 19, pp. 24897-24904, 2011.

[50] J. Orcutt, et al, "CMOS Photonics for High Performance Interconnects," in Optical Fiber Telecommunications VIA, I. P. Kaminow, T. Li, A. E. Willner Eds; Elsevier Academic Press 2013.

[51] D.Bertozzi, et al, "Error Control Schemes for On-Chip Communication Links: The Energy Reliability- Tradeoff", In proc. IEEE Trans. On Computer-Aided Design Of Integrated Circuits and Systems, vol.24, nº6, June 2005.

[52] S.Sridhara, N.Shanbhag,"Coding for System-on-Chip Networks: A Unified Framework", In proc. IEEE Trans. On Very Large Scale Integration (VLSI) Systems, vol.13,nº6, June 2005.

[53] A.Salem, et al, " Coding Algorithms for Network on a Chip",In proc. Of IEEE Conference on Systems On Chip, pp.216-221,2013

[54] A.Ejlali, et al,"Performability/Energy Tradeoff in Error-Control Schemes for On-Chip Networks", In proc. IEEE Trans. On Very Large Scale Integration (VLSI) Systems, vol. 18,nº1, January 2010.

[55] B.Fu, P.Ampadu,"On Hamming Product Codes With Type-II Hybrid ARQ for On-Chip Interconnects", In Proc. IEEE Trans. On Circuits and Systems I. vol.56,nº9,pp.2042-2054,September 2009.

[56] W.Flayyih, et al, "Crosstalk-Aware Multiple Error Detection Scheme Based on Two-Dimensional Parities for Energy Efficient Network on Chip", In Proc. IEEE Transactions on Circuits and Systems I. vol.61,nº7,pp.2034-2047,July,2014.

[57] Chia-Ching Chu, et al, "A fully parallel BCH codec with double error correcting capability for NOR flash applications," in Proc. IEEE ICASSP, 2012, pp.1605-1608.

[58] I. Yoo and I.-C. Park, "A Search-less DEC BCH Decoder for Low-Complexity Fault-Tolerant Systems," in Proc. IEEE SiPS, 2014, pp. 44-49.

[59] A.Enrich, J.Bas,"Low-Complexity Soft and Hard-Binary Bose-Chaudhuri-Hocquenghem (BCH) decoding for IEEE 802.15.6 Machine-to-Machine Communications", In proc. European Wireless (EW) 2014, May,2014, Barcelona, Spain.

[60] Xinmiao Zhang and Zhongfeng Wang, "A Low-Complexity Three-Error-Correcting BCH Decoder for Optical Transport Network," IEEE TCAS-II, vol.59, no.10, pp.663-667, 2012.

[61] Deb, S., et al. Wireless NoC as interconnection backbone for multicore chips: Promises and challenges. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems,2*(2), 228-239, 2012.

[62] Vidapalapati, A., et al. NoC architectures with adaptive Code Division Multiple Access based wireless links," *IEEE International Symposium on Circuits and Systems 2012*, pp. 636-639, May 2012.

[63] Mansoor, N., et al. "An Energy-Efficient and Robust Millimeter-Wave Wireless Network-on-Chip Architecture," *IEEE Int. Symp. On Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT) 2013*, pp.19-24, 2013.

[64] Piro, G., et al. Initial MAC Exploration for Graphene-enabled Wireless Networks-on-Chip," *ACM The First Annual International Conference on Nanoscale Computing and Communication*, pp. 1-9, 2014.

[65] Rezai, A., et al. "HiWA: A Hierarchical Wireless Network-on-Chip Architecture", *Proc. Int. Conf. On High Performance Computing & Simulation (HPCS)*, pp.499-505, 2014.

[66] E. Casini, et al, "Contention resolution diversity slotted aloha (CRDSA): An enhanced random access scheme for satellite access packet networks," IEEE Transactions on Wireless Communications, vol. 6, no. 4, pp. 1408-1419, 2007.

[67] Liva, G., Graph-based analysis and optimization of contention resolution diversity slotted ALOHA," *IEEE Transactions on Communications,59*(2), 477-487, 2011.

[68] Jakovetic, D., et al. Cooperative Slotted ALOHA for Multi-Base Station Systems," *IEEE Transactions on Communications*, to appear, 2015