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Reversible Binary Arithmetic for Integrated Circuit Design

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***Abstract*—**Application of reversible logic in integrated circuits results in the improved optimization of power consumption. This technology can be put into use in a variety of low power applications such as quantum computing, optical computing, nano-technology, and Complementary Metal Oxide Semiconductor (CMOS) Very Large Scale Integrated (VLSI) design etc. Logic gates are the basic building blocks in the design of any logic network and thus integrated circuits. In this paper, reversible Dual Key Gate (DKG) and Dual key Gate Pair (DKGP) gates that work singly as full adder/full subtractor are used to realize the basic building blocks of logic circuits. Reversible full adder/subtractor and parallel adder/ subtractor are designed using other reversible gates available in the literature and compared with that of DKG & DKGP gates. Efficient performance of reversible logic circuits relies on the optimization of the key parameters viz number of constant inputs, garbage outputs and number of reversible gates. The full adder/subtractor and parallel adder/subtractor design with reversible DKGP and DKG gates results in least number of constant inputs, garbage outputs, and number of reversible gates compared to the other designs. Thus, this paper provides a threshold to build more complex arithmetic systems using these reversible logic gates, leading to the enhanced performance of computing systems.

***Keywords*—**Low power CMOS, quantum computing, reversible logic gates, full adder, full subtractor, parallel adder/subtractor, basic gates, universal gates.

I. Introduction

MAJOR thrust is being given to the design, implementation, and analysis of logic circuits that are reversible, in research domain. The idea of reversible logic is increasingly employed in the areas of nanotechnology, quantum computing, low power VLSI design, and optical computing. As the complexity in circuit increases, the dissipation of power in the circuit becomes a major challenge in the design. Loss of the information results in dissipation of energy and consumption of power in conventional irreversible logic circuits. It was demonstrated by Landauer in 1961 [1] that heat energy of kT*log2 joules is dissipated for every bit of information lost, where the absolute temperature is represented by T (Kelvin) and k is the Boltzmann's constant respectively. Conversely, it was also shown by Bennet that power dissipated in logic circuits that comprise of logic gates that are reversible is zero [2].

The primary requirement for an 'n' input and 'k' output logic expression to be reversible is that the values of 'n' and 'k' must be equal. In reversible logic design, constant inputs (CI) are the extra inputs considered to fulfil this requirement. Similarly, the additional outputs that are not used further in the computation are called the Garbage Outputs (GO).

Performance of reversible full adder/full subtractor designs using DKG and DKGP gates are compared to other designs in this paper. Reversible full adder/full subtractor are the basic building blocks in arithmetic circuits that are reversible and can be used in the design of parallel adder/subtractor and division circuits. The key parameters viz quantum cost, number of CI, number of reversible gates, computational delay, and GO of the reversible full adder/full subtractor circuits are compared. In Section II, preview of few of the available reversible gates is explained. In Section III, realization of logic gates using reversible DKG and DKGP gates is discussed. In Sections IV and V, the reversible Full adder/full subtractor and parallel adder/subtractor designs are compared respectively, followed by conclusion in Section VI.

II. Preview of Reversible Logic Gates

A few of the numerous reversible gates that are available in literature are highlighted in this section with respect to quantum cost, input and output vectors and are listed in Table I.

III. Realization of Logic Gates Using DKG and DKGP Gates

Both DKG [4] and DKGP [5] gates can work singly as reversible full adder or a full subtractor. But the quantum cost of DKG gate is more than that of DKGP gate. NAND gate cannot be constructed using DKGP gate and NOR gate cannot be constructed using DKG gate using true values of inputs.

A. Reversible DKGP Gate

The 4* 4 reversible DKGP gate [5] can work singly as a reversible full adder or a full subtractor. If logic 0 is given to input A of reversible DKGP gate, it works as a full adder. If logic 1 is given to input A, the reversible gate works as a full subtractor. The DKGP gate and its quantum circuit are shown in Figs. 1 and 2 respectively. From the quantum circuit, the quantum cost of DKGP gate is calculated directly as 15 as it contains 2 positive controlled TG and 5 CNOT gates. It can further be reduced by using optimization techniques.

The DKGP gate can be used as Copy, NOT, EXOR, EXNOR, AND, OR and NOR gates. 2 CI are used and one

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GO is produced. NAND gate cannot be constructed using DKGP gate using true values of inputs.

TABLE I
PREVIEW OF REVERSIBLE GATES

Feynman (FG) [3]: Iv = (X, Y): $O_V = (M, N : M = X, N = X \oplus Y)$	QC=1
Toffoli (TG) [3]: Iv = (X, Y, Z) $O_V = (L, M, N : L = X, M = Y, N = XY \oplus Z)$	QC=5
Fredkin (FRG) [3]: Iv = (X, Y, Z) $O_V = (L, M, N : L = X, M = \overline{X}Y + XZ, N = XY + \overline{X}Z)$	QC=5
Peres (PG) [3]: Iv = (X, Y, Z) $O_V = (I, J, K : I = X, J = X \oplus Y, K = XY \oplus Z)$	QC=4
SRK [4]: Iv = (X, Y, Z) $O_V = (I, J, K : I = X, J = X \oplus Y \oplus Z, K = \overline{X}Y \oplus XZ)$	QC=4
DKG [4]: $I_v = (A, B, C, D), O_v = P, Q, R, S : P = B, Q = \overline{A}C + A\overline{D}, R = (A \oplus B)(C \oplus D) \oplus CD, S = B \oplus C \oplus D$	QC=17
DKGP [5]: Iv = (D, E, F, G) $O_v = (W, X, Y, Z : W = D \oplus F, X = E, Y = E \oplus F \oplus G, Z = D \oplus (D \oplus F)(D \oplus G) \oplus E(F \oplus G))$	QC=15
BVF [6]: Iv(A, B, C, D) $Ov = P, Q, R, S : P = A, Q = A \oplus B, R = C, S = C \oplus D$	QC=2
SV [7]: Iv=(A,B); $Ov = (P = A, Q = \overline{A \oplus B})$	QC=1
TR [8]: $I_v(A, B, C), O_V = P, Q, R : P = A, Q = A \oplus B, R = A\overline{B} \oplus C$	QC=6
PFAG [9]: $I_v = (A, B, C, D), O_v = P, Q, R, S : P = A, Q = A \oplus B, R = A \oplus B \oplus C, S = (A \oplus B)C \oplus AB \oplus D$	QC=8
HNG [10]: I_v= (A, B) $O_v = P, Q, R, S : P = A, Q = B, R = A \oplus B \oplus C, S = (A \oplus B)C \oplus AB \oplus D$	QC=6
OTG [10]: $I_v(A, B, C, D), O_V = P, Q, R, S : P = A, Q = A \oplus B, R = A \oplus B \oplus D, S = (A \oplus B)D \oplus AB \oplus C$	QC=9
TSG [10]: $I_v = (A, B, C, D), O = P, Q, R, S : P = A, Q = \overline{A\overline{C}} \oplus \overline{B}, R = (\overline{A\overline{C}} \oplus \overline{B}) \oplus D, S = (\overline{A\overline{C}} \oplus \overline{B})D \oplus (AB \oplus C)$	QC=17
R GATE [10]: $I_v(A, B, C), O_V = P, Q, R : P = A \oplus B, Q = A, R = \overline{C} \oplus AB$	QC=5

B. Reversible DKG Gate

The 4* 4 reversible DKG gate [4] can also work singly as a reversible full adder or a full subtractor. It works as a full adder or a full subtractor when the value of input A='0' and A='1' respectively. The DKG gate and its quantum circuit are shown in Figs. 3 and 4 respectively. From the quantum circuit, the quantum cost of DKG gate is calculated directly as 17 as it contains 2 positive controlled TG, 1 negative controlled TG, and 4 CNOT gates. It can further be reduced by using optimization techniques.

The DKG gate can be used as Copy, NOT, EXOR, EXNOR, AND, OR and NAND gates. 2 CI are used and one GO is produced. NOR gate cannot be constructed using DKG gate using true values of inputs.

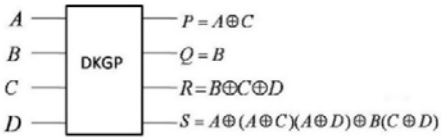


Fig. 1 Reversible DKGP gate

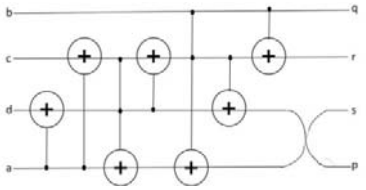


Fig. 2 Quantum circuit of DKGP gate

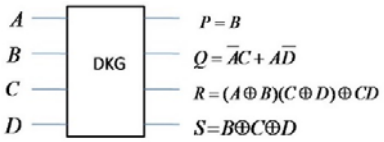


Fig. 3 Reversible DKG gate

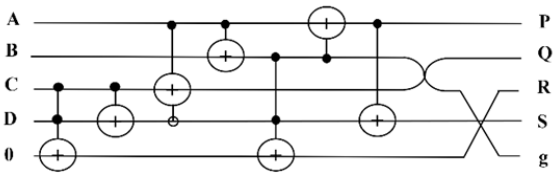


Fig. 4 Quantum circuit of DKG gate

IV. REVERSIBLE FULL ADDER/ SUBTRACTOR

Both reversible DKG and DKGP gates can work singly as reversible full adder/ subtractor by changing the control input from '0' to '1'. But, the quantum cost of DKG gate is more than that of DKGP gate. Few other reversible gates also work as full adder/subtractor.

Reversible full adder/full subtractor has one control input that determines the operation of gate as full adder or full subtractor. This is considered as CI for the gate. Table III provides comparison of all reversible full adder/full subtractor designs.

The number of CI, GO, Reversible gates (RG) used in DKG [4], DKGP [5], FA/FS [11] and Inventive 0 [12] gates are less than that of other designs indicated in row 5 to row 9 of Table III. The Quantum Cost of DKG [4] gate is higher than that of DKGP [5], FA/FS [11], Inventive 0 [12], Design II [14] and Design III [14] gates.

Even though Inventive 0 gate has a quantum cost less than of DKGP and FA/FS gates, the Carry and Borrow are not obtained at the same output line. This gate can be used as an individual full adder or an individual full subtractor. As such, this gate cannot be used in circuits where both adder and subtractor operations are required.

Even though Design II and III [14] have less quantum cost than DKGP and FA/FS gates, the CI, GO and the RG used in the design are greater. Thus, DKGP and FA/FS gates are more efficient compared to other reversible full adder/full subtractor

designs.

TABLE II
REALIZATION OF REVERSIBLE DKG AND DKGP GATES AS DIFFERENT LOGIC GATES (COPY, NOT, AND, OR, EXOR, EXNOR, NAND, NOR)

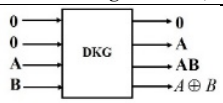
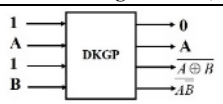
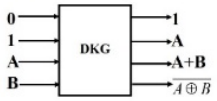
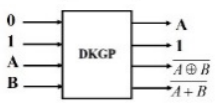
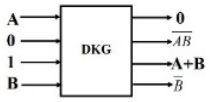
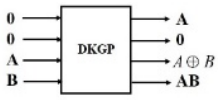
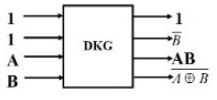
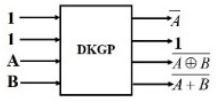
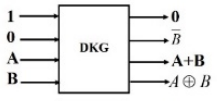
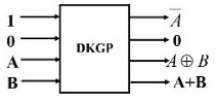
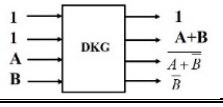
DKG gate: CI=2, GO=1		DKGP gate: CI=2, GO=1	
	Copy AND EXOR		Copy EXNOR
	Copy OR EXNOR		Copy EXNOR NOR
	NAND OR NOT		Copy EXOR AND
	NOT AND EXNOR		NOT EXNOR NOR
	NOT OR EXOR		NOT EXOR OR
	NOT AND EXNOR		

TABLE III
COMPARISON OF REVERSIBLE FULL ADDER/ FULL SUBTRACTORS

Reversible FA/FS	CI	GO	Reversible Gates (RG)	Quantum cost (QC)
DKG [4]	1	2	1	17
DKGP [5]	1	2	1	15
FA/FS [11]	1	2	1	15
Inventive 0 [12]	1	2	1	14
FA/FS-MUX [13]	5	7	8	28
FA/FS-TR [13]	6	8	10	25
FA/FS-Hybrid [13]	3	5	8	21
Design II [14]	2	3	4	14
Design III [14]	2	3	4	10
R Gate [15]	4	5	4	20
FRG [16]	2	3	4	20

V.4-BIT REVERSIBLE PARALLEL ADDER/SUBTRACTOR

Conventionally parallel adder/subtractor circuits are realized using full adder and EXOR gates. If the control input F='0', the circuit works as parallel adder, adding two 4-bit numbers. If the control input F='1', the circuit works as parallel subtractor, subtracting two 4-bit numbers. This is done using 2's complement method.

A reversible parallel adder/subtractor can be designed by replacing EXOR gate with reversible FG Gate and the full adder with any of the RG that work singly as full adder circuits. In literature, many such RG that work singly as full adder are available. PFAG [9], HNG, OTG, TSG [10] gates that work singly as a reversible full adder can be used in place of full adder in parallel adder/subtractor circuit shown in Fig. 5. Reversible full adder can also be constructed using multiple R-Gate [15] or multiple FRG-Gate [16]. Reversible parallel adder/subtractor using HNG gate as full adder is shown in Fig. 6.

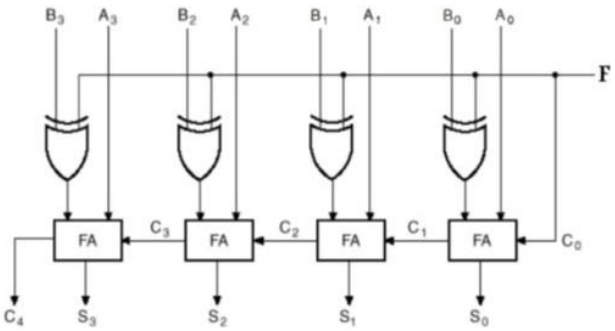


Fig. 5 Conventional 4-bit parallel adder/parallel subtractor circuit

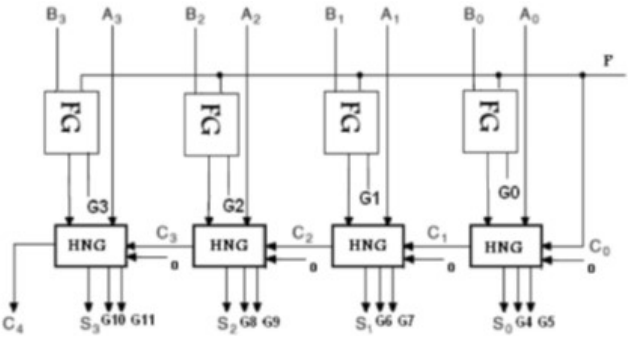


Fig. 6 Reversible parallel adder/subtractor using HNG gate

Other reversible full adders such as PFAG [9], OTG, and TSG [10] gates can be used in place of HNG gate in the parallel adder/subtractor circuit.

Reversible parallel adder/subtractor can also be designed using RG that work singly as full adder/full subtractor dispensing the use of FG Gate.

Full adder/subtractor adds or subtracts two 1-bit inputs along with carry input or borrow input, producing sum/ difference and carry out/borrow out. If two n-bit numbers are to be added or subtracted, 'n' number of full adder/ subtractors are cascaded in such a way that carry out/borrow of one stage is given as carry in/borrow in of next stage so that carry/ borrow is propagated from 1st stage to last stage. This circuit constitutes parallel adder/subtractor where the inputs are applied to all the stages of the circuit simultaneously.

A 4-bit reversible parallel adder/subtractor implemented using the reversible DKG gate is shown in Fig. 7. When the control input A=0, the circuit acts as a parallel adder, thus adding two binary numbers of 4 bits each and produces a 4-bit sum and a carry out. If the control input A=1, the circuit acts as a parallel subtractor, thus subtracting two binary numbers of 4 bits each and produces a 4-bit difference and a borrow out.

Reversible parallel adder/subtractor can similarly be implemented using DKGP and other reversible full adder/full subtractor gates.

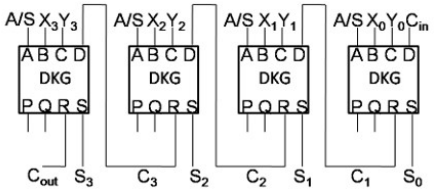


Fig. 7 Reversible 4-bit parallel adder/parallel subtractor circuit

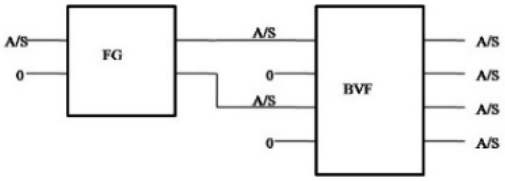


Fig. 8 Fanout circuit to duplicate the control signal A/S for parallel adder/subtractor using full adder/subtractor

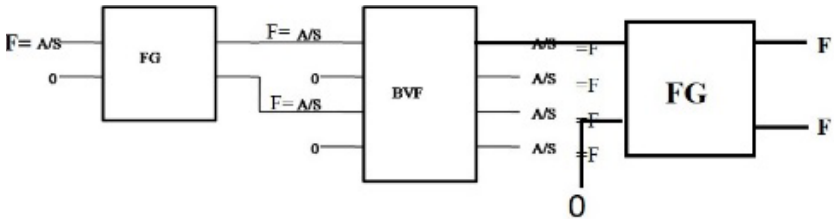


Fig. 9 Fanout circuit to duplicate the control signal F=A/S for parallel adder/subtractor using full adder and FG

Fanouts cannot be used in reversible logic synthesis and feedback from gate outputs to inputs is not permitted. So, fanout in reversible circuits is achieved using additional gates. Adequate care has been taken in this regard by using FG and BVF gates. Fanout circuit to duplicate the control signal A/S for parallel adder/subtractor using full adder/subtractor gates is shown in Fig. 8. Fanout circuit to duplicate the control signal F=A/S for parallel adder/subtractor using full adder and FG gates is shown in Fig. 9. Table IV gives the comparison between different reversible parallel adder/subtractor circuits using reversible full adder/subtractor gates, and, reversible full adders with FG gates. The values of CI, GO, number of RG used, and quantum cost include fanout circuit as well.

The reversible parallel adder/subtractor circuits with least quantum cost of 32 are implemented using HNG gates. But, the CI, GO, and number of RG used are 9, 12 and 11 respectively which are high compared to designs given in rows 1 to 3 of Table IV. Even though quantum cost of circuits using DKG, DKGP and FA/FS are higher, their CI, GO, and number of RG used are 4, 8 and 6 respectively which are lower compared to other designs indicated in Table IV.

The key parameter to enhance the efficiency of the reversible logic design is the reduction in the number of CI bits, number of GO and quantum delay.

In any reversible circuit, the CI and the GO are considered as avoidable overheads and need to be minimized. More number of the I/O pins would be required if the number of CI and the GO are more

The number of GO needs to be minimal for the design to be efficient. This is obtained in the designs using DKG, DKGP and FA/FS gates in parallel adder/subtractor circuit.

TABLE IV
COMPARISON OF REVERSIBLE 4-BIT PARALLEL ADDER/ SUBTRACTORS

Reversible FA/FS	CI	GO	RG	Quantum cost (QC)
DKG [4]	4	8	6	71
DKGP [5]	4	8	6	63
FA/FS [11]	4	8	6	63
FA/FS-MUX [13]	20	28	34	115
FA/FS-TR [13]	24	32	42	103
FA/FS-Hybrid [13]	12	20	34	87
Design II [14]	8	12	18	59
Design III [14]	8	12	18	43
HNG [10]	9	12	11	32
PFAG [9]	9	12	11	40
OTG [10]	9	12	11	44
TSG [10]	9	12	11	76
R Gate [15]	21	24	23	88
FRG [16]	13	16	23	88

VI. CONCLUSION

The design of reversible full adder/subtractor and parallel adder/ subtractor using different RG has been compared. It has been proved that full adder/subtractor and parallel adder/ subtractor design with reversible DKGP and DKG gates has

least CI, GO, and number of RG than other designs at the expense of quantum cost. But the quantum cost of DKG and DKGP gates can be reduced using optimization techniques. Moreover, the reversible DKG and DKGP gates can be used to realize all the logic gates including universal gates which act as backbone for digital and mixed mode Integrated circuit design. Thus, this design forms the basis for a reversible arithmetic circuit design and contributing to no or less power dissipation.

TABLE V
LOGIC GATES REALIZED USING REVERSIBLE DKG GATE

A	B	C	D	Operation
0	0	0	0	Copy, AND, OR, EXOR
0	0	0	1	Copy, NOT, AND, OR, EXOR, EXNOR
0	0	1	0	Copy, NOT, AND, OR, EXOR NAND
0	0	1	1	Copy, NOT, AND, OR, EXOR, EXNOR, NAND
0	1	0	0	Copy, NOT, AND, OR, EXOR, EXNOR
0	1	0	1	Copy, NOT, AND, OR, EXOR, EXNOR
0	1	1	0	Copy, NOT, AND,OR, EXOR, EXNOR, NAND
0	1	1	1	Copy, NOT, OR, EXNOR, NAND
1	0	0	0	Copy, NOT, AND, OR, EXOR
1	0	0	1	Copy, NOT, AND, OR, EXOR
1	0	1	0	Copy, NOT, AND, OR, EXOR, EXNOR, NAND
1	0	1	1	Copy, NOT, OR, EXOR, EXNOR, NAND
1	1	0	0	Copy, NOT, AND, OR, EXOR, EXNOR
1	1	0	1	Copy, NOT, AND, EXOR, EXNOR
1	1	1	0	Copy, NOT, AND, OR, EXOR, EXNOR, NAND
1	1	1	1	Copy, NOT, AND, EXNOR, NAND

TABLE VI
LOGIC GATES REALIZED USING REVERSIBLE DKGP GATE

A	B	C	D	Operation
0	0	0	0	Copy, NOT AND, EXOR
0	0	0	1	Copy, NOT, AND, OR, EXOR, EXNOR
0	0	1	0	Copy, NOT, AND, OR, EXOR, EXNOR
0	0	1	1	Copy, NOT, AND, OR, EXOR, EXNOR
0	1	0	0	Copy, NOT, AND, EXOR, EXNOR, NOR
0	1	0	1	Copy, NOT, AND, EXOR, EXNOR, NOR
0	1	1	0	Copy, NOT, OR, EXOR, EXNOR, NOR
0	1	1	1	Copy, NOT, OR, EXOR, EXNOR, NOR
1	0	0	0	Copy, NOT, AND, OR, EXOR
1	0	0	1	Copy, NOT, AND, OR, EXOR, EXNOR
1	0	1	0	Copy, NOT, AND, OR, EXOR, EXNOR
1	0	1	1	Copy, NOT, OR, EXOR, EXNOR
1	1	0	0	Copy, NOT, EXOR, EXNOR, NOR
1	1	0	1	Copy, NOT, EXOR, EXNOR, NOR
1	1	1	0	Copy, NOT, EXOR, EXNOR, NOR
1	1	1	1	Copy, NOT, EXOR, EXNOR, NOR

REFERENCES

[1] R. Landauer, "Irreversibility and Heat Generation in the Computing Process", IBM J. Research and Development, vol. 3, pp. 183-191, July 1961.
[2] C. H. Bennett, "Logical Reversibility of Computation", IBM J. Research and Development, pp.525-532, November 1973.
[3] Thapliyal, H. and Ranganathan, N., "Design of Reversible Sequential Circuits optimizing Quantum Cost, Delay, and Garbage Outputs", 2010 ACM J. Emerg. Technol. Comput. Syst. 6, 4, Article 14, (December 2010), 31 pages.
[4] D. Krishnaveni, M. Geetha Priya, 'A Novel Design of Reversible Serial and Parallel Adder/ Subtractor' IJEST vol 3,No 3, March 2011, pg 2280-2288.
[5] D. Krishnaveni, M. Geetha Priya, K. Baskaran, "Design of an Efficient Reversible 8x8 Wallace Tree Multiplier" World Applied Sciences Journal 20 (8): 1159-1165, © IDOSI Publications, 2012
[6] H. R. Bhagyalakshmi and M. K. Venkatesha, 'An improved design of a multiplier using reversible logic gates', International Journal of Engineering Science and Technology Vol. 2(8), 2010, 3838-3845
[7] D. Krishnaveni, M. Geetha Priya,'A Novel Reversible EX-NOR SV Gate and Its Application' vol 5, LNNS series, Springer, pg 105-114.
[8] Thapliyal, H. and Ranganathan, N. (2011) A New Design of the Reversible Subtractor Circuit. Proceedings of IEEE International Conference on Nanotechnology, Portland, 15-18 August 2011, 1430-1435.
[9] Md. Saiful Islam,' A Novel Quantum Cost Efficient Reversible Full Adder Gate in Nanotechnology'
[10] M. Surekha,' Efficient Approaches for Designing Quantum Costs of Various Reversible Gates', International Journal of Engineering Studies. ISSN 0975-6469 Volume 9, Number 1 (2017), pp. 57-78
[11] Maii T. Emam, Layle A. A. Elsayed, 'Reversible Full Adder/ Subtractor' Symbolic and Numerical Methods, Modeling and Applications to Circuit Design. (SM2ACD), 2010 XIth International Workshop on. IEEE, 2010
[12] Neeraj Kumar Misra, Mukesh Kumar Kushwaha, Subodh Wairya,' Cost Efficient Design of Reversible Adder Circuits for Low Power Applications', International Journal of Computer Applications (0975 – 8887) Volume 117 – No. 19, May 2015
[13] V.Kamalakannan1, Shilpakala.V2, Ravi. H. N,' Design of Adder/ Subtractor Circuits Based On Reversible Gates', International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering Vol. 2, Issue 8, August 2013, ISSN 2320 – 3765
[14] Rangaraju H G, Venugopal U, Muralidhara K N, Raja K B, "Low Power Reversible Parallel Binary Adder/Subtractor", International Journal of VLSI design & Communication Systems, Vol. 1, No. 3, pp. 23-34, 2010
[15] P. K. Lala, J. P. Parkerson, P. Chakraborty,' Adder Designs using Reversible Logic Gates', WSEAS Transactions on Circuits and Systems, Issue 6, Volume 9, June 2010, pg-369-378
[16] J.W. Bruce, M.A. Thornton, L. Shivakumaraiah, P.S. Kokate, X. Li, 'Efficient Adder Circuits Based on a Conservative Reversible Logic Gate'