WAFER MAPPING OF TOTAL DOSE FAILURE THRESHOLDS IN A BIPOLAR RECESSED FIELD OXIDE TECHNOLOGY

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Abstract

Ionizing radiation failure thresholds were measured across a silicon wafer using 10 KeV x-rays to determine the success of hardened process modifications and to examine wafer level hardness assurance screening techniques. Topological wafer maps of the total dose failure response for Signetics 74F00 circuits are presented.

Introduction

A study was initiated to map the ionizing radiation failure threshold distributions across a silicon wafer and determine process modifications required to increase the total dose hardness of a recessed field oxide technology. To accomplish that, (a) Signetics 74F00 wafers were exposed to 10 KeV x-rays using an Aracor wafer probing station, (b) several channel stop doping variations were evaluated for hardness improvement, and (c) topological variations in total dose hardness were mapped using graphics software.

Background

When advanced commercial bipolar technologies adopted recessed field oxides for speed improvement, serious total dose radiation problems resulted. Devices utilizing these field oxides were found to exhibit total dose failure thresholds of less than 10 KRads(Si) compared to the traditional megaread hard, junction isolated devices of the 1970's [1]. For a given device type, total dose failure thresholds were observed as low as 1-10 KRads(Si) and as high as 1 MRad(Si), depending on variables such as the vendor, process, or layout design. The first-order failure mode, observed in circuits exposed to ionizing radiation, was characterized by large increases in leakage current on device input pins.

For a system designer using off-the-shelf devices, the need for more reliable screening techniques is evident. Poor yield projections for new VLSI technologies are forcing the hardness assurance community to examine their traditional ways of radiation screening. Packaged part sampling techniques, as applied to VLSI technologies, may require sample sizes larger than "process yield economics" can afford. Consequently, wafer level characterization is proposed as an alternative.

When wafer level radiation characterization is implemented by semiconductor vendors as a (pre-packaged) screening technique, significant benefits are possible for both users and vendors. Overall, these benefits are realized by (a) eliminating the cost of packaging die from wafer lots with poor radiation tolerance, (b) allowing immediate feedback to process engineers for process changes that affect the radiation hardness of the technology, and (c)

providing hardness assurance engineers with pre-packaged wafer test data to reduce the amount of testing required on expensive packaged parts.

Investigating wafer level sampling techniques uncovered a new set of challenges. Four key questions surfaced during this research.

1. How uniformly distributed are the radiation induced failure thresholds across a wafer?
2. How uniformly distributed are the radiation induced failure thresholds between wafers of the same processing lot?
3. Are there special cases where data from electrically bad (vendor rejected) die can be used to assess the radiation tolerance of a technology without sacrificing electrically good (vendor accepted) die?
4. Can all radiation induced failure mechanisms be understood well enough to establish a correlation between the response of simple test structures and that of fully functional VLSI devices?

To investigate these questions, a project was initiated to evaluate the uniformity of ionizing radiation induced failure thresholds across a wafer. Identical structures were examined on both good and bad die to correlate the failure mechanism with the full-up circuit's response. "Bad die" were defined as die which were rejected (inked) by the vendor as unacceptable in performance or functionality. Failure distribution wafer maps were generated to permit interpretation of test data and provide a baseline for developing radiation hardened quality assurance sampling techniques.

Identification of Dominant Failure Mechanism

The first-order radiation induced failure mechanism for Signetics 74F00 devices was identified as a large increase in input leakage current (I_{ih}) for pins biased with a positive voltage during irradiation. This was reported in a previous study [1] to be parasitic NMOS transistor interaction between two adjacent transistor buried layers (see Figure 1). At critical points in the circuit layout where interconnect metallization crosses over recessed field oxide separating active transistors, ionizing radiation causes the parasitic NMOS field oxide transistor threshold voltage to degrade from well above 40 volts to less than 5 volts. At that point, normal circuit voltages can exceed the threshold of this NMOS device, causing internal component-to-component leakages.

A convenient method for measuring inversion thresholds from the outside world exists,

because these parasitic NMOS structures are a part of the normal input circuitry. If the square root of the input leakage current (I_{ih}) is plotted versus total dose, the NMOS field oxide transistor inversion threshold can be determined by extrapolation. Using this calculated threshold, the failure of each input can be predicted.

Radiation Induced Failure Mechanism of TTL Input Structure

Cross Sectional Representation

Schematic Representation

Figure 1

Process Hardening Technique

A well-established process hardening technique which increases the p-type channel stop doping under the recessed field oxide was used for this experiment. A three-way split lot of 74F00 wafers was processed by Signetics using their normal (proprietary) baseline process along with two variations, 2.0 E14/cm² and 4.0 E14/cm² boron implant doses in the channel stop area. The effect that this relatively simple processing change had on the total dose response of a wafer was investigated.

Description of Radiation Test System

Radiation testing was conducted using a 10 KeV Aracor x-ray system coupled to an Eagle LSI-4 automatic tester. The Eagle's high-speed digital test head was mounted within three feet of the wafer probe station. Test data was uploaded from the Eagle tester into a VAX 11/780 for storage on magnetic tape and subsequent data analysis using National Bureau of Standards' wafer mapping software [2]. This automated configuration allowed measurements to be made within one second after the radiation exposure.

The Eagle LSI-4 tester was programmed to perform both functional (2 MHz) and DC parametric tests. In addition to input leakage current (I_{ih}) tests, a complete electrical characterization was performed after each irradiation.

The 10 KeV x-ray source delivered a uniform 3-cm diameter beam. A special collimator was used to limit this beam to the area of one individual die site. Scattering effects of the beam on adjacent test die were determined to be negligible.

Before using the 10 KeV source, an experiment was performed to compare the behavior of parts exposed to Cobalt 60 versus those exposed to x-rays. Using similar bias conditions ($V_{cc}=5.0$ V, $V_{in}=5.0$ V), three packaged devices were exposed to Cobalt 60 and seven to 10 KeV x-rays. Package lids were removed from the 10 KeV samples to reduce any dose enhancement effects. The results of Figure 2 showed that 74F00 devices, exposed to 10 KeV x-rays, survived about two times greater dose when compared to data from those exposed to Cobalt 60. This difference was noted after a value of 1.8 for the mass absorption of silicon dioxide to silicon was taken into consideration. The effect is most likely attributed to a higher percentage of electron-hole recombination experienced in parts exposed to 10 KeV x-rays with oxide fields of less than 1.0 E5 volt/cm [3]. Based on the small number of samples used for this experiment, additional work needs to be performed before precise Cobalt 60 versus x-ray correlation factors are determined.

For the actual wafer mapping experiment, devices were biased using worst case DC voltage levels. Four wafers (one baseline, two 2.0 E14/cm², and one 4.0 E14/cm² process) were irradiated, one die at a time. X-ray dose rates were held at 560 Rad(Si)/sec for the baseline and 2.0 E14/cm² wafers, but were increased to 1695 Rad(Si)/sec for the 4.0 E14/cm² wafer. This was done to reduce exposure times because failure level for the 4.0 E14/cm² wafer was over 30 times greater than the others. With respect to testing one wafer at a higher dose rate, previous experiments (Figure 2) indicated that this change in procedure would give failure thresholds which were only slightly less than experienced at the lower rate.

Comparison of Cobalt 60 vs X-Ray Irradiation

Figure 2

Multiple x-ray exposures were used on each die to allow characterization of the device's electrical response to total accumulated dose. The time between each irradiation was kept to less than seven seconds. Each die site was exposed beyond failure before proceeding to the next die on the wafer.

Upon completion of each wafer, data was transferred to a VAX 11/780 for storage and processing. Input leakage current data was plotted as the square root of I_{ih} versus total dose (Figure 3). From these plots, two failure doses were determined: (a) the inversion threshold failure dose from extrapolating the square root of I_{ih} versus dose to zero and (b) the dose for exceeding the 100 μA Signetics data sheet specification limit for I_{ih} . Using National Bureau of Standards' graphics software (STAT2), topological wafer maps were generated to display each of these two failure doses. Also, statistical parameters (sample mean, sample median, standard deviation) were calculated for both good and bad die sites.

Experimental Results

Total dose sensitivities were discovered in all Signetics 74F00 (commercial) devices which utilize recessed field oxides to isolate transistor elements. The total dose failure mechanism was identified as surface inversion in the channel stop area under this field oxide. More than 430 die on four wafers were characterized for their radiation response using the 10 KeV x-ray source.

Radiation Hardened Process Improvement

The experimental channel stop hardening technique proved successful. By increasing the channel stop implant dose from the standard baseline to 4.0 $E14/cm^2$, total dose failure levels were increased over 33 times (from 15 to 500 KRads(SiO_2)). This improvement is illustrated in Figure 3.

Characteristic Plot of Failure Mechanism

Figure 3

The benefit of this hardening approach is limited to the maximum channel stop dose that can be implanted without impacting device yield and performance. On the yield side, the limiting factor is an increase in stacking faults

that grow in the epitaxial layer as channel stop doping is increased. Excessive stacking faults ultimately cause shorted transistors. It has been determined [1] that implanted doses can exceed 1.0 $E15/cm^2$ without significant yield loss. With respect to performance, increasing the channel stop doping level adds capacitance to the collector-substrate junction. This affects the maximum switching speed of the transistors.

Uniformity Across a Wafer

For the single wafer from the baseline process, the two failure distribution maps of Figure 4 indicate that statistical sampling can be used to predict the failure threshold within a range of (+/-) 30% of the computed mean. The results show excellent uniformity and reflect a process that has been in production for several years. Comparing the two maps from the same wafer, the calculated NMOS transistor inversion threshold is seen to track the input current (I_{ih}) failure threshold. This relationship between inversion threshold and input current failure was expected.

Distribution Comparison Between Inversion and Input Current Failure Threshold

Figure 4

A uniform circular pattern, about the center of the wafer, was observed in each map. This inner region contained die which were most sensitive to radiation. It is speculated that this pattern variation was caused by topological changes in (a) epitaxial layer thickness, (b) channel stop implant dose, or (c) parameters associated with the field oxide etch/growth process. All of these process variations directly affect the threshold characteristics of recessed field oxides.

For the wafers with higher doped channel stops, failure distribution maps (Figure 5(b-d)) showed a breakdown of the circular pattern. Even with this pattern breakdown, the overall distribution of failure thresholds still fell within (+/-) 30% of their calculated mean. Although not shown graphically, the inversion threshold distributions for the higher doped wafers continued to track the input current failure thresholds.

Distribution Comparison of Total Dose Failure Levels

Total Dose Input Current Failure Threshold
Wafer 1 - Baseline Process

Figure 5a

Total Dose Input Current Failure Threshold
Wafer 2 - 2.0 E14/cm2 Implant Dose

Figure 5b

Total Dose Input Current Failure Threshold
Wafer 3 - 2.0 E14/cm2 Implant Dose

Figure 5c

Total Dose Input Current Failure Threshold
Wafer 4 - 4.0 E14/cm2 Implant Dose

Figure 5d

(Mean + 2.25 (Sigma)) to (Mean + 3.00 (Sigma))
 (Mean + 1.50 (Sigma)) to (Mean + 2.25 (Sigma))
 (Mean + 0.75 (Sigma)) to (Mean + 1.50 (Sigma))
 Mean to (Mean + 0.75 (Sigma))

(Mean - 0.75 (Sigma)) to Mean
 (Mean - 1.50 (Sigma)) to (Mean - 0.75 (Sigma))
 (Mean - 2.25 (Sigma)) to (Mean - 1.50 (Sigma))
 (Mean - 3.00 (Sigma)) to (Mean - 2.25 (Sigma))

Figure 5

In Figure 5(a-d), each process's distribution was plotted to their statistical mean with maximum/minimum limits at (+/-) three times the calculated standard deviation. A comparison of these wafer maps verified that placement of test structures at specific locations around a wafer would not always predict the worst-case response.

A summary of the radiation data from each wafer is given in Figure 6. Histogram analysis (Figure 7(a-d)) indicates that wafers with higher doped channel stops contain fewer outliers than the baseline. These histograms show that, for all 74F00 wafers tested, the worst-case maximum/minimum failure limit falls within (+/-) 30% of the calculated mean.

Statistical Summary of Failure Thresholds

Total Dose Inversion Threshold

Wafer	Process Variation	Sample Size	Sample Mean	Standard Deviation	Coefficient of Variation
1	Baseline Process	111	7.9 KRad	0.85	10.8%
2	2E14 Impl. Dose	117	65.9 KRad	6.41	9.7%
3	2E14 Impl. Dose	96	66.3 KRad	4.67	7.0%
4	4E14 Impl. Dose	109	176.0 KRad	9.62	5.5%

Total Dose Input Current Failure Threshold

Wafer	Process Variation	Sample Size	Sample Mean	Standard Deviation	Coefficient of Variation
1	Baseline Process	111	15.3 KRad	1.53	10.0%
2	2E14 Impl. Dose	117	135.9 KRad	15.19	11.2%
3	2E14 Impl. Dose	96	134.2 KRad	9.79	6.6%
4	4E14 Impl. Dose	109	501.2 KRad	41.37	8.3%

Figure 6

Distribution Comparison of Total Dose Failure Levels

Histogram Distribution of Total Dose Failure Levels

Figure 7a

Histogram Distribution of Total Dose Failure Levels

Figure 7b

Histogram Distribution of Total Dose Failure Levels

Figure 7c

Histogram Distribution of Total Dose Failure Levels

Figure 7d

-4 : (75.4% (Mean))
 -3 : (80.0% (Mean))
 -2 : (86.7% (Mean))
 -1 : (93.3% (Mean))

1 : (106.7% (Mean))
 2 : (113.3% (Mean))
 3 : (120.0% (Mean))
 4 : (126.6% (Mean))

Figure 7

Uniformity Between Wafers

Another issue addressed in this experiment was wafer-to-wafer uniformity. Two wafers with 2.0 E14/cm2 channel stop doping were used for this evaluation. Each was exposed under identical test conditions (i.e., dose rate, dose levels, and operating bias). A comparison of the failure thresholds is mapped in Figure 8. These plots were generated using the calculated mean with maximum/minimum limits set at (+/-) three times the standard deviation of wafer 2. For the two wafers tested, the statistical means fell within (+/-) 1% of each other. Histogram plots of the data (Figure 7(b-c)) show some difference in the distributions. The standard deviation was almost twice as much for wafer 2 because (a) it had several weak outliers along its right-hand edge and (b) 22% more sites were tested. In contrast, wafer 3 had many sites along its outside edges that were testable.

Testability of Electrically Rejected Devices

Finally, comparisons were performed on inversion thresholds from both good (vendor accepted) and bad (vendor rejected) die. From Figure 9, the mean failure levels compared within 0.4% (best wafer) to 6% (worst wafer). Using vendor rejected die proved successful on this experiment, as the first-order failure mechanism was still observable on the inputs of non-functional devices.

Conclusions

The radiation response of these Signetics 74F00 devices was improved 33 times (to 500 KRad(SiO2)) by increasing the boron doping concentration in the channel stop area (located directly under the recessed field oxide). This process modification was used as an inexpensive technique for obtaining hardened devices from standard commercial processes.

Distribution Comparison Between Two Wafers of the Same Process Variation

Figure 8

Statistical Comparison of Good vs Bad Die

Total Dose Inversion Threshold

Wafer	Process Variation	Die Status	Sample Mean	Standard Deviation	Coefficient of Variation
1	Baseline	Good	7.7 KRad	0.62	8.1%
	Process	Bad	8.0 KRad	1.01	12.5%
2	2E14	Good	65.4 KRad	4.46	6.8%
	Impl. Dose	Bad	66.1 KRad	8.55	12.9%
3	2E14	Good	64.3 KRad	3.07	4.8%
	Impl. Dose	Bad	68.2 KRad	5.33	7.8%
4	4E14	Good	175.4 KRad	8.53	4.9%
	Impl. Dose	Bad	176.1 KRad	10.2	5.8%

Total Dose Input Current Failure Threshold

Wafer	Process Variation	Die Status	Sample Mean	Standard Deviation	Coefficient of Variation
1	Baseline	Good	14.8 KRad	1.01	6.8%
	Process	Bad	15.7 KRad	1.82	11.6%
2	2E14	Good	135.6 KRad	12.1	8.9%
	Impl. Dose	Bad	135.5 KRad	19.0	14.0%
3	2E14	Good	131.0 KRad	6.82	5.2%
	Impl. Dose	Bad	137.4 KRad	9.41	6.8%
4	4E14	Good	501.8 KRad	37.6	7.5%
	Impl. Dose	Bad	500.6 KRad	42.8	8.5%

Figure 9

For all wafers tested, only a single (first-order) failure mechanism (surface inversion of the channel stop area) was observed. For this failure mechanism, sampling electrically "bad" die gave realistic estimates of the failure threshold.

Statistical sampling techniques were shown to be useful for predicting the radiation response across a wafer. By radiation testing simple input structures, Signetics 74F00 wafers can be pre-screened for most requirements. In addition, wafer-to-wafer variations were found to be minimal for the sample size tested.

A problem in correlating the data taken on a 10 KeV x-ray source versus Cobalt 60 was uncovered. The failure threshold for devices exposed to 10 KeV x-rays was a factor of two greater than the threshold experienced using Cobalt 60. In spite of this difference, the x-ray system proved to be an acceptable wafer level screening tool.

Summary

This investigation served as a foundation for developing future VLSI hardness assurance techniques. The data indicated that sampling electrically accepted or rejected die can result in accurate estimates of failure thresholds if the radiation failure mechanism is well understood. The experiment showed that simple measurements of the inversion threshold dose of a parasitic NMOS transistor (in place of irradiating the whole 74F00 circuit) will predict the total dose hardness of the Signetics process. This statement is valid because the total dose failure mode of the Signetics 74F00 process is dependent upon a SINGLE failure mechanism.

Wafer level screening techniques, which irradiate test structures instead of the complex VLSI, have been proposed by some "experts" as an attractive, cost effective means for pre-screening the radiation response of our next generation devices. The study has proven this true for devices with one dominant failure mechanism.

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References

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