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RADIATION-INDUCED INTERFACE TRAPS IN POWER MOSFETS[†]

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Abstract

Methods for estimating radiation-induced interface trap density from the current-voltage (I-V) characteristics of MOSFETs are described and applied to commercially available power MOSFETs. The power MOSFETs show severe degradation on radiation exposure with the effects of positive oxide trapped charge dominating; however, interface trap buildup is significant. The results are compared to experimental measurements available on other technologies.

1. Introduction

There are a number of applications which require that large currents or voltages be controlled or switched efficiently over a wide range of frequencies. Power MOSFETs (metal-oxide-semiconductor field-effect transistors) offer an excellent choice over power bipolar transistors as far as current-handling capability, switching speed, thermal stability, and breakdown voltage are concerned. However, their electrical characteristics are deleteriously altered if exposed to ionizing radiation. The radiation susceptibility of these devices depends on a number of factors including device design, processing details, lithographic steps, and metallization procedure. This is a multi-faceted problem and its every aspect needs to be investigated before the full potential of power MOSFETs in radiation environments can be realized.

The effect of radiation exposure on the operating characteristics of power MOSFETs has been studied by a number of workers over the past few years.[1-10] The dominant effect due to ionizing radiation exposure is the shift in the threshold voltage. Degradation in transconductance, leakage current, and breakdown voltage has also been observed. Drain-source resistance increase has been observed for high-voltage devices exposed to neutrons.[3]

In general, ionizing radiation exposure of MOSFETs results in a buildup of positive trapped charge in the oxide and an increase in the interface trap density at the Si-SiO_2 interface. The effects of positive trapped charge (N_{ot}) buildup has so dominated the measurements of ionizing radiation effects on power MOSFETs that the effects of interface trapped charge (N_{it}) have been ignored. However, any effort to reduce the sensitivity of this class of device to ionizing radiation exposure must include measurement and control of interface trapped charge.[11]

The purpose of this paper is to investigate radiation-induced interface trap density in commercial state-of-the-art power MOSFETs and to compare this response to measurements of interface trap density for both commercial and radiation-hardened integrated circuit MOSFETs. Devices from different manufacturers were examined to illustrate the spread in interface trap density that might be expected from a variety of commercial fabrication techniques. Section 2 describes the analysis techniques used in this work. Section 3 presents the experimental data and estimates of the values of interface trap density. Section 4 discusses these results in view of experimental data available on other technologies.

2. Methods for Estimating Interface Trap Density

Two methods for estimating the radiation-induced interface trap density from the current-voltage characteristics of power MOSFETs have been applied. The methods are: 1) the slope of the subthreshold technique introduced by Van Overstraeten et al.[13]; and 2) the "simple model" approach for the effect of interface and oxide charge on the linear region characteristics of MOSFETs described by Galloway et al.[12]

Shifts in device subthreshold electrical characteristics have been used by several workers to extract values for the radiation-induced oxide trapped charge and the radiation-induced interface traps. Recent work by Winokur et al.,[14] Benedetto and Boesch,[15] and Gaitan and Russell[16] has discussed the measurement of radiation-induced interface traps using methods based on changes in MOSFET subthreshold current characteristics. [Winokur et al.[14] also present a technique for separating MOSFET threshold voltage shifts into components due to interface traps and to trapped oxide charge.]

Another approach to determining the radiation-induced oxide and interface charges was described by Galloway et al.[12] This paper[12] makes assumptions as to the effects of the radiation-induced charge on channel mobility and channel charge and uses these assumptions with the gradual channel approximation. Expressions are derived which relate the radiation-induced interface charge to changes in device transconductance, while changes in both interface and oxide charge are related to threshold voltage shifts. The expressions developed are only valid in the linear region of MOSFET operation. It is assumed that the change in effective mobility due to a radiation-induced increase in interface traps, δN_{it} [Number.cm^{-2}], can be parameterized as:

$$\mu = \frac{\mu_o}{1 + \alpha \delta N_{it}} \ , \tag{1}$$

where the mobility, μ_o, is determined to reflect the device I-V curves before radiation exposure, and α is a constant. This leads to an expression for the change in transconductance in the linear region:

$$\Delta G_m = G_m - G_{mo} = -\left(\frac{\alpha \delta \overline{N}_{it}}{1 + \alpha \delta \overline{N}_{it}}\right) G_{mo} \ , \tag{2}$$

where G_{mo} is the transconductance before radiation exposure and G_m is the transconductance following exposure. The effective radiation-induced density of interface traps (averaged across the channel), $\delta \overline{N}_{it}$, can be calculated if a value for α is known. A value of $(8 \pm 2) \times 10^{-13}$cm^2 for α can be used to fit the data presented by Sexton and Schwank[17] and by Galloway et al.[12] In this work, the assumption is made that this value of α can be used to estimate the radiation-induced change in interface traps in power MOSFETs.

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The presence of interface traps causes the surface potential, ϕ_s, to be less sensitive to changes in the gate voltage. This decreases the slope of the ln (I_d)-V_g characteristics of a MOSFET operating in weak inversion (i.e., the region where the gate voltage is between the flatband voltage and the threshold voltage).[13] The average value of the interface trap density D_{it} [Number.eV^{-1}.cm^{-2}] is related to the slope of the ln (I_d)-V_g:[16]

$$\overline{D}_{it} = \frac{1}{q}\left(\left[\frac{\frac{q}{kT}}{\frac{\partial \ln(I_d)}{\partial V_g}} - 1\right] C_{ox} - C_D\right), \tag{3}$$

where C_{ox} is the gate oxide per unit area, and C_D is the depletion layer capacitance per unit area at $\phi_s = \frac{3}{2}\phi_f$. Here ϕ_f is the Fermi potential under the gate. $\overline{D}_{it}$ represents an average value of the interface trap density, D_{it}, around the surface potential $\phi_s = \frac{3}{2}\phi_f$. The depletion layer capacitance and the Fermi potential are evaluated by the equations:

$$C_D = \sqrt{\frac{q\epsilon_{si}N_B}{2(\phi_s + \frac{kT}{q})}}, \quad \text{and} \quad \phi_f = \frac{kT}{q}\ln\left[\frac{N_B}{n_i}\right]. \tag{4}$$

N_B is the dopant density under the gate of the MOSFET, and n_i is the intrinsic carrier concentration.

In this work, the interface trap density was determined from the slope of the $\ln(I_d)$-V_g characteristics of the devices operating in weak inversion using equation (3). Unlike the "simple model"[12] which yields the change in the effective number of charged interface traps, $\delta\overline{N}_{it}$, the weak inversion measurement gives the density of interface traps, $\overline{D}_{it}$, at a fixed value of surface potential $\frac{3}{2}\phi_f$. For an n-channel transistor with a p-type silicon substrate, $\overline{D}_{it}$ will represent the density of interface traps per unit energy at an energy slightly above the center of the bandgap.

3. Experimental Details

Commercially available nonradiation-hardened power VDMOSFETs (vertical double-diffused MOSFETs) were used. N-channel enhancement-mode devices were obtained from four different manufacturers – devices A, B, C, and D. All devices had equivalent nominal electrical characteristics and were packaged in a TO-204AA style case. These devices are intended as replacement parts for one another with industry part number IRF440 (rated at 500 V). Figure 1 shows a cross section typical of these devices.

The pre-rad current-voltage characteristics from the subthreshold to the saturation region were examined for 12 devices from each manufacturer. Four devices from each manufacturer were selected on the basis of comparable electrical characteristics for radiation testing. The pre-rad observed threshold voltage and

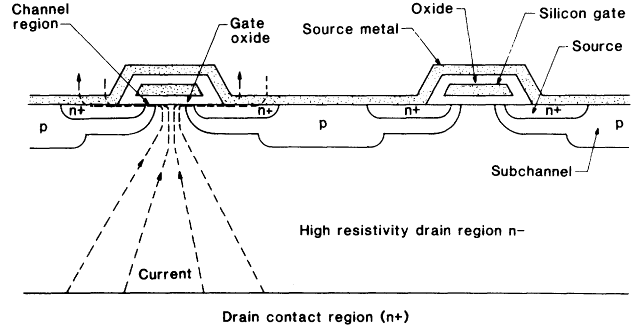

Figure 1: Schematic of a planar vertical double-diffused n-channel power MOSFET.

transconductance values averaged over the set of four devices are given in Table I.

Test devices were irradiated in a water-shielded Cobalt-60 cylindrically symmetrical gamma source at the National Bureau of Standards. Dose rate at the time of this experiment was 0.1203 krad(Si)/sec.

Test devices were biased during radiation exposure by applying +9 V to the gate and grounding all other terminals. The bias voltage was disconnected after the test fixture was removed from the radiation enclosure. Prior to irradiation and after cumulative doses of 25 to 600 krad(Si), the $I_d - V_g$ characteristics were measured at $V_{ds} = 0.05$ V within one hour of radiation exposure.

The threshold voltage was determined by extrapolating the maximum-slope line of the $I_d - V_g$ characteristics in the linear region of device operation to $I_d = 0$, and the transconductance was obtained from the maximum slope.

4. Experimental Results

The $I_d - V_g$ characteristics shown in Figure 2a are typical of the effects of ionizing radiation on the linear region of all of the devices studied. There is a marked shift in the threshold voltage and considerable degradation in the transconductance. The $\ln(I_d) - V_g$ plot shown in Figure 2b allows the effect of radiation on the subthreshold region to be observed. At very low drain currents ($\approx 10^{-12}A$), the measurement of $\ln(I_d)$ versus V_g is limited by instrumentation, fixturing and device leakage.

Figure 3 shows the average shift in the threshold voltage normalized to the pre-rad value for the four device types. The error bars represent one standard deviation about the average shift and show the combined effect of experimental errors and variations from transistor to transistor. Error bars on all of the plots in this paper have a similar meaning. Note that for these n-channel enhancement-mode devices, the threshold shift is as large as 40 V at 500 krad(Si). For hardened n-channel

Table I

Average Pre-Rad V_{th} & G_m Values

Device Type / Parameter	A	B	C	D
Threshold Voltage (V)	3.90 ± 0.10	3.18 ± 0.53	3.19 ± 0.16	3.56 ± 0.21
Transconductance (mho)	$(31.68 \pm 0.87) \times 10^{-3}$	$(41.23 \pm 1.95) \times 10^{-3}$	$(40.09 \pm 0.97) \times 10^{-3}$	$(31.75 \pm 2.36) \times 10^{-3}$

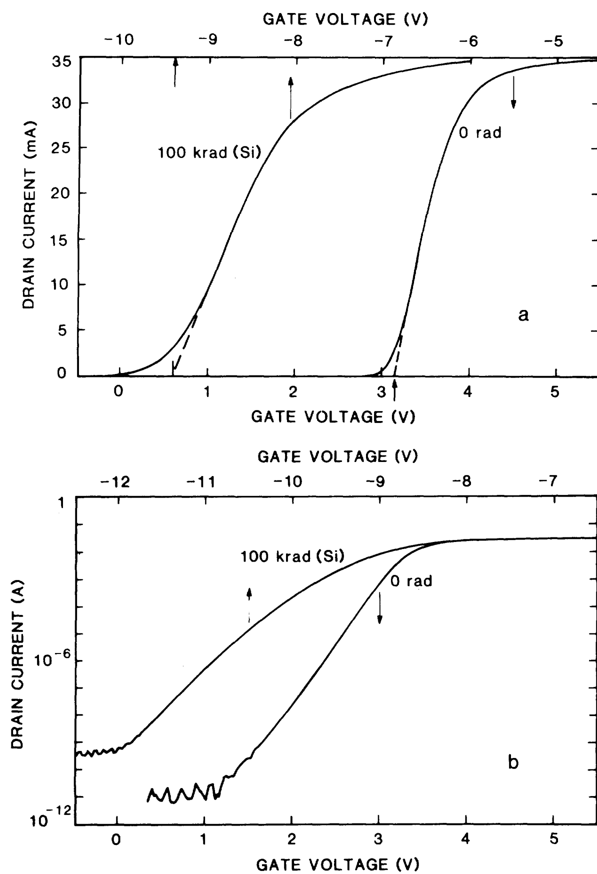

Figure 2: Drain current versus gate voltage at gamma dose of 0 and 100 krad(Si), ($V_{ds} = 0.05V$). Figure 2a is a linear plot emphasizing the linear region of operation. Figure 2b is a log plot illustrating the subthreshold region.

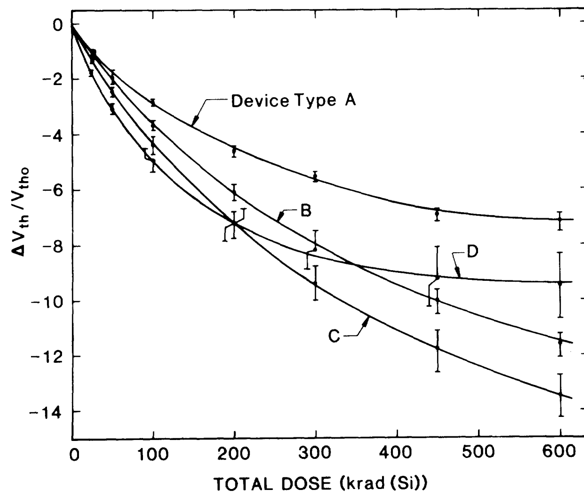

Figure 3: Normalized threshold voltage shift versus total gamma dose for the four device types: A, B, C, and D.

MOSFETs, the threshold shift can be less than 1 V at 500 krad(Si).[16] The data in Figure 3 show no recovery that can be attributed to the generation of interface traps at dose levels up to 600 krad(Si).

Normalized changes in transconductance versus total dose are shown in Figure 4. The normalized change is a useful parameter since it is independent of the resistance due to the drain material. This independence is very important; other-

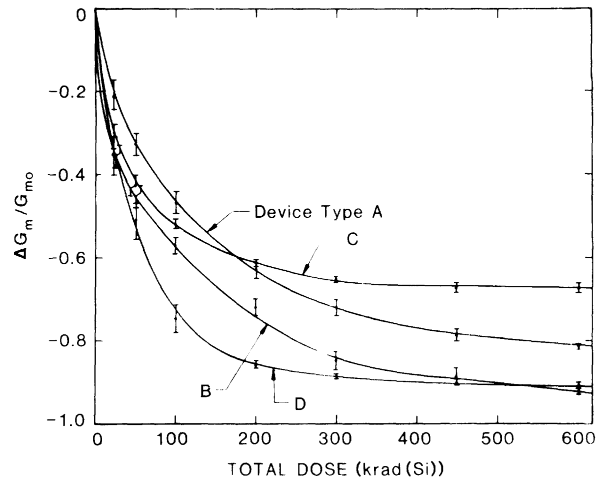

Figure 4: Normalized variation in the transconductance versus total dose for the four device types.

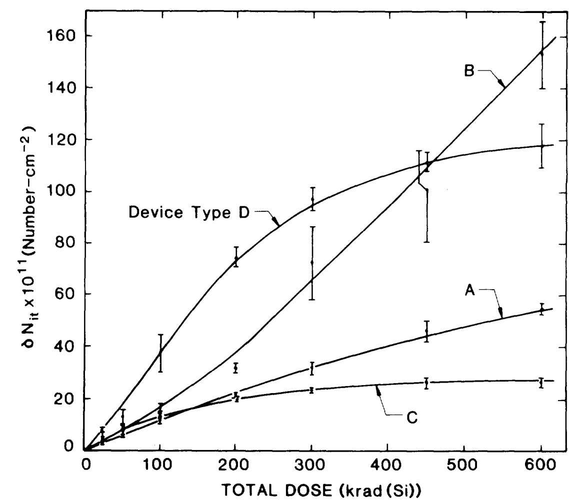

Figure 5: Buildup in the effective interface trap density ($\delta\overline{N}_{it}$ number·cm^{-2}) versus total dose.

wise, equation (2) cannot be used to estimate the interface trap density ($\delta\overline{N}_{it}$). This point is discussed further in Appendix A.

Figure 5 illustrates the buildup of effective interface trap density ($\delta\overline{N}_{it}$) with increasing radiation dose. The interface trap density was calculated using equation (2) and the linear characteristics taking $\alpha = 8 \times 10^{-13}$ cm^2. All device types studied show considerable buildup of interface traps. The variation seen among devices indicates that this buildup depends on the specifics of the commercial fabrication process used by each manufacturer for the gate oxide. Also, note that the value of α selected may not be optimum for the power MOSFET process. However, this estimate is expected to be good within an order of magnitude.

The interface trap density per unit energy ($\overline{D}_{it}$) at $\frac{3}{2}\phi_f$ was estimated using equation (3) and the subthreshold characteristics. Here, N_B was assumed to be 1×10^{15} cm^{-3} and the oxide thickness was taken as 100 nm. These values are expected to be typical for the commercially available power MOSFETs used in this experiment. Change in the interface trap density ($\Delta\overline{D}_{it}$) with total dose estimated by this technique is shown in Figure 6. Again, all device types show a considerable buildup of interface traps using this estimation technique.

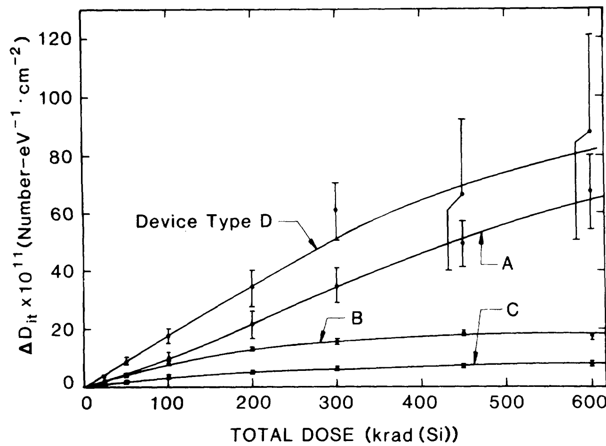

Figure 6: Variation in the average interface trap density ($\Delta\overline{D}_{it}$ number·$eV^{-1} \cdot cm^{-2}$) versus total dose.

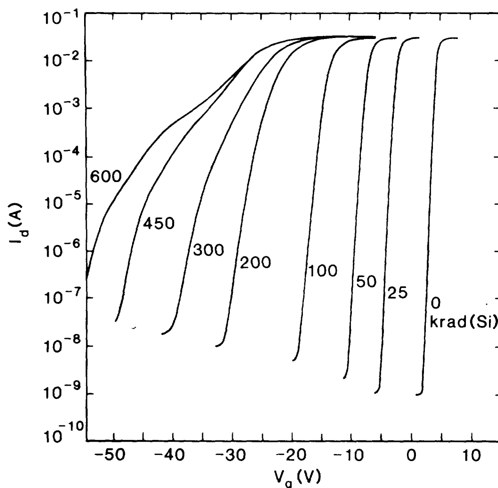

Figure 7: $\ln(I_d)$-V_g characteristics in the subthreshold region at different total dose levels illustrate increasing leakage current with dose, and distortions in the characteristics at high dose levels.

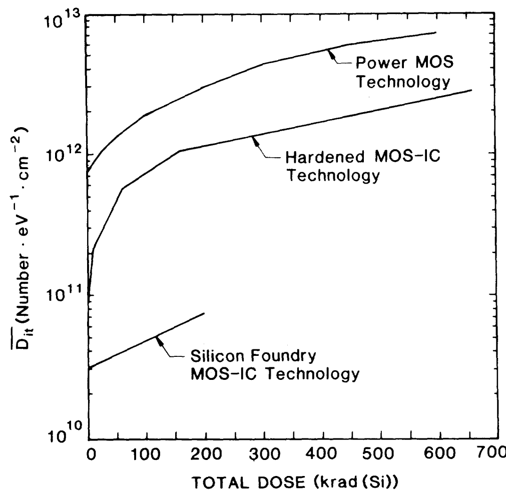

Figure 8: A comparison of the interface trap density ($\overline{D}_{it}$ number·$eV^{-1} \cdot cm^{-2}$) as a function of total dose for the three technologies: silicon foundry MOS IC technology, a previous generation hardened MOS IC technology, and the commercial state-of-the-art power MOSFET technology.

The distortion of device characteristics in the subthreshold region leads to large uncertainties in applying the subthreshold slope technique and may totally invalidate the procedure. For example, the large errors for device type D arise from such distorted characteristics (see Fig. 7). At high dose, either a spatial variation of N_{it} within the many transistor cells of the power MOSFET or a very nonuniform D_{it} within the silicon bandgap leads to this kind of distortion. Also, Figure 7 illustrates the increase of leakage currents with dose typically seen in all device types studied.

5. Discussion and Summary

The threshold voltage shift observed in Figure 3 can be interpreted in terms of oxide and interface trapped charge. The shift to more negative values of this threshold voltage indicates that positive oxide trapped charge is the dominant effect. An earlier report[7] observed that the charge trapping in commercial power MOSFETs was higher, by approximately a factor of 15, than the charge trapping in samples of a rad-hard MOS IC technology. More importantly for this work, the transconductance shift observed (Fig. 4) and the subthreshold behavior of the device types studied suggest a significant buildup of interface trapped charge due to radiation exposure (Figs. 5 and 6). In some hardened technologies, a balance is struck between radiation-generated oxide trapped charge and radiation-generated interface trapped charge to minimize threshold voltage shifts.[16] Even though the buildup of interface trapped charge is very large in comparison to values for other MOS technologies, it is insufficient to compensate for the oxide trapped charge effects.

Figure 8 illustrates the variation of $\overline{D}_{it}$ with dose for a silicon foundry MOS IC technology, a previous generation hardened MOS IC technology,[16] and an average value for all the power MOSFET devices studied here. The estimated density of interface traps is found to be greatest for the power MOSFET technology.

Typical processing sequences for the vertical double-diffused power MOSFET structure used for the devices included in this work can be found in the literature.[19,20] In general, no special processing procedures are applied to minimize either the radiation buildup of oxide trapped charge or the radiation buildup of interface traps. A dry oxidation at 1050°C is typical. The radiation susceptibility of gate oxides prepared under these conditions is not surprising. Procedures such as reported by Winokur et al.[11] and by Naruke et al.[21] must be applied to the processing technology for these devices in order to develop and control a radiation hardened product.

The data presented in this paper indicate that commercial power MOSFETs experience a large buildup in interface trapped charge. This observation has been masked by the dominance of the positive charge trapping. Any effort to improve the radiation resistance of power MOSFET technology to ionizing radiation effects must account for this in the development of appropriate hardened processes.

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7. References

1. W.E. Baker, Jr., The Effects of Radiation on the Characteristics of Power MOSFETs, *Proc. POWERCON 7*, D3-1-6 (1980).
2. S. Rattner, Additional Power VMOS Radiation Effects Studies, *IEEE Trans. Nucl. Sci.* NS-27, 1329-1331 (1980).
3. D.L. Blackburn, T.C. Robbins, and K.F. Galloway, VDMOS Power Transistor Drain-Source Resistance Radiation Dependence, *IEEE Trans. Nucl. Sci.* NS-28, 4354-4359 (1981).
4. W.E. Abare and W.K. Martindale, Dose Rate Tolerant HEXFET Power Supply, *IEEE Trans. Nucl. Sci.* NS-28, 4380-4383 (1981).
5. S.S. Seehra and W.J. Slusark, Jr., The Effects of Operating Conditions on the Radiation Resistance of VDMOS Power FET's, *IEEE Trans. Nucl. Sci.* NS-29, 1559-1563 (1982).
6. H. Volmerange and A.A. Witteles, Radiation Effects on MOS Power Transistors, *IEEE Trans. Nucl. Sci.* NS-29. 1565-1568 (1982).
7. D.L. Blackburn, D.W. Berning, J.M. Benedetto, and K.F. Galloway, Ionizing Radiation Effects on Power MOSFETS During High Speed Switching, *IEEE Trans. Nucl. Sci.* NS-29, 1555-15558 (1982).
8. G.B. Roper and R. Lowis, Development of a Radiation Hard N-Channel Power MOSFET, *IEEE Trans. Nucl. Sci.* NS-30, 4110-4115 (1983).
9. D.L. Blackburn, J.M Benedetto, and K.F. Galloway, The Effect of Ionizing Radiation on the Breakdown Voltage of Power MOSFETs, *IEEE Trans. Nucl. Sci.* NS-30, 4116-4121 (1983).
10. D.M. Jobson Scott, An Investigation into Radiation Induced Second Breakdown in N Channel Power MOSFETs, *IEEE Trans. Nucl. Sci.* NS-31, 1508-1512 (1984).
11. P.S. Winokur, E.B. Errett, D.M. Fleetwood, P.V. Dressendorfer, and D.C. Turpin, Optimizing and Controlling the Radiation Hardness of a Si-Gate CMOS Process, *IEEE Trans. Nucl. Sci.* NS-32, 3954-3960 (1985).
12. K.F. Galloway, M. Gaitan, and T.J. Russell, A Simple Model for Separating Interface and Oxide Charge Effects in MOS Device Characteristics, *IEEE Trans. Nucl. Sci.* NS-31, 1497-1501 (1984).
13. R.J. Van Overstraeten, G.J. Declerck, and P.A. Muls, Theory of the MOS Transistor in Weak Inversion – New Method to Determine the Number of Surface States, *IEEE Trans. Electron Dev.* ED-22, 282-88 (1975).
14. P.S. Winokur, J.R. Schwank, P.J. McWhorter, P.V. Dressendorfer, and D.C. Turpin, Correlating the Radiation Response of MOS Capacitors and Transistors, *IEEE Trans. Nucl. Sci.* NS-31, 1453-1460 (1984).
15. J.M. Benedetto and H.E. Boesch, Jr., MOSFET and MOS Capacitor Response to Ionizing Radiation, *IEEE Trans. Nucl. Sci.* NS-31, 1461-1466 (1984).
16. M. Gaitan and T.J. Russell, Measurement of Radiation Induced Interface Traps Using MOSFETs, *IEEE Trans. Nucl. Sci.* NS-31, 1256-1260 (1984).
17. F.W. Sexton and J.R. Schwank, Correlation of Radiation Effects in Test Transistors and Integrated Circuits, *IEEE Trans. Nucl. Sci.* NS-32, 3975-3981 (1985).
18. S.M. Sze, *Physics of Semiconductor Devices*, 2nd ed., John Wiley & Sons, New York, NY (1981), p. 440.
19. P. Rossel, Power M.O.S. Devices, *Microelectronics and Reliability*, 24, 339-366 (1984).
20. B.J. Baliga, Silicon Power Field Controlled Devices and Integrated Circuits, *Silicon Integrated Circuits, Part B*, Applied Solid State Science, Supplement 2, Dawon Kahng, Editor, Academic Press, New York (1981), pp. 109-274.
21. K. Naruke, M. Yoshida, K. Maeguchi, and H. Tango, Radiation-Induced Interface States of Poly-Si Gate MOS Capacitors Using Low Temperature Gate Oxidation, *IEEE Trans. Nucl. Sci.* NS-30, 4054-4058 (1983).

Appendix A

Transconductance in equation (2) refers to the channel transconductance at a constant voltage across the channel. But the observed transconductance is calculated at a fixed drain-source voltage. The constant drain-source voltage, being the sum of the voltage drops across the channel and the series resistance due to the drain material, does not permit the voltage across the channel to remain constant as the gate voltage is increased. Consequently, the observed value of the transconductance is not the same as the channel transconductance. However, the derivation given below shows that equation (2) is still valid for the purpose of calculating the interface trap density even after replacing the channel transconductance by the observed one.

Figure A1 represents a simplified dc circuit for the power MOSFET. Here, R_{ch} refers to the channel resistance and R_d, the series resistance of the drain material. V_{ch} denotes the voltage across the channel and V_{ds}, the drain-source voltage.

Using the expression for the drain current[18]

$$I_d = \beta(V_g - V_{th})V_{ch}, \qquad (A1)$$

the channel and the observed transconductances can be written as:

$$G_m = \left(\frac{\delta I_d}{\delta V_g}\right)_{V_{ch}}, \qquad (A2)$$

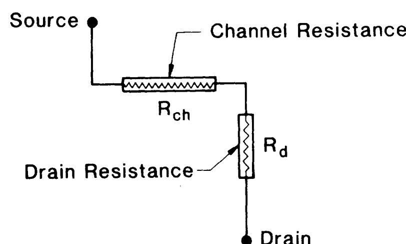

Figure A-1: A simplified equivalent dc circuit for the power MOSFET. Here R_{ch} and R_d refer to the channel resistance and the resistance of the drain material, respectively.

$$(G_m)_{obs} = \left(\frac{\delta I_d}{\delta V_g}\right)_{V_d} = \beta V_{ch} + \beta(V_g - V_{th})\left(\frac{\delta V_{ch}}{\delta V_g}\right)_{V_d}. \quad (A3)$$

Since

$$V_{ch} = V_d - I_d R_d, \quad (A4)$$

one gets

$$\left(\frac{\delta V_{ch}}{\delta V_g}\right)_{V_d} = -\left(\frac{\delta I_d}{\delta V_g}\right)_{V_d} R_d. \quad (A5)$$

From equations (A3), (A4), and (A5), we can write

$$G_m = (G_m)_{obs}\left[1 + \left(\frac{I_d}{V_d - I_d R_d}\right) R_d\right], \quad (A6)$$

which leads to

$$\frac{\Delta G_m}{G_{mo}} = \frac{(\Delta G_m)_{obs}}{(G_{mo})_{obs}}, \quad (A7)$$

at any value of I_d in the linear region.