Temperature Dependence of Transient Electron Radiation
Upset in TTL NAND Gates*

by

T. F. Leedy

National Bureau of Standards

and

G. F. McLane and G. C. Guenzler

Naval Research Laboratory

Abstract

The temperature dependence of transient upset caused by a 40-MeV electron flux was investigated for junction-isolated gold-doped and nongold-doped TTL NAND gate devices in the temperature range from 20 to 125°C. Data for five devices are presented. Over this temperature range, the dose rate required to upset the logical 1 and logical 0 output levels of the gate increased by a factor of between 2 and 3 for the gold-doped devices, but remained essentially constant for the nongold-doped (Schottky) devices. Schottky-clamped devices are not gold-doped, and the gold-doped devices did not employ Schottky clamps. A correlation was observed between the temperature dependence of the upset dose rate and the collector-substrate depletion width as determined from capacitance measurements for both device types. It is proposed that nearly all of the upset photocurrent for gold-doped devices is generated in the collector-substrate depletion region and that variations in the depletion width with temperature cause the observed results.

Key Words: Digital integrated circuits; dose-rate effects; electron irradiation effects; radiation hardness; radiation upset; semiconductor devices; transistor-transistor logic.

Introduction

The effect of temperature upon the transient radiation susceptibility of semiconductor devices is of interest to designers of digital logic systems which must withstand a nuclear radiation environment. In this study, the transient high energy electron radiation-induced upset of gold-doped and nongold-doped (Schottky) 7400 transistor-transistor logic (TTL) NAND gates was investigated over a temperature range from 20 to 125°C for 1- μ s, 40-MeV LINAC electron pulses [1]. The dose rate required for upset (i.e., a change in logic level) increases with temperature by a factor between 2 and 3 over this temperature range for the gold-doped devices and remains essentially constant for the Schottky devices which are not gold-doped.

Upset is induced by radiation in junction-isolated integrated circuits as a result of extraneous currents (or photocurrents) generated at the p - n junctions of the circuit elements. Photocurrents are produced by carriers photogenerated in the junction depletion regions and by minority carriers photogenerated in the surrounding field-free regions which diffuse to the depletion

regions. The relative magnitudes of the component of photocurrent produced in the depletion region and the component resulting from diffusion to the depletion region depend upon the details of the process employed in the fabrication of the TTL circuit. This is because the depletion region volume and the minority carrier lifetime, and thus diffusion length, depend upon these processes.

A cross section of a typical gold-doped TTL component transistor is shown in figure 1. Notice that the largest area p - n junction is between the collector and substrate regions. In normal circuit operation, this p - n junction is always reverse biased. An estimate of the extent of the collector-substrate depletion region of the transistor is shown by the dashed lines in this figure.

Experimental Procedure and Results

Both Schottky and gold-doped dual in-line integrated circuit packages were mounted on a temperature-controlled stage such that each device could be independently exposed to the LINAC electron flux. The temperature of the stage was controlled to $\pm 0.5^\circ\text{C}$ during the exposure of the devices. The dose rate given to the circuit was varied by positioning the entire test fixture on a table that allowed it to be moved over a 200-cm distance along the axis of the electron beam. This arrangement permitted the dose rate to be varied over a range of 60:1 for any given set of LINAC operating conditions. The beam uniformity was determined to be 6 percent at a dose rate of 3×10^9 rad/s. A similar uniformity is expected at other dose rates.

The dose rate of the electron pulse was monitored by a pin diode mounted near the circuit under test. The photocurrent response of the pin diode was displayed on one channel of a dual-channel oscilloscope. The other channel displayed the output voltage of the TTL circuit after the signal was conditioned by a line-driver circuit located in the test fixture. Calibration of the dose-rate response of the pin diode was performed by integrating the current pulse from the diode. The integral was then correlated with the total dose as determined by calcium fluoride thermoluminescent dosimeters (TLD). The accuracy of the dosimetry was estimated to be 20 percent.

The output voltage levels for TTL circuits for a logical 0 (low) and a logical 1 (high) are designated as V_{0l} and V_{0h} , respectively. The permis-

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sible ranges of these levels by standard TTL design rules are [2]:

$$0 \text{ V} < V_{01} < 0.4 \text{ V} \quad (\text{For logical 0}) \\ \text{and} \\ 2.4 \text{ V} < V_{oh} < V_{cc} \quad (\text{For logical 1}),$$

where V_{cc} is the supply voltage to the circuit which was 5.0 V for these tests. The test device was subjected to incrementally higher dose rates until a transient upset was recorded. This point was defined to be that at which the output voltage during the exposure varied beyond the permissible range of either V_{01} or V_{oh} as specified by the manufacturer. The output voltage was initially set by applying the worst-case input voltage to the inputs of the gate. The worst-case input voltage for a logical 0 output of an NAND gate is the lowest value of input voltage permitted by TTL design rules (2.0 V) for a logical 0 output. Likewise, the worst-case input voltage to produce a logical 1 output is the highest value of input voltage permitted (0.8 V) for a logical 1 output.

Figure 2 shows typical oscilloscope traces of the upset of the logical 1 and 0 output voltages of a gold-doped device (upper traces), along with the simultaneous outputs of the dose-rate monitoring diode (lower traces). Similar oscilloscope traces were observed for the nongold-doped devices. Notice that the photographs show that for a device in the logical 1 state, the upset is a relatively smooth voltage transient, while for the logical 0 state the upset is characterized by many sharp excursions of approximately 50-ns duration.

The temperature dependence of the measured threshold dose rate for upset for both the logical 1 and the logical 0 output states is shown in figure 3. Over the temperature range of 20 to 125°C, the dose rate required to upset a gold-doped device increased by a factor between 2 and 3, while the dose rate required for upset of nongold-doped (Schottky) devices was essentially constant.

The temperature dependence of the logical 0 and 1 dose-rate upset levels were also measured for several low-power Schottky devices. The results were similar to the standard Schottky device curves of figures 3a and 3b, where dose-rate upset levels were found to be relatively constant with temperature. However, the dose-rate upset level magnitudes for the low-power Schottky devices were approximately an order of magnitude lower than for the standard Schottky devices. This is to be expected since the resistance values of the low-power devices are an order of magnitude larger than for the standard devices; normal circuit currents would be correspondingly an order of magnitude smaller than for the standard devices.

Circuit Photocurrents

The electrical schematics for both the gold-doped and the Schottky NAND gates are shown in figures 4a and 4b, respectively. They are similar except for the inclusion of two additional transistors,

Q3A and Q4A, in the Schottky device to increase the output drive capability of this circuit. Schottky transistors consist of an n - p - n transistor with a Schottky diode in parallel with the collector-base junction. This arrangement prevents the Schottky transistor from saturating while in the "on" state and reduces the turn-off time. Transistor saturation would result in a relatively long turn-off time. In the standard TTL gate, gold doping is used to reduce the carrier recombination time, τ , and therefore turn-off time. Gold doping also reduces the carrier diffusion length, L , since $L = \sqrt{D\tau}$ where D is the diffusion constant. Both gold-doped and Schottky devices are available in "open-collector" versions for specialized circuit applications. These gates perform the same logical function as discussed previously. They differ in that they lack the transistors and associated "pull-up" circuitry to supply current into the output. Unless indicated otherwise, the discussion below pertains to normal (i.e., not open-collector) NAND gates.

The logical 1 output state of both the gold-doped and Schottky TTL NAND gates results when at least one input is less than 0.8 V, causing the input transistor Q1 to be in its on state. Under this condition transistors Q2 and Q4 will be off, transistor Q3 will be on and the output voltage, V_{oh} , will be approximately 3.6 V. The dominant photocurrent produced during radiation is that generated at the collector-substrate junction of transistor Q2. It was observed for both gold-doped and Schottky gates that the logical 1 output of the gate continuously decreased from its nominal value of 3.6 V before irradiation to 2.4 V during the irradiation in nearly direct proportion to the dose rate of the radiation pulse. The primary photocurrent generated in the collector of Q2 is proportional to dose rate. This photocurrent flows through resistor R2 and causes a voltage decrease at the base of Q3 in proportion to the dose rate. This voltage decrease causes a decrease in voltage at the output of the gate.

The logical 0 output state of the NAND gate results when both input voltages are greater than 2.0 V. This causes the base-emitter and base-collector junctions of Q1 to be reverse and forward biased, respectively. Transistor Q1 now operates in its inverse mode, with its collector supplying current to the base of Q2. Under these conditions Q3 is off, Q4 is on, and the output voltage is approximately 0.2 to 0.4 V. The logical 0 state upset occurs at a dose rate for which the current supplied by the collector of transistor Q1 to the base of transistor Q2 is reduced sufficiently to begin switching it off, thus causing an abrupt upset, as shown in figure 2b. Below this critical dose rate, transistor Q2 remains on, and the output of the circuit remains in the logical 0 state.

Radiation-induced photocurrents are generated in the depletion and diffusion regions of p - n junctions in proportion to the volumes of these regions and the dose rate. If the carrier recombination times are short compared to the radiation

pulse width, junction primary photocurrent, I_{pp} , in amperes is given by [3]:

$$I_{pp} = qK_g \dot{V} = q K_g \dot{V} (W + L_n + L_p) A, \quad (1)$$

where q (electronic charge)

$= 1.6 \times 10^{-19}$ coulombs,

K_g (generation constant for Si)

$= 4.2 \times 10^{13}$ electron-hole pairs/cm³-rad,

$\dot{V}$ = radiation dose rate (rad(Si)/s),

V = effective generation volume (cm³),

W = depletion width (cm),

L_n = diffusion length for electrons on p -type side (cm),

L_p = diffusion length for holes on n -type side (cm), and

A = area of junction (cm²).

An estimate of the temperature dependence of minority carrier diffusion length, and therefore the diffusion component of I_{pp} , can be obtained by using the Einstein relationship in the equation for diffusion length.

$$L = \sqrt{D\tau} = \sqrt{\frac{kT\mu\tau}{q}}, \text{ cm}$$

where D = diffusion coefficient (cm²/s),

τ = minority carrier lifetime (s), and

μ = minority carrier mobility (cm²/V·s).

k = Boltzmann constant, (8.62×10^{-5} eV/K).

The temperature dependence of hole mobility [4] and lifetime [5] in gold-doped silicon have been reported as proportional to $T^{-1.8}$ and $T^{3.5}$, respectively, where T is the Kelvin temperature. Thus, the temperature dependence of the hole diffusion length varies as $T^{1.35}$. Similarly, for electrons, the carrier mobility and lifetime are proportional to $T^{-1.8}$ and $T^{2.0}$, respectively. The temperature dependence of the electron diffusion length varies as $T^{0.6}$.

Therefore, theory predicts that diffusion lengths, and hence diffusion photocurrents, should increase with temperature, which would tend to cause upset dose rates to decrease with temperature. Since this is opposite to what was observed experimentally, it can be concluded that the major portion of the photocurrent is not due to the diffusion currents but is due to generation currents produced in the depletion region of the gold-doped device.

Consider now the depletion region component of the photocurrent. The depletion width of an abrupt p - n junction, assuming complete ionization of all donors and acceptors, can be calculated as [6]:

$$W = \sqrt{\frac{2\epsilon}{q} \frac{N_A + N_D}{N_A N_D}} (V + \phi), \text{ cm} \quad (2)$$

where ϵ = permittivity of silicon = 1.03×10^{-12} farads/cm,

N_A = acceptor concentration in p -type region (cm⁻³),

N_D = donor concentration in n -type region (cm⁻³),

V = applied reverse junction voltage (V),

ϕ = equilibrium junction potential (V),

$$\phi = \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2}, \text{ and}$$

$$n_i = \text{intrinsic carrier density (cm}^{-3}\text{)}.$$

The primary photocurrent generated within the depletion region is expected to be proportional to the depletion width. From the device geometry doping concentrations and applied junction voltages, it is possible to calculate the depletion region photocurrents for a given dose rate. Consider the case for the room temperature logical 1 upset for the gold-doped device, where upset is produced by the photocurrent in the collector of transistor Q2, as shown in figure 4a, through resistor R2. The area of the collector-substrate junction was determined from photomicrographs to be 7500 μm^2 . The acceptor concentration, N_A , of the substrate is approximately 1×10^{15} cm⁻³, and collector region donor concentration, N_D , is approximately 2×10^{15} cm⁻³. Between the output terminal of the gate and the collector of transistor Q2 are two forward-biased diodes, D3, and the base-emitter junction of Q3. The collector voltage of Q2 is thus approximately twice the forward voltage drop of a diode (0.72 V) plus the output voltage of the gate. Thus, the collector-substrate voltage of Q2 for the logical 1 upset level (2.4 V) is 3.8 V. The collector depletion region volume of Q2 when the output of the gate is 2.4 V (the logical 1 voltage upset level) is 2.19×10^{-8} cm³. The dose-rate level for the transient upset shown in figure 2a is 2.5×10^9 rad/s. From eq (1), the primary photocurrent in the collector circuit of Q2 is then 0.367 mA. The negative voltage upset pulse produced by this photocurrent flowing through R2 is

$$V_{out} = 3.67 \times 10^{-4} \text{ A} \times 1.6 \times 10^3 \Omega = 0.6 \text{ V}.$$

This voltage drop is approximately one-half the measured upset voltage change of 1.2 V observed during a logical 1 upset.

This underestimation in the change in output voltage may be attributed to several uncertainties of values in the calculations above. Most significantly, accurate estimates of impurity concentrations of the junctions are difficult to obtain. Errors in the estimates of the impurity concentrations affect the result of the calculation of depletion width. An additional source of uncertainty is the difference in area of the p - n junction that generates photocurrents as opposed to the geometrical junction area determined from photomicrographs. Finally, the resistance values of the diffused resistors used in TTL circuits may typically have 20 percent tolerance limits. Errors in the estimates of these fabrication parameters along with the 20 percent uncertainty in dosimetry will affect the value of the calculated upset voltage shown above.

Comparison of the dose rate required for transient upset between Schottky and gold-doped devices also requires a knowledge of the fabrication parameters. For example, the collector-substrate areas of transistors Q1 and Q2 were approximately 40 and 10 percent smaller, respectively, for the Schottky devices than for the gold-doped devices. Resistors R1 and R2 have a

smaller value in the Schottky devices than for the gold-doped devices. These differences would suggest that for a given photocurrent, the dose rate required for upset would be higher for Schottky devices than for gold-doped devices. However, there may be large diffusion photocurrents present in Schottky devices because of the longer lifetime. This tends to lower the dose rate required for upset of these devices compared to that required for a gold-doped device at room temperature [7]. Theoretically, the diffusion length and diffusion photocurrent should increase with temperature for nongold-doped devices [8]. However, an increase in photocurrent with temperature was not observed experimentally.

Temperature Effects

To determine the temperature dependence of the depletion width, the capacitance of the output collector-substrate junction of both gold-doped and Schottky open-collector gates was measured as a function of voltage and temperature. All capacitance measurements were made at 1 MHz. Open-collector devices, as indicated in figure 4, were used in this measurement to eliminate interferences from the pull-up portion of the circuit. The capacitance was measured between the output pin of the circuit and the ground or substrate pin. All other pins of the circuit were connected to the ground pin. The total measured collector-substrate capacitance, C_m , consisted of the collector-substrate junction capacitance, C_{CS} , in parallel with a parasitic capacitance, C_p . The parasitic capacitance should not be dependent on voltage or temperature since it represents the capacitance associated with the external circuit, the metallization, and bonding wires. Since the collector-substrate and the parasitic capacitances are in parallel,

$$C_m = C_{CS} + C_p \text{ (farads)} . \quad (3)$$

This may be written as

$$C_m = \frac{\epsilon A_{CS}}{W_{CS}} + C_p \quad (4)$$

$$= A_{CS} \sqrt{\frac{\epsilon q N_A N_D}{2(N_A + N_D)}} (V + \phi)^{-1/2} + C_p ,$$

where A_{CS} = area of collector-substrate junction (cm^2) and

W_{CS} = width of the collector-substrate depletion layer (cm).

The value of C_p can be determined by extrapolating the total measured capacitance-voltage curves, as shown in figure 5, until they intersect the ordinate. By the extrapolated data shown in figure 5, the parasitic capacitance of the collector-substrate junction of the output transistor of the gold-doped and Schottky gate devices were determined to be 3.8 and 3.2 pF, respectively. Figure 6 is a plot of the collector-substrate junction capacitances of these transistors at 5.0-V reverse bias as a function of temperature. This figure shows that the capacitance of the collector-substrate junction of the gold-doped devices increases with increasing temperature while the capacitance of a

comparable junction in the Schottky devices remains essentially constant.

The temperature dependence of the capacitance of both the Schottky and gold-doped devices shown in figure 6 may be explained as follows. The junction capacitance is inversely proportional to the collector-substrate junction width, W_{CS} , which is given in eq (2). The dielectric constant of silicon is not strongly dependent on temperature, so that if the applied voltage is much greater than the equilibrium junction potential, ϕ , and the impurity levels are completely ionized, the junction width in the devices is expected to be independent of temperature. This is consistent with the Schottky data presented for the devices in figure 6 for which the capacitance is not dependent upon temperature. Collins *et al.* [4] have found that for gold doping concentrations comparable to the shallow dopant concentrations, carrier concentrations increase with temperature. Under these conditions, the width of the depletion region is expected to decrease with temperature. Thus, the capacitance should increase with temperature, which is consistent with the capacitance measurements shown in figure 6 for gold-doped TTL devices.

A direct observation of the change in photocurrent collection volume as a function of temperature was made using the electron-beam-induced-current (EBIC) technique [10]. The intersection of the collector-isolation junction with the surface of the silicon devices was exposed to a 15-keV electron beam in a scanning electron microscope. The photocurrent generated at the junction was measured as a function of electron-beam position. In this manner, a detailed analysis of the origins of the photocurrents could be made. The photocurrent generated at the junction was amplified and plotted as a function of beam position across the junction. Figure 7 shows the photocurrent profile at the collector-substrate junction of a gold-doped open-collector gate with zero applied bias voltage. The decrease of the effective photocurrent generation width at the silicon surface was estimated to be approximately 0.5 μm for the temperature change of 20 to 100°C. The range of 15-keV electrons in silicon is approximately 1.8 μm . Thus, the photocurrent generation volume is near the surface of the collector-isolation junction. The concentration of the isolation diffusion is greatest at the surface, and consequently the depletion width is narrowest at the point where the photocurrent profile was obtained. It also would be expected that the temperature dependence of photocurrent generation will be less. By contrast, 40-MeV electrons from the LINAC have sufficient energy to produce photocurrents throughout the collector-substrate depletion volume. Figure 8 shows the EBIC signal from a Schottky device at these two temperatures and zero applied bias voltage. These plots show negligible change in effective collection width over a temperature range of 20 to 100°C.

These results suggest that the depletion photocurrents at any given dose rate for gold-doped devices should decrease with temperature and, for Schottky devices, should be temperature indepen-

dent. This is consistent with the logical 1 and 0 dose-rate upset temperature dependence shown in figure 2.

Johnston *et al.* [9] measured transient upset levels in the temperature range of -50 to 125°C for gold-doped TTL gates and obtained results similar to those reported here. However, they were not able to correlate their results with temperature-dependent capacitance measurements, probably because their measured total capacitance is composed of the unresolved sum of junction-depletion capacitance and the parasitic capacitance. The present correlation was observed when these two components of the capacitance were separated. The relatively small temperature-dependent capacitance changes of the junction are easily masked by the parasitic capacitance.

Conclusion

The temperature sensitivity of transistor-transistor logic circuits to 40-MeV electron radiation was investigated over a temperature range of 20 to 125°C. The upset threshold dose rate for gold-doped circuits was found to increase by a factor of approximately 2 to 3 over this temperature range. Devices which were not gold-doped exhibited an upset threshold dose rate that was independent of temperature. A correlation between the temperature dependence of the radiation threshold and collector-substrate junction capacitance indicates that the active photocurrent generation volume decreases with increasing temperature in the gold-doped devices. Direct observation of EBIC photocurrents as a function of position and temperature also indicates a decrease in the effective photocurrent generation volume. This decrease was not observed for nongold-doped devices.

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Figure 1. A cross section of a typical gold-doped TTL component transistor.

- a. Upper trace: The logical 1 output voltage upset pulse at a dose rate of 2.5×10^8 rad(Si)/s. Transient upset occurs when the output of the gate is less than 2.4 V. Lower trace: Corresponding output voltage pulse from the dose-rate monitoring *pin* diode.

- b. Upper trace: The logical 0 output voltage upset pulse at a dose rate of 2.0×10^9 rad(Si)/s. Transient upset occurs when the output of the gate exceeds 0.4 V. Lower trace: Corresponding output voltage pulse from the dose-rate monitoring *pin* diode. Time scale is 500 ns/division.

Figure 2. Oscilloscope photographs of transient upset for a gold-doped device at 20°C.

- a. Transient upset in the logical 1 state.

- b. Transient upset in the logical 0 state.

Figure 3. The temperature dependence of the measured threshold dose rate for transient upset. Data for three nongold-doped and two gold-doped devices are shown.

a. A 7400 gold-doped NAND gate; a 7405 open-collector version.

b. A 74S00 Schottky-clamped NAND gate; a 74S03 open-collector version. The designation for a transistor with a Schottky-clamp diode is shown in inset.

Figure 4. Electrical schematics of TTL NAND gates.

a. Capacitance of the gold-doped transistor. Measurements were made at the external terminal of the gate on an open-collector version of 7400 gate.

b. Capacitance of the nongold-doped (Schottky) transistor. Measurements were made at the external terminal of the gate on an open-collector Schottky 74S03 gate.

Figure 5. Capacitance of the collector-substrate junction of transistor Q9 as a function of reverse-bias voltage plus equilibrium junction potential $(V + \phi)$, and as a function of temperature. Extrapolation of capacitance *versus* $(V + \phi)^{-1/2}$ gives parasitic capacitance, C_p .

Figure 6. Collector-substrate capacitance of the gold-doped and Schottky gate devices as a function of temperature with parasitic capacitance, C_p , subtracted.

Figure 7. Electron-beam-induced current (EBIC) as a function of beam position across a junction for a gold-doped device.

Figure 8. Electron-beam-induced current (EBIC) as a function of beam position across a junction for a Schottky barrier device.

automatic test equipment.

Thomas F. Leedy (S'64, M'65) was born in Harrisburg, PA on October 3, 1942. He received a B.S. in Physics from The American University in 1965, and an M.S.E.E. from George Washington University in 1973, and is currently working toward a degree in Engineering Administration. He has been employed by the National Bureau of Standards since 1965 where he has worked on the fabrication of microelectronic devices, investigated radiation effects on integrated circuits and is presently responsible for development of electronic metrology for

components, and studying the effects of radiation on integrated circuits.

George F. McLane was born in Philadelphia, PA on November 19, 1938. He received the B.E.E. degree from Villanova University in 1960, and the Ph.D. degree in electrical engineering from the University of Pennsylvania in 1971. He worked in the computer field at Remington Rand Univac from 1960 to 1962, and at RCA Service Company from 1962 to 1964. From 1971 to present he has been at the Naval Research Laboratory, Washington, DC, where he has worked on fabricating semiconductor diode lasers, investigating the laser vulnerability of satellite

Nuclear Agency.

Charles S. Guenzer was born in Chicago, IL on April 27, 1943. He obtained his B.S.E. (Phys.) from the University of Michigan in 1966, his Ph.D. from the Applied Physics Department at Stanford University in 1972 and his J.D. from Georgetown University in 1980. He has been employed at the Naval Research Laboratory since 1972 primarily in the area of radiation effects on electronics. His present responsibilities include nuclear hardening of satellites and single event radiation effects. He has been organizing a research program in the latter area for the Defense