THE EFFECTS OF TEST CONDITIONS ON MOS RADIATION-HARDNESS RESULTS*

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ABSTRACT

It is well known that the bias value applied between the gate and substrate can have a significant effect on the threshold voltage shift of MOS transistors under gamma irradiation. However, not so well known are the facts that the bias configuration of the source and drain during the irradiation also can have a significant effect on the threshold voltage shift measured, as can the bias condition applied between the times of irradiation and threshold voltage measurements. An alternating bias (between "ON" and "OFF" states) applied to the gate during irradiation need not give threshold voltage shifts intermediate between those for the two DC bias conditions. In this paper, we present data demonstrating the importance of these effects and discuss their implications with regards to specifications and techniques for radiation-hardness testing.

Introduction

Since the earliest experiments on the radiation hardness of MOS devices,[1] the bias value applied between the gate and substrate has been recognized as an important parameter in determining the threshold voltage shift under gamma irradiation. Although there is some dependence on the process technology used, in general, the worst case bias (i.e., largest negative threshold voltage shift) for n-channel transistors is for the gate biased positively relative to its substrate (the transistor biased in the "ON" state); for p-channel transistors, the worst case bias (largest negative threshold voltage shift) is for the gate at the same potential as its substrate (the transistor biased in the "OFF" state). In the past, these radiation tests have been performed with little attention paid to the configuration of the source and drain during irradiation. For convenience, the source and drain are usually tied to the substrate.

In a functional circuit, the source and drain of a given transistor need not both be at the substrate potential when the gate is at either a high or low potential. It has been found that the configuration of the source and drain during irradiation can have a marked effect on the threshold voltage shift measured. We will present data illustrating the differences in measured shifts for the various configurations that might be expected to occur in a functional integrated circuit.

Radiation damage in MOS circuits is known to anneal with time after irradiation.[2] As a result, specifications for testing often state a maximum time allowed between irradiation and testing of a part. It has recently been found that the bias applied to the part between irradiation and test can have a large effect on the rate and amount of "annealing," and that the shifts associated with the "annealing" may be much more rapid and larger than generally recognized.

After presenting data demonstrating the behavior and magnitudes of these effects, we will briefly consider models and possible explanations for the observed behavior. We postulate that the annealing

effect is more likely associated with the development of further radiation-induced states or traps rather than a true annealing or lessening of radiation damage. Implications for MOS hardness testing will then be discussed, along with recommendations for test programs that will adequately ensure test reproducibility and applicability for a given system or environment.

Unless otherwise specified, all data presented herein is from devices processed with Sandia's present standard polysilicon-gate ELA (Expanded Linear Array, a standard cell design approach) CMOS rad-hard process described fully in Reference 3. Therefore, quantitative threshold shift data and annealing rates may be unique to that process, although we have tested parts processed in other technologies and observed qualitatively similar results. When radiation or annealing data for different configurations or values are compared, transistors from the same wafer lot were employed; in many cases transistors from the same wafer were used. In general, all precautions possible were taken to ensure that the sole cause for the variations observed was the variable intended. All threshold voltages quoted are true thresholds extrapolated from current versus gate voltage measurements, so any effects from differences in transconductance are excluded. The dose rate of the Co^{60} source used for irradiations was 1.54×10^6 rads(Si)/hr.

Effect of Bias Configuration

In a standard CMOS circuit, there are several possible steady-state bias configurations of the source and drain when the gate of transistor is biased to turn the channel "ON" or "OFF." The configurations tested are illustrated in Figure 1. Although in some logic gate configurations intermediate values of voltage could appear on the source or drain, these have not been tested. Configuration number 1 (where the source and drain are tied to the substrate and the gate is tied to a positive voltage for n-channel and tied to a negative voltage for p-channel) is the usual "ON" bias for a transistor in an inverter. Configuration number 4 is the usual "OFF" bias for a transistor in an inverter. Configuration numbers 2, 3, and 6 can occur for transistors in simple logic gate configurations (e.g., NOR or NAND gates). All configurations are possible for a transistor used as a transmission gate.
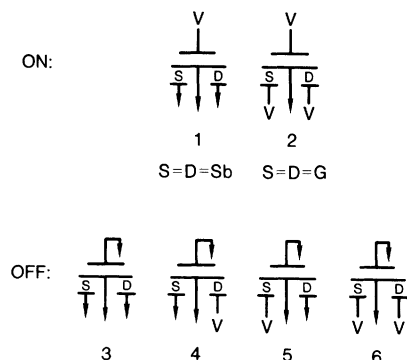

Figure 1. Bias configurations tested: for n-channel transistors, V = +10 V; for p-channel transistors, V = -10 V; other terminals at ground potential.

For the plots which follow, a total of 62 silicon-gate test transistors from one wafer lot were irradiated; groups of several transistors each were irradiated under each of the six bias configurations. The irradiations were performed in steps and the parts tested at each dose level. Between irradiation and testing, the transistor terminals were shorted together, and testing was completed within several minutes after removal from the radiation source. The spread in observed individual transistor threshold voltage shifts was generally small except for bias configuration number 1 on the n-channel transistors at the highest doses.

Figure 2 plots threshold voltages versus total gamma radiation dose for the n-channel transistors with the bias configuration of the source and drain as a parameter. There are marked differences between threshold voltage shifts for the various configurations, particularly for the two cases with the n-channel biased "ON." Configuration number 2 (with the source and drain tied to the gate, as can occur in a transmission or logic gate) represents the worst-case bias for the n-channel "ON" transistor, showing almost a 40-percent greater maximum negative threshold voltage shift than configuration number 1 (the source and drain tied to the substrate, as in an inverter). Also, the maximum shift occurs at 1×10^5 rads(Si) for configuration number 2; whereas for configuration number 1 it occurs at 3×10^5 rads(Si). The differences between the biased "OFF" configurations are much smaller, and are probably not statistically significant (with the possible exception of configuration number 6 in the low 10^5 rads(Si) range).
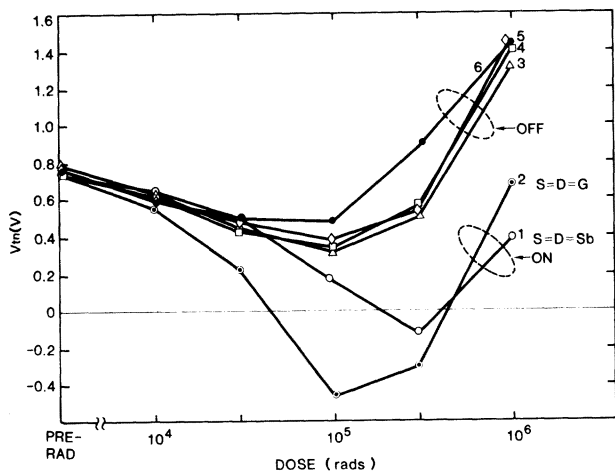

Figure 2. N-channel threshold voltage versus dose for each of the six bias configurations during irradiation.

In Figure 3 are plotted the data for the p-channel transistors. The differences are not as striking as in the n-channel "ON" case, but they are statistically significant. Again, bias configuration number 2 gives the worst-case "ON" bias as in the n-channel transistors, but the difference is only quantitative and not qualitative, as before. Configuration number 6 (with the source and drain at a potential opposite that of the gate and substrate) represents the worst-case "OFF" bias, giving an approximately 20 percent greater threshold voltage shift than the best-case "OFF" bias (configuration number 3, with the source, drain, substrate, and gate shorted together).
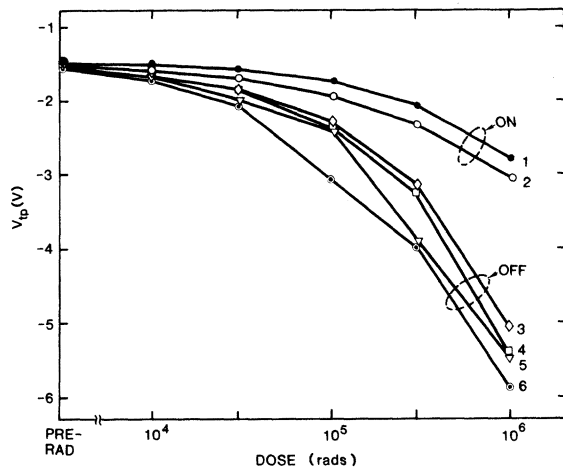

Figure 3. P-channel threshold voltage for each of the six bias configurations during irradiation.

Neither of the worst-case bias configurations correspond to those expected for transistors in normal inverter operation (numbers 1 and 4). The question arises whether these worst-case biases are dominant during operation of a functional circuit. Functional 8-bit Arithmetic Logic Units (ALUs) from the same wafer lot as the above transistors were irradiated under the static bias configuration used for burn-in (11 of the inputs connected to V_{DD}, the other 13 inputs connected to V_{SS}, and no connection to the outputs). Functional data was taken on a Fairchild Sentry tester. Between irradiation and testing, all leads were shorted together, and testing was completed within 30 minutes of irradiation. The data was then examined to determine if the dominant bias configuration of the transistors during irradiation could be extracted. In Figure 4 is plotted the static power supply current I_{DD} as a function of radiation dose; the current peaks at 3×10^5 rads(Si), implying that for the n-channel "ON" bias, configuration number 1 (the usual inverter configuration) is most representative of the transistors in this particular circuit (or at least the transistors in this configuration dominate the leakage current characteristics). This result is what one might reasonably expect, since configuration number 1 occurs much more often for "ON" transistors in logic gates (or inverters) than number 2.
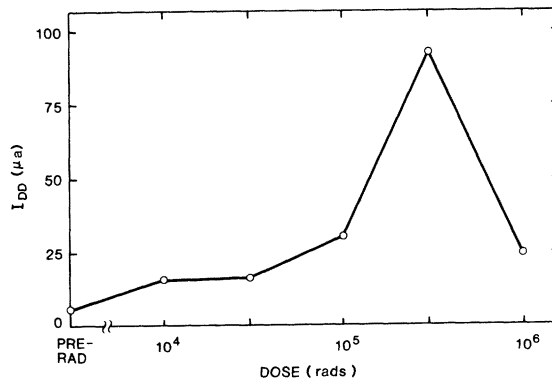

Figure 4. Power supply leakage current as a function of radiation dose for ELA ALU.

Figure 5 shows the increase in a critical path delay time as a function of total gamma dose. The general behavior correlates well with that of the p-channel test transistor data as expected, since the increasing magnitude of the p-channel threshold voltage reduces the current drive of the gates in this logic path substantially. However, there was not enough information to determine which bias configuration best represents the majority of the p-channel transistors in the functional parts.
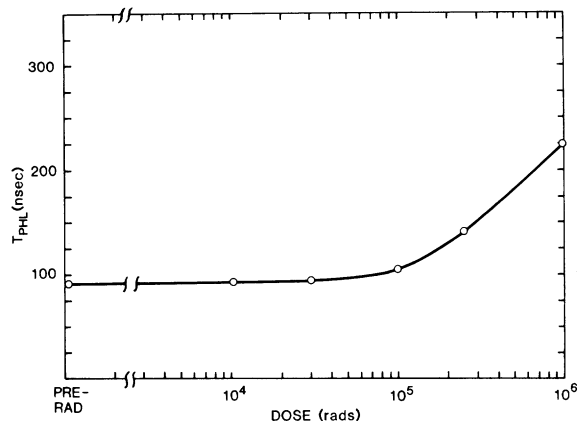

Figure 5. Critical path delay time as a function of total dose for ELA ALU.

It should be noted that the magnitudes of the differences between the configurations is dependent on the process technology employed for the parts. Test transistors processed with Sandia's standard radiation-hardened metal gate process have been tested with different bias configurations under irradiation, and differences have been observed. The differences between configurations are smaller, as are the total radiation-induced threshold voltage shifts, than the silicon-gate parts. For example, at one megarad, n-channel transistors biased "ON" in configuration number 1 show a threshold voltage shift of $\approx$ -0.57 V, whereas those biased in configuration number 2 show a shift of $\approx$ -0.70 V. Configuration number 1 shows the "turnaround" in n-channel threshold voltage shift between 1 and 3 megarads; whereas number 2 does not turn around until higher radiation levels. Thus in this instance, the worst-case configuration for the metal-gate parts is the same as for the polysilicon-gate parts, but the turnaround characteristics are qualitatively different.

Effect of Bias During "Anneal"

Another parameter of importance in determining the radiation-induced threshold voltage shift is the bias condition between the times of irradiation and testing (which, for convenience, we will refer to as the annealing condition). Test transistors from a silicon-gate wafer lot were irradiated to 3×10^5 rads(Si) under bias configuration number 1 for the "ON" bias (source and drain tied to substrate) and under bias configuration number 3 for the "OFF" bias (all terminals shorted together). Threshold voltages were measured immediately ($\approx$ 3 sec) after completion of an irradiation and then remeasured at intervals up to ~ 5×10^4 sec after the dose. During this "annealing" time period, the source, drain, and substrate of the transistors were shorted together, and the gate was biased at either +10 V, 0 V, -10 V, or left floating.

To ensure that the observed threshold shifts with time were not associated with ionic contamination or other instabilities, unirradiated parts from the same lot were subjected to a temperature-bias stress test. Transistors were biased either on or off, and held under that bias for 168 hours (6×10^5 seconds) at 150°C. The maximum threshold voltage shifts observed under either bias condition were ~ 0.02 V for the n-channel transistors and ~ 0.07 V for the p-channel transistors, much less than the shifts observed below.

Figure 6 illustrates the threshold voltage versus time after irradiation for n-channel transistors biased "ON" with identical bias conditions during irradiation and the four different bias conditions after irradiation. There are extraordinary differences among the four cases. If the positive bias is maintained on the gate after irradiation, the threshold voltage shifts positively by large amounts (~ 1 V) in relatively short times (< 1000 sec) and continues to shift at much longer times. If the leads are shorted together after the irradiation, the shifts are small in the first 1000 seconds, but at longer times, the positive shift can become large, of the order of a volt. If the gate is biased negatively or left floating, at short times after the irradiation the threshold voltage shifts more negative, then shows small shifts until long times (~ 10^4 sec) when it begins to shift in the positive direction. These characteristics are reproducible on other transistors from the lot, although in some cases the positive shift at long times for the +10 V anneal condition has been somewhat less than that shown. Transistors processed with a silicon-gate C^2L (Closed Complementary Logic) process have also shown similar annealing behavior.
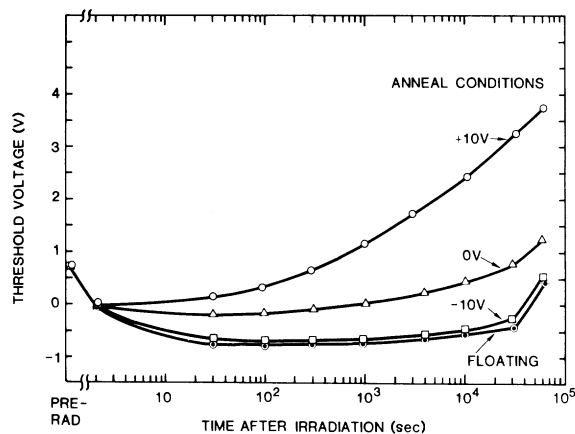

Figure 6. N-channel threshold voltage versus time after irradiation to 3×10^5 rads(Si), biased "ON" during irradiation, with different anneal conditions.

In Figure 7 is shown similar data for n-channel transistors biased "OFF" during irradiation and the different anneal conditions after irradiation. Again, a positive bias on the gate during the anneal causes significant positive shifts in threshold voltage in short times (< 1000 sec). Little difference is observed between cases with the gate at 0 V, -10 V, or floating; in all cases the threshold voltage shifts positively, but not by large amounts until long times.

Figures 8 and 9 present the data for p-channel transistors biased "OFF" and "ON" during irradiation, respectively. For the p-channel "OFF" applying a positive bias causes the threshold voltage to shift in the positive direction slightly until long times. The other three gate anneal conditions produce similar effects until long times, when the -10 V condition appears to cause negative threshold shifts. For the p-channel biased "ON" during irradiation there is very little difference between the four anneal conditions.
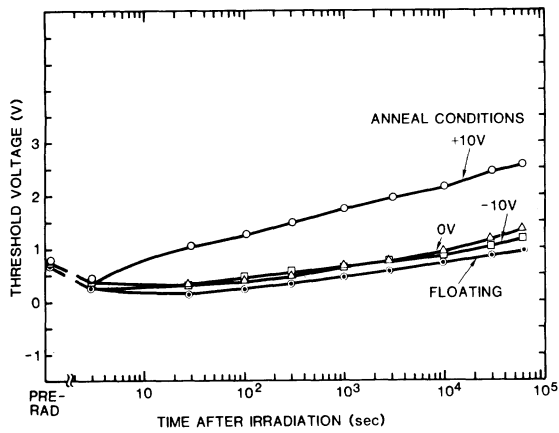
Figure 7. N-channel threshold voltage versus time after irradiation to 3×10^5 rads(Si), biased "OFF" during irradiation, with different anneal conditions.

Figure 8. P-channel threshold voltage versus time after irradiation to 3×10^5 rads(Si), biased "OFF" during irradiation, with different anneal conditions.
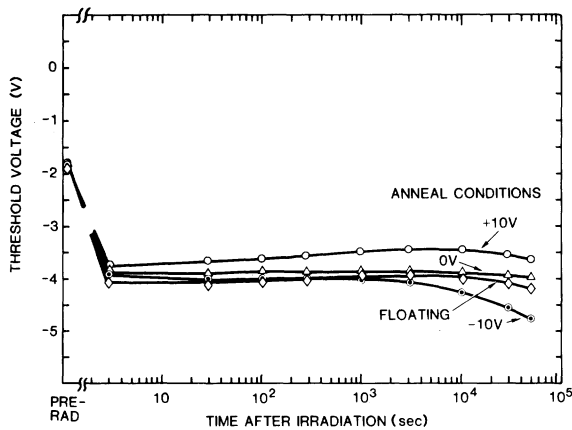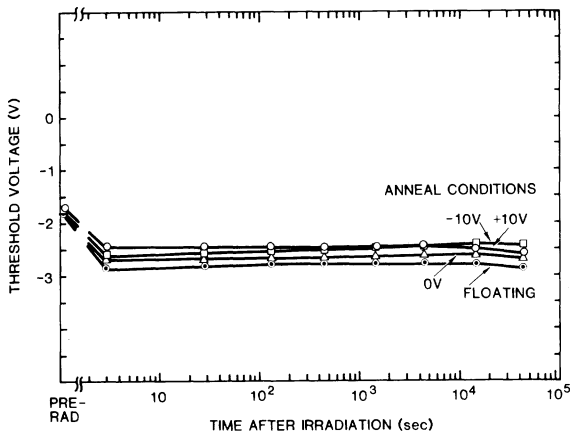

Figure 9. P-channel threshold voltage versus time after irradiation to 3×10^5 rads(Si), biased "ON" during irradiation, with different anneal conditions.

One other point of interest is that if these same parts are reirradiated after the long anneal time to accumulate a total dose, the results can be significantly different between parts that had different anneal conditions, and also between these parts and similar ones irradiated to the same level but without significant annealing times. In particular, if there

was a large difference in threshold voltage between transistors at the end of the anneal time, this difference is reflected in the measured threshold voltages after reirradiation. For example, the parts of Figure 6 were reirradiated in the "ON" bias configuration to accumulate a total dose of 6×10^5 rads after annealing for 6×10^4 seconds. The threshold voltage for the transistor with +10 V on the gate during the anneal dropped to 3.03 V, the one with 0 V on the gate dropped to 1.07 V; for the -10 V anneal, the threshold became 0.63 V; and for the transistor that had the gate floating during the anneal, the threshold became 0.50 V, all thresholds being measured ≈ 3 sec after completion of the irradiation. For a similar part biased "ON" and irradiated to 3×10^5 rads and then to a total dose of 6×10^5 rads with no anneal, the threshold voltage was 0.01 V.

Thus all the anneal conditions for the n-channel biased "ON" during irradiation give results for net threshold voltage shift (and thus hardness) upon reirradiation to a given total dose different from a part which was not allowed to anneal between incremental doses to the same total dose. This statement is also true for the n-channel biased "OFF" during irradiation and allowed to anneal. For the p-channel transistors, the shifts during annealing are small and upon reirradiation, the results are comparable to those obtained from transistors which were not allowed to anneal.

Part of the significance of these anneal characteristics for functional part testing can be seen in Figure 10, where the power supply leakage current for a functional ALU from the same lot as the above transistors is plotted versus time after irradiation to 3×10^5 rads(Si). The part was biased statically during irradiation, and all leads were shorted during the anneal. As shown earlier, the leakage current for this part is dominated by the radiation characteristics of the n-channel transistor biased "ON" in configuration number 1. Thus this characteristic should be compared to that for the n-channel with 0 V on the gate during the anneal in Figure 6. The leakage current drops rapidly around 10^3 seconds after irradiation, which is almost precisely the time at which the n-channel threshold voltage becomes positive and continues to shift more positive. Because of the anneal characteristics, the leakage current falls rapidly in short times after irradiation. Tests on functional parts in which the static bias is maintained between irradiation and test indicate that the leakage current tends to fall more rapidly with time than when the leads are shorted together during the anneal, in qualitative agreement with the test transistor data.
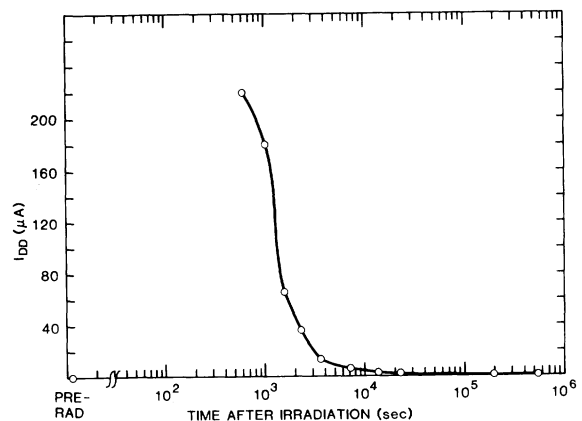

Figure 10. Power supply leakage current as a function of time after irradiation for ELA ALU.

Also expected from the data on test transistors is that the ALU should slow down at long times after irradiation. This has also been observed with functional parts. For example, on the same part for which the leakage currents of Figure 10 were measured, the critical path delay at 600 seconds after the irradiation was 176 nsec; at 22,800 seconds, it was 189 nsec; at 1.9×10^5 seconds it was 197 nsec; and at 3.6×10^6 seconds, it had slowed to 208 nsec.

Again, details of the anneal characteristics depend on the process technology used for the parts.[4] Sandia's metal-gate parts show differences in anneal characteristics for different gate biases during the anneal, qualitatively similar to the polysilicon-gate parts, but the shifts are substantially smaller. For example, for an n-channel transistor biased "ON" in configuration number 1 to a dose of 5×10^5 rads(Si), after an anneal of 5×10^4 seconds with the gate at +10 V, the threshold voltage has shifted positively from its immediate postrad value by only 0.25 V; for the other annealing conditions, the shifts are less.

Models

At this point in time, little can be said quantitatively about models to explain the observed behavior, but some qualitative statements can be made. We will initially address the characteristics observed for threshold voltage shifts with different bias conditions applied between irradiation and testing, or what we have called "anneal" conditions. The first point to be made is that the effect may not be an "anneal" in the sense of a reduction in radiation damage with time but could be associated with the development of further radiation-induced states or traps at long times after the irradiation. Extensive studies of the field- and time-dependent buildup of radiation-induced interface states have been performed by workers at Harry Diamond Laboratories.[5] They have found that the buildup of interface states is a two-stage process in which the field applied during the irradiation and during the time for holes to transport through the oxide (< 1 second for the fields and temperatures considered here) determines the final value of interface states and that during the second stage, which continues for thousands of seconds after the irradiation, the field applied determines the rate at which interface states build up.

The data presented here is consistent with that work in that most of the characteristics can be explained by a long-term buildup of radiation-induced interface states proceeding in parallel with a true thermally activated anneal of radiation damage which may contribute at very long times.

The data for the n-channel transistor biased "ON" during irradiation (Figure 6) illustrates the major points. With +10 V on the gate during the anneal, interface states build up fairly rapidly with time leading to large positive shifts in threshold voltage. At 0 V on the gate, the field in the oxide is much reduced; thus the rate of buildup of interface states is much slower and the positive threshold shift with time is also less. From the above-mentioned work,[5] interface state buildup is expected to be suppressed for -10 V on the gate, and the shifts with time at shorter times (~ $10-10^4$ sec) are small; at longer times, the shifts may be a manifestation of real annealing of the radiation damage. If the slow buildup of interface states is caused by positive ion drift through the oxide as has been proposed,[6] then floating the gate should suppress this motion (since there is then no allowed current flow) and thus prevent interface state generation as does the -10 V

bias. This is supported by the data of Figure 6. Interface-state measurements on capacitors processed to simulate the silicon-gate process, biased at +10 V during irradiation, and subjected to the different anneal conditions qualitatively confirm these trends in interface state generation. The negative shift in threshold at short times (< 30 sec) observed for the -10 V and floating gate anneals is not understood at this time.

The data of Figures 7, 8, and 9 also are consistent with this model. For the n-channel biased "OFF" during irradiation, the field in the oxide is low during the irradiation and thus the final number of interface states generated should be less. This appears to be the case. The p-channel threshold voltage would be expected to be less sensitive to interface state generation, in particular since the capacitor measurements show a peak in radiation-induced interface state density above midgap, a region where the states are not likely to contribute charge to the interface at threshold (under the usual assumption that these states would be acceptor-type).

Less can be said regarding the cause for differences in threshold voltage shifts depending on bias configuration. Certainly the field in the oxide region near the source and drain will be different depending on whether the source and drain are biased relative to the substrate or not. It might be expected then that the charge trapping in the oxide near the source and drain regions could be different depending on the bias configuration. Any differences from this were not observable from the transistor characteristics. To date, the only measurable difference observed (other than the initial threshold voltage shift) has been the annealing characteristics of n-channel transistors biased "ON" in configuration number 1 versus those in configuration number 2. Figure 11 shows these characteristics for two transistors biased "ON" during irradiation to 1×10^5 rads(Si), one in each of the source-drain bias configurations, and then "annealed" with all leads shorted together. As is evident, the shift with time of the device which had the source and drain tied to the gate during irradiation is much more rapid than for the other case. This implies that the interface-state buildup is also much more rapid. Since the initial negative threshold shift is greater for this configuration, it either causes an enhancement of hole-trapping during the irradiation or a suppression of interface-state generation. The annealing data could be consistent with either possibility.
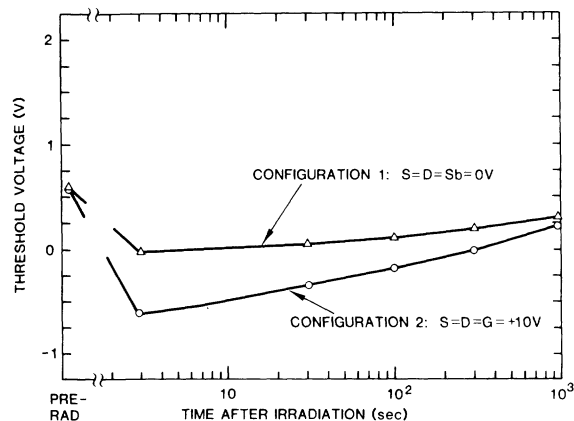

Figure 11. N-channel threshold voltage versus time after irradiation to 1×10^5 rads(Si), biased in the two "ON" configurations, and annealed with all terminals shorted.

Effect of AC Bias

The above work and most test specifications are concerned primarily with determining the worst-case conditions under static bias. However, in functional circuits, some transistors may switch between the "ON" and "OFF" states many times during the irradiation, whereas others may remain in only one state. Since the time constants and mechanisms involved for hole trapping and interface state generation are radically different, transistors switching between states need not necessarily have radiation responses similar to or the average of those for a transistor always "ON" or always "OFF." Static bias tests could conceivably not represent the worst-case situations.

Figures 12 and 13 show threshold voltages as a function of total radiation dose for n-channel and p-channel transistors, respectively. The different curves are for transistors biased "ON" during the irradiation (configuration number 1), biased "OFF" during the irradiation (configuration number 3), and switched between the "ON" and "OFF" states by a 100 KHz square wave during the irradiation. The n-channel transistors switched between states show larger positive threshold voltage shifts than either the "ON" or "OFF" bias, and the p-channel transistors switched between states show less negative shift than either the "ON" or "OFF" bias. At frequencies below 10 KHz, the characteristics of the switched transistors tend to fall between those of the "ON" and "OFF" bias.
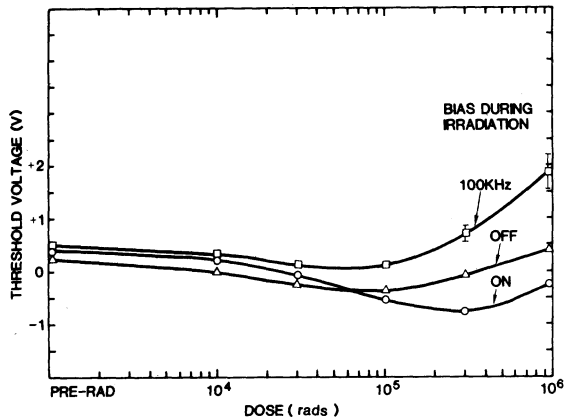

Figure 12. N-channel threshold voltage versus dose for transistors biased "ON," "OFF," or switched between the "ON" and "OFF" states at 100 KHz during irradiation.
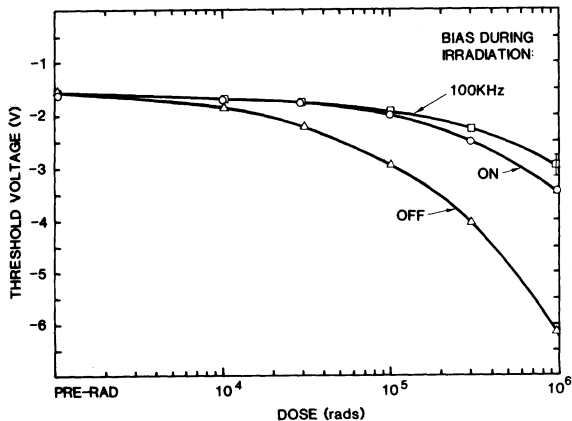

Figure 13. P-channel threshold voltage versus dose for transistors biased "ON," "OFF," or switched between the "ON" and "OFF" states at 100 KHz during irradiation.

Although at high frequencies the threshold shifts of transistors do not fall between those of transistors statically biased "ON" or "OFF," for most applications, the static bias (n-channel "ON," p-channel "OFF") will represent the worst case. Therefore, MOS hardness assurance test programs based on static biasing during irradiation in general can continue to be employed with confidence, providing the requirements stated below are followed.

Summary and Implications

It has been shown that the bias configuration of the source and drain during irradiation can have a significant effect on the threshold voltage shifts measured after irradiation, particularly for n-channel transistors biased "ON." For radiation response testing of MOS test transistors to apply to functional parts, it is thus necessary to know which configuration dominates the important characteristics of the functional circuit. For combinational logic circuits, it appears that the dominant configuration for n-channel transistors biased "ON" is with the source and drain tied to the p-well; it should be noted that this is not the worst case "ON" bias configuration. For p-channel transistors, we have not determined which configuration dominates in functional circuits; the characteristics of the different configurations are qualitatively similar, and quantitatively the difference between the best and worst case "OFF" bias configuration is only about 20 percent.

The bias value applied to the gate affects the "annealing" characteristics of devices. For n-channel transistors, a positive bias applied to the gate after irradiation can cause large positive threshold voltage shifts, whether the device was biased "ON" or "OFF" during the irradiation. Smaller positive threshold voltage shifts are observed with time after irradiation when the gate is shorted to the other terminals for the n-channel transistors. In p-channel transistors, the threshold shifts with time after irradiation are relatively bias independent and generally small. The implications of these results for MOS radiation hardness assurance are that the length of time between irradiation and test and the bias applied during this time can markedly influence the test results. Parts which might pass a leakage current specification 20 minutes after irradiation might not pass 10 minutes after that same irradiation. Maintaining bias on the parts, as has been suggested for some radiation test specifications, may not represent the worst-case situation.

In order to achieve reproducibility of radiation test results between laboratories, and even within a laboratory, it is necessary to fully define the test conditions. For test transistors, the source-drain bias configuration must be specified. The length of time between irradiation and test and the bias during this time also must be standardized and rigidly adhered to. For the results to be useful for assuring hardness of a particular circuit in a particular environment, that circuit and environment must be fully understood with regards to the transistor source-drain bias configuration which will dominate the radiation response and the annealing bias which will predominate during the time the circuit must operate. The test conditions specified should then reflect these considerations. In particular, for low dose rate environments, the proper conditions must apply to acquire the impulse response and annealing data needed for hardness prediction by any technique such as convolution integrals and linear system theory, which has been described previously.[2]

Acknowledgments

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