IEEE Transactions on Nuclear Science, Vol. NS-27, No. 6, December 1980

CONSIDERATIONS FOR HARDENING MOS DEVICES AND CIRCUITS FOR LOW RADIATION DOSES

James M. McGarrity
U.S. Army Electronics Research and Development Command
Harry Diamond Laboratories
Adelphi, MD 20783

Abstract

The radiation response of MOS devices has been shown to be dependent on the details of the device processing and of the device design. To produce megarad-hard devices process controls have been used and special design considerations have been developed. This paper considers the special problem of hardening IC's for low radiation doses (1-10krad). A worst case calculation of the radiation induced threshold voltage shift shows that it may be possible to guarantee the total dose hardness of MOS IC's for low doses by controlling only the gate oxide and field oxide thickness with no other process controls.

Introduction

A great deal of progress has been made in improving the hardness of metal oxide semiconductor (MOS) devices and circuits. The failure levels have been raised at least two orders of magnitude. These gains have been made as a result of careful research which determined that device response is affected by the cleanliness of the processing equipment,[1] the details of the processing such as oxide growth and anneal temperatures[2,3] and the physical properties of the circuit such as the gate oxide thickness.[3,4] The radiation response of the circuits has also been shown to be sensitive to the metallization procedure[2,5] and with the advent of e-beam and x-ray lithography, even the lithography step has its negative effect on hardness.[6] The benefits of using thin gate oxides were pointed out several years ago,[7] and it has been shown that by considering the oxide thickness along with other process modifications megarad-hard integrated circuits (IC's) can be produced.[3] This paper considers the special case of designing MOS IC's to survive low radiation doses (1 to 10 krads (SiO_2)) by controlling only the oxide thickness. By using the basic physics of the radiation response of thermally grown SiO_2, an approach to hardening is suggested which is based on worst-case calculations of the threshold voltage shift. Such an approach guarantees the hardness level and would require that only the oxide thickness be monitored to assure hardness.

Model of Worst-Case Radiation Response

It has been shown that ionizing radiation produces electron-hole pairs in the bulk SiO_2 film in an MOS structure. Under the influence of the applied field in the SiO_2, the electrons and holes which escape initial recombination are transported to the metal-oxide or silicon-oxide interfaces where they are either removed from the system or trapped.[8,9,10] However, the electrons have been shown to be rapidly removed from the SiO_2 leaving a distribution of holes in the SiO_2 which moves toward either interface via a slower phonon assisted process. The threshold voltage shift is proportional to the net positive charge which results, and the largest flatband voltage shifts are observed under positive bias when the holes transport to the Si/SiO_2 interface where a certain percentage is trapped. The percentage of holes trapped in the Si/SiO_2 interface and therefore the resulting threshold voltage shift has been found to be a sensitive function of the device processing.[11] One other major effect of ionizing radiation is the production of interface states, which has also been found to be a function of the device processing. However, the buildup of interface states is generally not a significant problem until the dose reaches 10^5 rads or greater.[12]

The model which is developed in this paper to predict the radiation induced threshold or flatband voltage shifts is based on worst case assumptions about the generation and trapping of charge in MOS structures. The two major assumptions are (1) every 18 eV of energy deposited in the SiO_2 creates an electron-hole pair[8,13] and none of these pairs recombine, and (2) all the electrons are removed from the oxide and all the holes are trapped at the SiO_2/Si interface. A third assumption is that there is little or no interface-state buildup in the dose range considered in this paper (1 to 10 krads). The goal is to make worst-case assumptions and to develop a design rule for making MOS IC's which will meet the radiation hardness goals independent of the device manufacturing details except for gate-oxide and field-oxide thickness.

The first assumption allows us to calculate the worst-case flatband shift without having to consider the effects on the radiation response of operating voltage and the specific ionizing radiation environment. The ionization energy or the energy to create one electron-hole pair in thermally grown SiO_2 has been found by several investigators to be in the range from 18 to 19 eV.[8,13,14] It is assumed here that every 18 eV of energy absorbed in the SiO_2 produces an electron-hole pair. However, under normal operating conditions for MOS devices, it has been found that some fraction of these electron-hole pairs recombine. The fractional yield of electron-hole pairs that escape this initial recombination has been reported in the literature for several types of radiation. Three sets of charge yield data from irradiation experiments with 12 MeV electrons[15], Co^{60} gamma rays[16], and 5 Kev electrons[17] are presented in Figure 1.

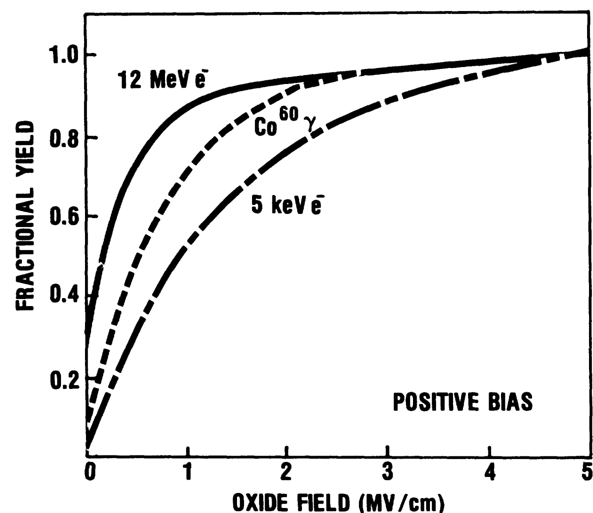

Figure 1. Field and energy dependence of the yield charge generated in thermally grown SiO_2 MOS structures

The fractional yield $F(E,\varepsilon)$, of electrons and holes can be seen to be a function of the electric field in the

U.S. Government work not protected by U.S. copyright.

SiO_2 (or the operating voltage of an MOS IC) and the energy and type of radiation. It can be seen that for the normal electric field range for MOS devices (E < 2 MV/cm) the fractional yield is less than 1.0. At 1 MV/cm the fractional yield is 0.85 for the 13-MeV irradiation, 0.70 for the Co^{60} irradiation, and as low as 0.50 for the 5-keV irradiation. This dependence is important, however, not only for this discussion but also as an consideration in the testing and evaluation of the radiation hardness of MOS devices and circuits. As can be seen in Figure 1, the three sets of yield curves asymptotically approach unity at infinite field. Therefore this maximum value of $F(E,\varepsilon)$ is assumed, so that we can design the circuits to meet the hardness goals independent of operating voltage or radiation environment.

The second assumption, 100 percent hole trapping, eliminates the need for any controls on the oxide processing except for oxide thickness. The net effect of the processing prescriptions developed by the hardening has been to reduce the hole trapping at the Si/SiO_2 interface to 1 percent or less.[3,4] In contrast, the hole trapping has been determined to be in the 10 to 88 percent range in commercially available devices.[18] If, however, we assume that 100 percent of the holes are trapped exactly at the Si/SiO_2 interface and design the device accordingly, these devices should meet or exceed the design goal, independent of specific processing details such as oxide growth and anneal temperatures, metallization procedures, lithography techniques, etching procedures, and so on.

Using the assumptions proposed above, the model for the worst-case threshold voltage shift can be developed. A general expression for the threshold voltage of a MOSFET is given by[19]

$$V_T = \phi_{MS} + \phi_B - \frac{Q_{ox}}{C_{ox}} \frac{Q_B}{C_{ox}} , \qquad (1)$$

where ϕ_{MS} is the potential difference caused by the work function differences between the gate metal and the Si substrate, ϕ_B is the total potential barrier due to band bending, Q_{ox} is the process induced oxide charge, C_{ox} is the oxide capacitance under the metal gate, and Q_B is the depletion region charge. If all the radiation generated holes are assumed trapped at the interface, then effectively the oxide charge is increased by an amount Q_{rad}, and the resulting shift in threshold voltage can be given by[20]

$$\Delta V_T = - \frac{Q_{rad}}{C_{ox}} , \qquad (2)$$

where Q_{rad} is the total density of positive trapped charge generated by a given low dose of radiation. The general expression for the radiation produced trapped charge is

$$Q_{rad} = q\, N_h\, (l_{ox}\, A)\, F(E,\varepsilon)\, f_t\, D \qquad (3)$$

where q = electronic charge (holes)
N_h = initial number of electron hole pairs/cm^3/krad (SiO_2)
l_{ox} = oxide thickness (cm),
A = area under the metal gate,
$F(E,\varepsilon)$ = the fraction of electron-hole pairs escaping initial recombination,
f_t = fraction of holes trapped at the Si/SiO_2 interface,
D = radiation dose in krads (SiO_2).

If, as discussed, we assume that $F(E,\varepsilon) = 1.0$ and $f_t = 1.0$, then Q_{rad} reduces to

$$Q_{rad} = q\, N_h\, (l_{ox}\, A)\, D , \qquad (4)$$

and the resulting flatband or threshold voltage shift is

$$\Delta V_T = - \frac{q\, N_h\, (l_{ox} A)\, D}{C_{ox}} . \qquad (5)$$

For SiO_2 the initial number of electron-hole pairs created by a dose of 1 krad (SiO_2) is given by $N_h = 7.6 \times 10^{15}$ electron-hole pairs per cm^3 per krad (SiO_2), assuming 18 eV per electron-hole pair. Substituting $C_{ox} = \varepsilon\varepsilon_o\, (A/l_{ox})$ and $\varepsilon\varepsilon_o = 3.4 \times 10^{-13}$ farad/cm Equation (5) can be simplified to

$$\Delta V_T = -0.36\, l_{ox}^2\, D \qquad (6)$$

where l_{ox} is in kÅ and D is in krads.

In the next section this simple expression is used to calculate the worst case threshold voltage shifts for various gate or field-oxide thicknesses.

Results of Calculations

The dominant total-dose radiation problems in MOS devices and circuits have been the gate threshold voltage shift (ΔV_T) and the radiation induced inversion and subsequent leakage under the field oxide in the LSI (large-scale-integration) level non-guardbanded circuits. With these two problems in mind, the model is used to determine how thin the gate oxide and field oxides have to be to meet certain hardness goals for typical NMOS and CMOS circuits. The calculations are made assuming operation under positive bias since this has been the worst case. PMOS is discussed later.

Equation (6) has been used to calculate the radiation-induced threshold voltage shift for the gate oxide under positive bias, which, for the case of little or no interface-state buildup, is the worst case. The results are plotted in Figure 2, and some values are given in Table 1. In Table 1 the oxide thicknesses which would result in a threshold voltage shift of $\Delta V_T = 0.1$ V, $\Delta V_T = 0.2$ V, and $\Delta V_T = 1.0$ V are given for various radiation doses. To assure hardness, therefore, the gate-oxide thickness should be less than that given in the table for a desired total dose hardness.

Table 1

Calculated Maximum Gate-Oxide Thickness

	Gate-oxide thickness (Å) at various ΔV_T		
DOSE (krad (SiO_2))	ΔV_T=0.1V	ΔV_T=0.2V	ΔV_T=1.0V
1	527	750	1667
2	373	527	1178
3	304	430	962
5	235	333	742
10	167	235	527

The state-of-the-art gate oxide thickness is down to 700 Å, which makes guaranteeing CMOS hardness in the 5-krad range look very achievable assuming an acceptable -1 V ΔV_T. For NMOS the problem is a little more difficult because the acceptable threshold voltage shifts are in the range -0.1 to -0.2 V.[21] The calculation indicates that NMOS could fail at 1 krad (SiO_2) or less if one assumes a 700-Å gate oxide. However, a more advanced NMOS process is clearly on the horizon. In the recent issue of IEEE Transactions on Electron Devices (April 1979), there were many papers from various organizations reporting on devices with

l_{ox} less than 700A and as thin as 250A. If an acceptable shift of $\Delta V_T = -0.10$ V is assumed for an NMOS circuit, then with a 250-A gate oxide a hardness level of 4.4 krad is guaranteed.

The second total dose problem for the LSI-level MOS circuits has been the threshold voltage shift under the field oxide.[23] It is recognized that the thick field oxide is generally not a high quality oxide like the gate oxide, and there is evidence that electron trapping is much more significant in these thick oxides.[24] However, since there is little information available in the literature on the radiation response of thick field oxides, equation (6) has been used to calculate the worst-case threshold voltage shifts for the thick field oxides. The results are shown in Figure 3. Some values are given in Table 2, where $\Delta V_T = -10$ V and $\Delta V_T = -25$ V were selected to bracket the range of field oxide threshold voltage shifts found in the literature.

Table 2

Calculated Maximum Field-Oxide Thickness

Dose(krad(SiO_2))	Field-oxide thickness (kA) at various ΔV_T	
	$\Delta V_T = -10$ V	$\Delta V_T = -25$ V
1	5.3	8.3
2	3.7	5.9
3	3.0	4.8
5	2.4	3.7
10	1.7	2.6

Most of the thickness of the field oxide shown in Table 2 are thinner than those currently used. The calculation, however, is much more conservative for the thick oxides, because the actual field across the oxide is much lower at normal operating voltages than for the gate oxide. As pointed out earlier, the yield of charge is field dependent. For the thickest oxides, the actual yield of charge can be as low as 0.2 of the yield obtained at high fields.

Because these thicknesses are less in line with current technology, it may be necessary to relax the constraint on the fractional yield factor $F(E,\varepsilon)$ in order to be able to apply the general approach. If we no longer assume $F(E,\varepsilon) = 1.0$ then equation 6 becomes

$$\Delta V_T = -0.36\, l_{ox}^2\, D\, F(E) \qquad (7)$$

A designer could use the $F(E,\varepsilon)$ curve most appropriate for the type of radiation environment the circuits are to survive in. However, it would be more conservative to use the $F(E,\varepsilon)$ curve for the high-energy irradiation, since the yield of charge is the largest of the three sets of data shown in Figure 1. Although no detailed study has been made of the yield of charge for different energy radiations, it is not likely that the yield versus field results would be much greater than for the case of the 13-MeV electrons. Generally, the yield is expected to be related to the stopping power of the radiations. For the higher energy irradiations, the recombination should be predominately geminate and the resulting charge yield high. As the stopping power of the primary and secondary radiation decreases, columnar recombination will begin to dominate and the charge yield should be lower. Mozumder and Magee[25] have developed a detailed model of ionizing radiation tracks for aqueous solutions which demonstrates these conclusions.

The $F(E,\varepsilon)$ data for the 13-MeV electron irradiation obtained from a best fit of a geminate recombination model is given in Table 3.[15]

Table 3

Hole Yield in MOS Capacitors for 13-MeV Electron Irradiation

E (MV/cm)	F(E)	E (MV/cm)	F(E)
0.0	0.245	1.0	0.83
0.1	0.40	1.2	0.85
0.2	0.50	1.4	0.87
0.3	0.58	1.6	0.88
0.4	0.65	1.8	0.90
0.5	0.69	2.0	0.92
0.6	0.73	2.5	0.94
0.7	0.76	3.0	0.95
0.8	0.78	3.5	0.96
0.9	0.80	4.0	0.98

Using these results in conjuction with equation (7), a less than worst-case but still conservative prediction of the radiation-induced threshold voltage shift can be calculated for the thick field oxide. Only the ΔV_T under positive bias is presented since this is the most severe situation. Under negative bias both the hole trapping and the interface state buildup are significantly reduced, and because the two effects add to cause a negative threshold voltage shift, there is no problem with inversion under the p-channel field oxide. The results of the calculations are shown for two radiation levels (2 krad(SiO_2) and 10 rad(SiO_2)) in Figure 4. As can be seen, more acceptable values of the field-oxide thickness are predicted. Some of the results are also tabulated for a range of radiation levels in Table 4.

Table 4

Modified Predicted Maximum Field-Oxide Thickness

	Field-oxide thickness (kA) under various conditions					
	$\Delta V_T = -10$ V			$\Delta V_T = -25$ V		
	Worst	Applied Voltage		Worst	Applied Voltage	
Dose	Case	+10 V	+5 V	Case	+10 V	+5 V
1	5.3	8.6	9.6	8.5	13.0	14.0
2	3.7	5.5	6.6	6.0	9.4	10.6
3	3.1	4.2	5.1	4.8	7.5	8.7
5	1.4	3.0	3.7	3.7	5.5	6.3
10	1.9	2.0	2.4	2.8	3.5	4.2

Since the range of field oxides which are currently in use is from 7 to 10 kA, these results indicate that the situation has only been improved for applications in the 2 to 3 krad(SiO_2) range. With future scaling of MOS devices it seems possible that field oxides in the range of 2500 A could be used, which would make hardening to 10 krad(SiO_2) possible. For the present, however, it would appear that a designer could not be

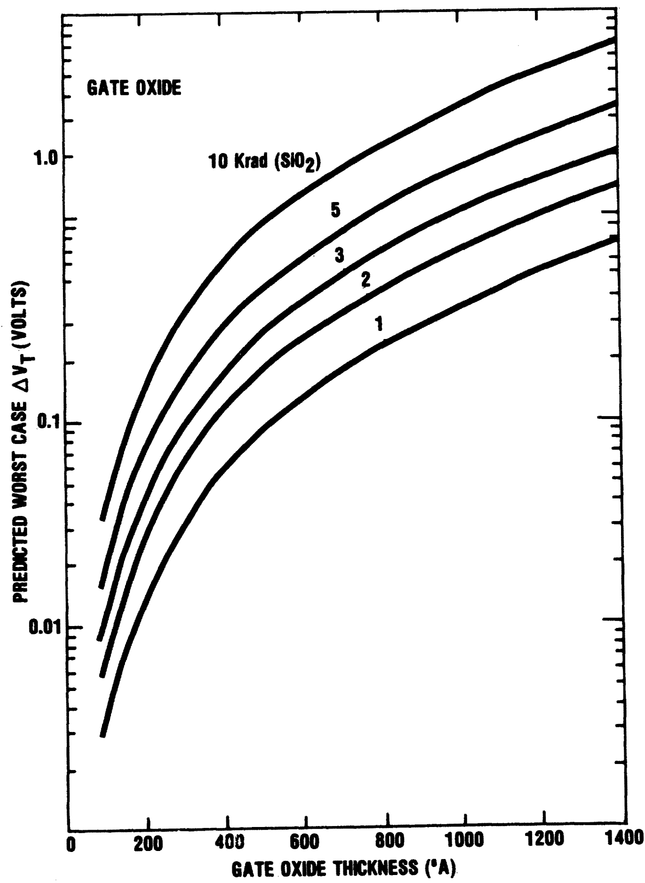

Figure 2. Predicted worst-case threshold voltage shift (ΔV_T) in thermally grown gate oxides at various radiation doses

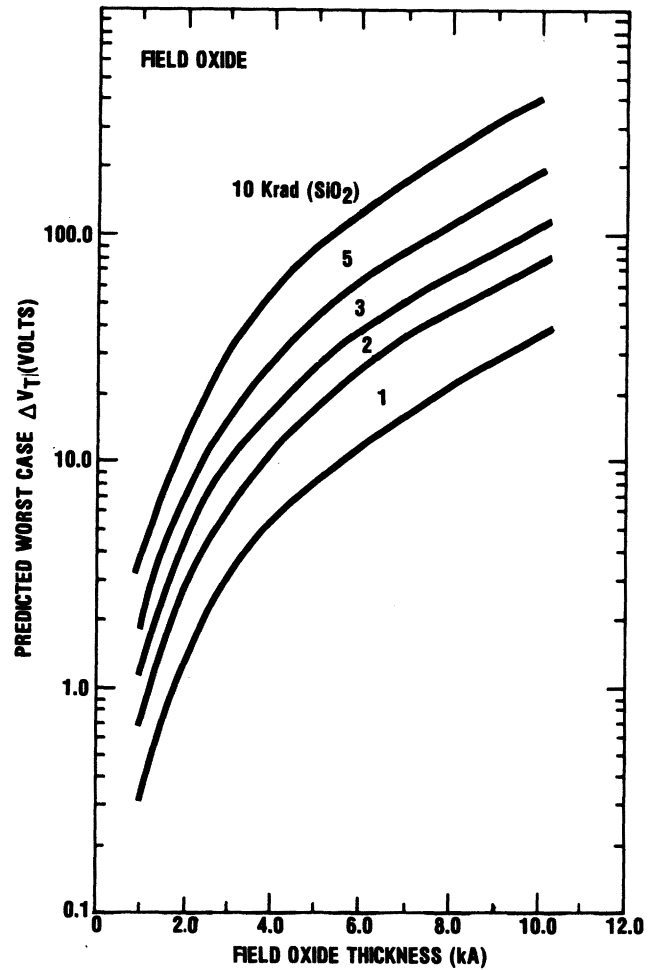

Figure 3. Predicted worst-case threshold voltage shift in thick field oxides at various radiation doses.

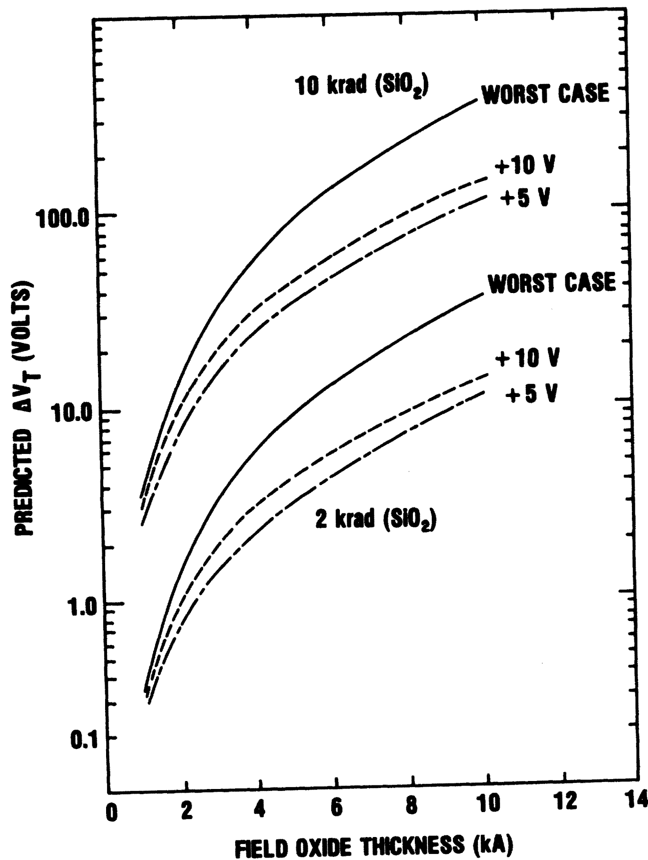

Figure 4. Predicted threshold voltage shift in thick field oxides corrected for field-dependent recombination at +10V and +5V operating voltages

sure of meeting hardness goals greater than about 3 krad unless he resorts to special processing or uses the hardened field oxides which have been developed.[23,26]

Discussion of Assumptions and Predictions

The worst-case calculation of the radiation induced threshold voltage shift presented in Figures 1 through 4 and in Table 1 through 4 indicates that for today's technology it looks quite feasible to meet some low-dose hardness requirements by controlling only the gate oxide and field-oxide thickness. Although the assumptions were conservative, they were not extreme. By assuming no recombination, we are building in a safety factor of only 0.1 to 2 depending on the field and the energy and type of radiation. The most restrictive assumption is of course the 100 percent hole trapping at the Si/SiO_2 interface. As mentioned earlier, the highest percentage of trapping reported has been 88 percent, but some researchers have produced samples in which the trapping is as low as 1.0 percent. It is possible that in some case we are conservative by two orders of magnitude in our predicted threshold voltage shift. It is more likely that for commerical devices we are only conservative by a factor of 2 to 4.

If the percentage of hole trapping is known for a given process, then new values of l_{ox} can be calculated for the tables 1, 2 and 4 using the correction factor shown in Table 5 for a given f_T.

Table 5

Correction Factor for L_{ox} as Function Of Percentage of Hole Trapping

f_T	L_{ox} Corrections
1.0	1.0
0.75	1.15
0.50	1.4
0.25	2.0
0.10	3.2
0.05	4.5
0.01	10.0

This correction was developed by putting the factor f_t (which was assumed for the worst case equal to 1.0) back into equation (6) and showing that l_{ox} is proportional to $(f_t)^{-1/2}$. If the correction is used however, then process controls must be instituted to assure that f_t does not change with time, which defeats one of the original goals of the paper.

There will also be some annihilation of trapped holes even at short times due to the injection of electrons from the Si, which will reduce the response from the predictions made by the model. This effect has been observed even at low temperature when the holes are distributed in the bulk SiO_2. The holes trapped within 30 A of the interface were annealed out in about 800 s.[27] In fact, electron injection is likely to be the explanation of why the highest reported value of hole trapping is 88 percent. In most experiments the flatband or threshold voltage is not measured until several minutes after the radiation exposure, and during that time some of the holes are annihilated. The injection of electrons is likely to become a much more significant factor in determining ΔV_T as the gate oxides are continually thinned down during the scaling process to produce VLSI (very-large-scale-integration) circuits. In fact, measurements made in very thin oxides ($l_{ox} \leq 90$ Å) some years ago by S. Share et. al. showed that all the holes could be annealed out after an irradiation to 10^6 rads with no bias applied.

The second major effect of ionizing radiation in MOS structures is the production of interface states. It was assumed, however, in the development of the model that interface state generation was negligible at low radiation doses. This is consistent for a model of worst-case threshold voltage shifts, except for p-channel devices. For n-channel devices, the interface states have been observed to compensate for the negative threshold voltage shift caused by the trapped positive charge, so the worst case is to assume no interface states. For the n-channel field oxide, again the contribution of interface states negatively charged under positive bias will prevent the surface from inverting under the field oxide. For the p-channel field-oxide, the positively charged interface states will cause a negative threshold voltage shift which will add to the threshold voltage shift caused by the trapped positive charge. This negative shift will of course prevent inversion under the field oxide. The only problem which does occur is with p-channel gate oxides, where the buildup of interface states and oxide charge shifts the threshold voltage and prevents the channel from forming. This occurs at high doses (10^5 to 10^6 rads) and is not likely to be a problem at low doses. But this is a situation in which the worst-case threshold voltage shift is observed when there *is* an interface-state buildup.

The magnitude of the threshold voltage shift caused by interface-state buildup in p-channel devices cannot be estimated on the basis of the physics of the process, because no good physical quantitative model has been developed to describe the interface-state buildup. We can, however, estimate the worst-case buildup based on the data available in the literature. The emphasis of the research has been on the study of specially prepared hard oxides, and little information is available on the buildup of interface-states at low doses for unhardened oxides. However, the worst cases found reported interface-state densities following irradiation to 1 Mrad(SiO_2) in the range from 10^{12} to 10^{13} cm^{-2}.[28,29,30] Using the total-dose power-law dependence, $D^{2/3}$, which has been reported[12] for hard oxides the radiation induced interface-state density can be estimated for 1 and 10 krads. Assuming 10^{13} states cm^{-2} at 1 Mrad then the estimated densities are 10^{11} cm^{-2} at 1 krad and 5×10^{11} cm^{-2} at 10 krad. If these states were positively charged, there could be a resulting shift of approximately 0.1 V at 10^3 rads (SiO_2) and 0.5 V at 10^4 rads(SiO_2) in the p-channel threshold voltage for the thicker gate oxides. These negative shifts, even when added to the shifts caused by hole trapping, should not cause a problem.

Advantages of this Approach

The biggest advantage of using this worst-case approach for hardening is that circuits hard at low doses could be produced by any manufacturer with the thin-oxide technology needed to make the parts. The only process controls would be the normal ones required to produce reliable IC's. The hardness assurance would be carried out by simple capacitance measurements or ellipsometry measurements to determine oxide thickness.

Another advantage of this approach is that the devices designed by these rules will also be hard at

cryogenic temperatures. For megarad-hard oxides where the hole trapping may be as low as 1 percent, the radiation sensitivity is greatly enhanced at low temperatures because the radiation-generated holes are immobilized in the bulk SiO_2[14,15] or their transport is severely slowed. The dominant mechanisms for these devices to recover from the radiation is for the holes to transport the interface, where 99 percent are removed; therefore, if the holes do not move to the interface these devices do not recover. But for oxides with more than 50 percent hole trapping there is no short-term recovery. In fact, as the holes transport to the interface, the threshold voltage shift becomes larger.[27] For the assumptions made in this model, the worst case is the room-temperature case, since 100 percent of the holes trapped at the interface causes twice the flatband voltage shift that would be caused by the 100 percent of holes immobilized uniformly at low temperature in the bulk SiO_2.

An application of these results is for the worst-case assessment of commercially produced devices or IC's. Manufacturers who have not intentionally developed a hardened process can use this type of model to estimate the minimum hardness of their MOS products. If, because of their design characteristics, the products look like they will meet DoD requirements, these manufacturers may be encouraged to do further testing to determine the hardness. Since no process changes would be required of these manufacturers, more rad-hard devices could be made available to the user community.

Conclusion

The conservative analysis presented in this report indicates that it is possible to assure the hardness of MOS devices and circuits for low total-dose exposures by controlling only the gate-oxide and field-oxide thickness. This approach has the advantage that circuits designed according to these guidelines could be manufactured on any process line. The range of gate-oxide thicknesses required for both CMOS and NMOS appears to be reasonable. The field-oxide thickness range is reasonable if the constraint on recombination is relaxed as suggested in the test. However, with the scaling down which is currently underway commercially and with the support of the DoD VHSIC program, a thin-oxide technology which could be hard to 10^4 rads(SiO_2) may soon be available. In fact, in the paper by E.E. King and G.J. Manzo, in this issue there is evidence presented that suggests that the effects are already being observed.

References

1. H.L. Hughes, R.D. Baxter and B. Phillips, IEEE Trans. Nucl. Sci., NS-19, No. 6, 256, (1972).
2. K.G. Aubuchon, IEEE Trans. Nucl. Sci., NS-18, No. 6, 117, (1971).
3. G.F. Derbenwick and B.L. Gregory, IEEE Trans. Nucl. Sci., NS-22, No. 6, 2151, (1975).
4. G.W. Hughes and R.J. Powell, IEEE Trans. Nucl. Sci., NS-23, No. 6, 1569, (1976).
5. J.M. Aitkin, D.J. DiMaria and D.R. Young, IEEE Trans. Nucl. Sci., NS-23, No. 6, 1526, (1976).
6. H.L. Hughes, IEEE Trans. Nucl. Sci., NS-26, No. 6, 5053, (1979).
7. S. Share, A.S. Epstein, V. Kumar, W.E. Dahlke and W. Haller, J. Appl. Phys., Vol. 45, No. 11, Nov. 1974.
8. J.R. Srour, O.L. Curtis, Jr and K.Y. Chiu, IEEE Trans. Nucl. Sci., NS-21, No. 6, 73, (1974).
9. H.E. Boesch, Jr, F.B. McLean, J.M. McGarrity and G.A. Ausman, IEEE Trans. Nucl. Sci., NS-22, No. 6, 2163, (1975).
10. R.C. Hughes, E.P. EerNisse and H.J. Stein, IEEE Trans. Nucl. Sci., NS-22, No. 6, 2227, (1975).
11. F.B. McLean, H.E. Boesch, Jr and J.M. McGarrity, IEEE Trans. Nucl. Sci., NS-23, No. 6, 1506, (1976).
12. P.S. Winokur, H.E. Boesch, J.M. McGarrity and F.B. McLean, IEEE Trans. Nucl. Sci., NS-24, No. 6, 2113, (1977).
13. G.A. Ausman and F.B. McLean, Appl. Phys. Lett., 26, 173, (1975).
14. H.H. Sander and B.L. Gregory, IEEE Trans. Nucl. Sci., NS-22, No. 6, 2157, (1975).
15. H.E. Boesch and J.M. McGarrity, IEEE Trans. Nucl. Sci., NS-23, No. 6, 1520, (1976).
16. J.R. Srour and K.Y. Chiu, IEEE Trans. Nucl. Sci., NS-24, No. 6, 2140, (1977).
17. O.L. Curtis, Jr, J.R. Srour and K.Y. Chiu, J. Appl. Phys., 45, 4506, (1974).
18. R. Freeman and A. Holmes-Siedle, IEEE Trans. Nucl. Sci., NS-25, No. 6, 1216, (1978).
19. W.M. Penny and L. Lau, MOS Integrated Circuits, p. 58, Van Notbrand Reinhold Co., (1972).
20. A.S. Grove, Physics and Technology of Semiconductor Devices. J. Wiley and Son, N.Y., N.Y. (1969).
21. D.K. Meyers, IEEE Trans. Nucl. Sci., NS-24, No. 6, 2169, (1977).
22. R.H. Dinnard, F.H. Gaensslin, E.J. Walker and P.W. Cook, IEEE Trans. Elec. Dev., ED-26, No. 4, p. 325, (1979).
23. J.R. Adams, W.R. Daives and T.J. Sanders, IEEE Trans. Nucl. Sci., NS-24, No. 6, 2099, (1977).
24. J.H. Thomas, III and F.J. Feigl, J. Phys. Chem. Solids, Vol. 33, 2197, (1972).
25. A. Mogunder and J.L. Magie, Radiation Research, 28, 203, (1966).
26. E.E. King, IEEE Trans. Nucl. Sci., NS-26, No. 6, (1979).
27. H.E. Boesch, Jr, F.B. McLean, J.M. McGarrity and P.S. Winokur, IEEE Trans. Nucl. Sci., NS-25, No. 6, 1239, (1978).
28. R.A. Kjar and D.K. Nichols, IEEE Trans. Nucl. Sci., NS-22, No. 6, 2193, (1975)
29. C.R. Viswanathan and J. Maserjian, IEEE Trans. Nucl. Sci., NS-23, No. 6, 1540, (1976).
30. P.S. Winokur, J.M. McGarrity and H.E. Boesch, Jr, IEEE Trans. Nucl. Sci., NS-23, No. 6, 1580, (1976).