

Development of a High Density Pixel Multichip Module at Fermilab

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Abstract—At Fermilab, both pixel detector multichip module and sensor hybridization are being developed for the BTeV experiment. The module is composed of three layers. The lowest layer is formed by the readout integrated circuits (ICs). The backs of the ICs are in thermal contact with the supporting structure, while the tops are flip-chip bump bonded to a pixel sensor. A low mass flex-circuit interconnect is glued on the top of this assembly, and the readout IC pads are wire-bonded to the circuit. The BTeV pixel detector is based on a design relying on this hybrid approach. This method offers maximum flexibility in the development process, choice of fabrication technologies, and the choice of sensor material. This paper presents strategies to handle the required data rate and performance characteristics of the pixel module prototypes.

Index Terms—Bump bond, flex circuit, multichip module, pixel detector, pixel readout chip, pixel sensor.

I. INTRODUCTION

AT FERMILAB, the BTeV experiment has been proposed for the C-Zero interaction region of the Tevatron [1]. The vertex detector for this experiment will be a pixel detector composed of 60 pixel planes of approximately $100 \times 100 \text{ mm}^2$ each, assembled in 30 stations. The planes are located perpendicular to the colliding beam with pixels as close as 6 mm to the beam. Each plane is formed by an arrangement of multichip modules of various lengths. The modules are formed by up to 8 pixel readout chips bump bonded to a single silicon pixel sensor. The modules on opposite faces of the same pixel station are assembled perpendicularly in relation to each other (see Fig. 1).

A “hit” in the pixel sensor occurs when a charged particle (from the collision of a proton with an anti-proton) passes through the biased sensor (Fig. 2). The pixel cells are n^+ implants in the n bulk of the sensor, isolated from each other with a p implant. The back of the sensor is biased with a negative voltage, so the passage of charged particle creates an ionized channel in the depleted sensor [2]. The signal in the sensor from the particle is integrated in the pre-amplifier of the readout chips (connected by bump-bonds to the sensor pixel elements).

The multichip module packaging must conform to special requirements dictated by BTeV [1]: the pixel detector will be in-

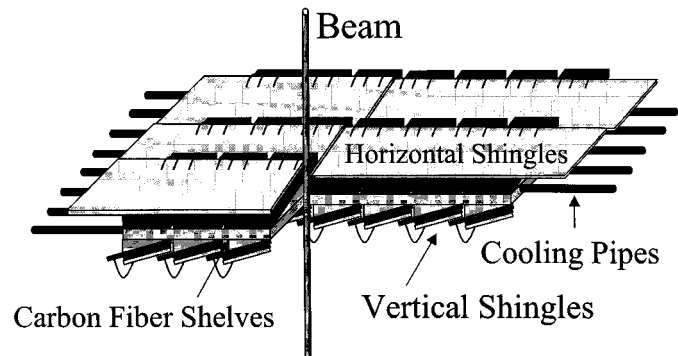


Fig. 1. Pixel half station.

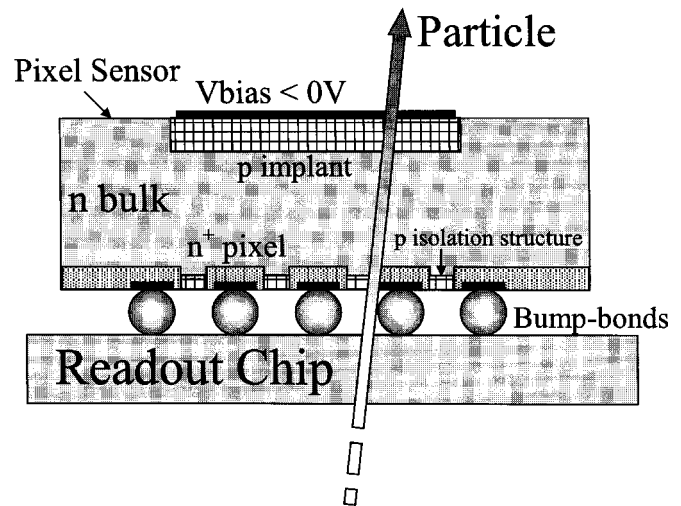


Fig. 2. Pixel sensor.

side a strong magnetic field (1.6 Tesla), the flex circuit and the adhesives cannot be ferromagnetic, the pixel detector will also be placed inside a high vacuum environment, so the multichip module components cannot outgas, the radiation rates (around 3 Mrad per year) and temperature (-5°C) also impose severe constraints to the pixel multichip module packaging design.

The pixel detector will be employed for online particle trajectory finding for the lowest-level event selection system (trigger) and, therefore, the pixel readout chips will have to read out all detected hits. This requirement imposes a severe constraint on the design of the readout chip, the hybridized module, and data transmission to the trigger and data acquisition system. It also

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	<i>a</i>	<i>b</i>	<i>c</i>	<i>d</i>	<i>e</i>	<i>f</i>	<i>g</i>	<i>h</i>	<i>i</i>
Module 1 →	11	13	17	17	20	18	16	13	8
Module 2 →	11	18	26	31	39	33	25	18	12
Module 3 →	16	20	37	61	76	59	39	26	18
Module 4 →	17	35	63	141	234	130	65	36	16
Module 5 →	23	35	74	234	• ← Beam				

Fig. 3. Average bit data rate at middle station, in Mb/s.

22			0
ADC	Beam-Crossing Number	Column	Row

Fig. 4. Pixel module data format (23 b).

TABLE I
HALF PLANE REQUIRED BANDWIDTH, IN Mb/s

	Req. Bandwidth
Module 1	133
Module 2	213
Module 3	352
Module 4	737
Module 5	366
Total	1801

requires the collection of a large amount of data (~ 216 Gb/s) that is going to be used to identify interesting interactions.

Several factors impact the amount of data that each readout chip needs to transfer: readout array size, distance from the beam, number of bits of analog to digital converter (ADC) bits, data format, etc. Presently, the most likely dimension of the pixel chip array is 128 rows by 22 columns of pixels and 3 b of ADC information.

II. PIXEL MODULE READOUT

The pixel module readout must allow the pixel detector to be used in the lowest-level experiment trigger. Our present assumptions are based on simulations that describe the data pattern inside the pixel detector [3]. The parameters used for the simulations are: luminosity of $2 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$ (corresponds to an average of two beam-beam interactions per 132 ns beam-crossing time), pixel size of $400 \times 50 \mu\text{m}^2$, threshold of 2000 e^- and a magnetic field of 1.6 Tesla.

Fig. 3 shows a sketch of the 40 chips that may compose a pixel half-plane. The beam passes through the place represented by the black dot. These numbers assume the 23-b data format shown in Fig. 4. The rows in Fig. 3 represent pixel multichip modules. For this discussion, the modules are numbered from 1 to 5 from top to bottom. The chips are labeled from *a* to *i* from left to right. Module 4 is the busiest pixel module. The chip *e* in module 4 and chip *d* in module 5 are the busiest chips.

Table I presents the required bandwidth per module. From this table we see that each half pixel plane requires a bandwidth of approximately 1.8 Gb/s.

Simulations were run on a model of the readout architecture with a readout clock of 35 MHz. This frequency can support a readout efficiency of approximately 98%, even when the hit rate for the readout chip closest to the beam is three times the nominal hit rate. Efficiency is lost due to a combination of a

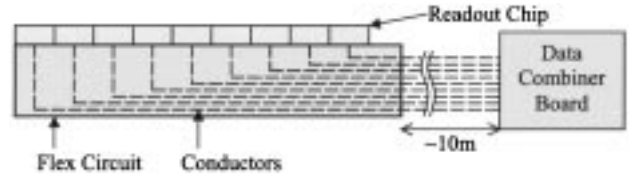


Fig. 5. Pixel module point-to-point connections.

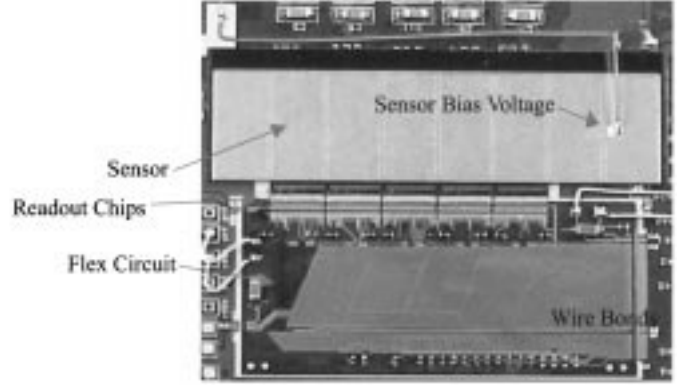


Fig. 6. Prototype pixel module.

pixel all being hit more than once before the first hit can be read out and to bottlenecks in the core circuitry.

A. Proposed Readout Architecture

The readout architecture is a direct consequence of the BTeV detector layout. The BTeV detector covers the forward direction, 10–300 mrad, with respect to both colliding beams. Hence, the volume outside this angular range is outside the active area and can be used to house heavy readout and control cables without interfering with the experiment. The architecture takes advantage of this consideration.

The data combiner board (DCB), located approximately 10 m away from the detector, remotely controls the pixel modules. All the controls, clocks, and data are transmitted between the pixel module and the DCB by differential signals employing the low-voltage differential signaling (LVDS) standard. Common clocks and control signals are sent to each module on buses seen by each readout IC. All data signals are point-to-point connections from each readout IC to the DCB. Fig. 5 shows a sketch of the proposed readout architecture. For more details refer to [4].

This readout technique requires the design of just one rad-hard chip: the pixel readout chip. The point-to-point data links minimize the risk of an entire module failure due to a single chip failure, and eliminate the need for a chip ID to be embedded in the data stream. Simulations have shown that this readout scheme results in readout efficiencies that are sufficient for the BTeV experiment.

III. FIRST PIXEL MULTICHIP MODULE PROTOTYPE PACKAGING

Fig. 6 shows the first prototype of the pixel module. It is composed of five Fermilab Pixel (FPiX1) readout chips bump-bonded to a pixel sensor and a four layer high density flex circuit made by Fujitsu Computer Packaging Technologies (FCPT), San Diego, CA. This flex circuit has line traces of $20 \mu\text{m}$ with

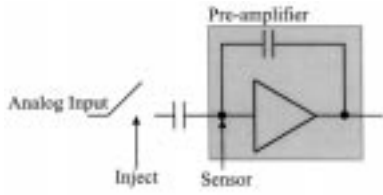


Fig. 7. FPIX1 pre-amplifier inputs.

TABLE II
PERFORMANCE OF THE FIVE CHIP MODULE (IN INPUT e^- EQUIVALENT)

Chip	1	2	3	4
μ_{Th}	1030	1250	1500	1400
σ^2_{Th}	400	350	370	420
μ_{Noise}	75	70	70	80
σ^2_{Noise}	26	25	20	24

TABLE III
PERFORMANCE OF ONE CHIP IN THE FIVE CHIP MODULE
(IN INPUT e^- EQUIVALENT)

μ_{Th}	σ^2_{Th}	μ_{Noise}	σ^2_{Noise}
6360	380	70	20
2900	380	74	28
1030	400	75	26

40 μm pitch, copper line thickness of 5 μm , vias spaced by 200 μm , via cover pads of 100 μm and average via hole diameter of 26 μm .

In this prototype, the flex interconnect is located on the side of the readout chips instead of on the top of the sensor (as in the baseline design). The pixel sensor used is oversized; it can be bump bonded to a total of 16 readout chips.

There are two ways to inject charge into the pre-amplifier of FPIX1. The first one is through the connection with the sensor that occurs when a particle hits a pixel. The second way is to inject an analog signal to a capacitor in the input of the chip pre-amplifier (Fig. 7).

This pixel module has been characterized for noise [noise mean (μ_{Noise}) and noise variance (σ^2_{Noise})] and threshold dispersion [threshold mean (μ_{Th}) and threshold variance (σ^2_{Th})]. These characteristics were measured by injecting charge with a pulse generator via the analog front end of the readout chip, and reading out the hit data through a logic state analyzer.

Data from four readout chips is available because one of the chips failed. The results for one specific threshold are summarized in Table II. Results for three different thresholds are shown in Table III.

The flex circuit has several digital lines (21 differential and 11 single ended) that can inject noise into the sensor underneath it. For this reason, a solid ground plane was placed in the bottom layer of the flex circuit to shield from the flex circuit's digital activity. The comparison of these results with the results from a single FPIX1 chip with no flex circuit shows no noticeable degradation in performance [5]. Fig. 8 shows the hit map of a pixel chip in the five-chip pixel module using a radioactive source (Sr 90). Furthermore, tests with a deadtimeless mode, where the charge injected into the front end is time-swept in relation to the readout clock, also do not reveal any degradation

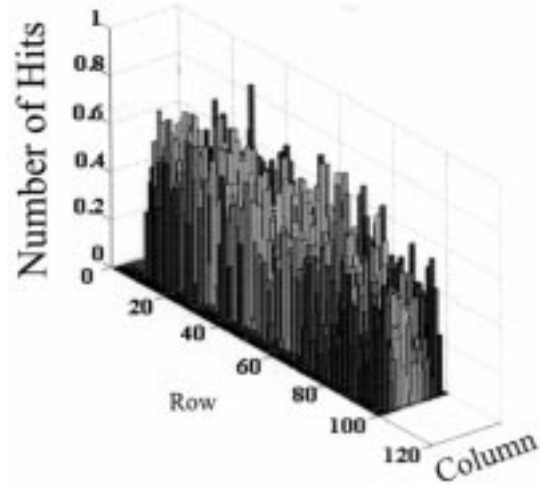


Fig. 8. Pixel chip hit map.

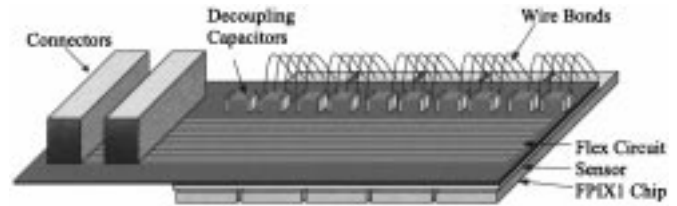


Fig. 9. Sketch of the pixel multichip module.

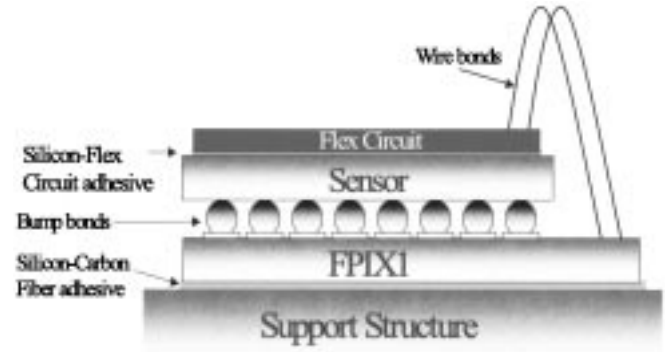


Fig. 10. Sketch of the pixel multichip module "stack" (not to scale).

in performance, indicating no crosstalk problems between the digital and analog sections of the FPIX1 and flex circuit.

IV. SECOND PIXEL MULTICHIP MODULE PROTOTYPE PACKAGING

Fig. 9 shows a sketch of the second pixel multichip module prototype. This design also uses the FPIX1 version of the Fermilab Pixel readout IC.

The pixel module is composed of three layers, as depicted in Fig. 10. The pixel readout chips form the bottom layer. The backs of the chips are in thermal contact with the station support structure, while the other sides are flip-chip bump bonded to the silicon pixel sensor. The clock, control, and power pad interfaces of FPIX1 extend beyond the edge of the sensor [6].

The interconnect circuitry (flex circuit) is placed on the top of this assembly and the FPIX1 pad interface is wire-bonded to the flex circuit. The circuit then extends to one end of the module

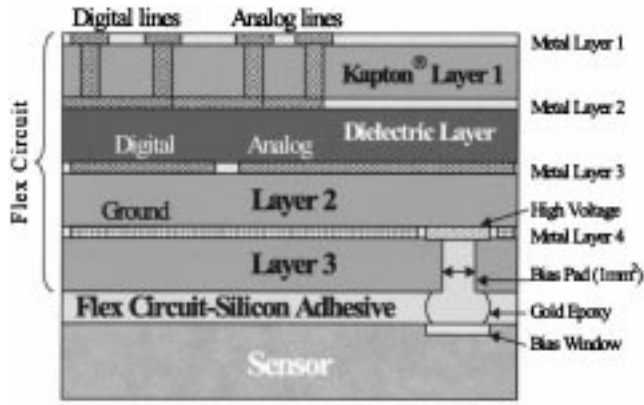


Fig. 11. Sketch of flex circuit cross section.

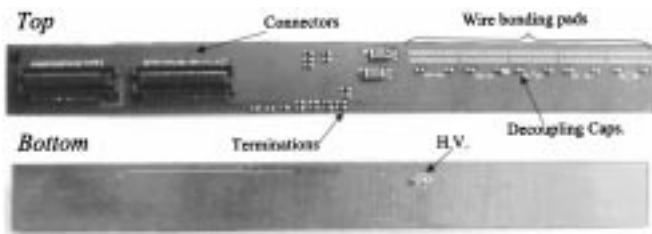


Fig. 12. Flex circuit.

where low profile connectors interface the module to the data acquisition system. The large number of signals in this design imposes space constraints and requires aggressive design rules, such as $35\ \mu\text{m}$ trace width and trace-to-trace clearance of $35\ \mu\text{m}$.

This packaging requires a flex circuit with four layers of copper traces (as sketched in Fig. 11). The data, control and clock signals use the two top layers, power uses the third layer and ground and sensor bias voltage use the bottom layer. The flex circuit has two power traces, one analog and one digital. These traces are wide enough to guarantee that the voltage drop from chip to chip is within the FPIX1 $\pm 5\%$ tolerance. The decoupling capacitors on the flex circuit are close to the pixel chips. The trace lengths and vias that connect the capacitors to the chips are minimized to reduce the interconnection inductance. A picture of the flex circuit made by European Organization for Nuclear Research, Geneva, Switzerland, is shown in Fig. 12.

To minimize coupling between digital and analog elements, signals are grouped together into two different sets. The digital and analog traces are laid out on top of the digital and analog power supply traces, respectively. Furthermore, a ground trace runs between the analog set and the digital set of traces.

A. High Voltage Bias

The pixel sensor is biased with up to 1000 VDC through the flex circuit. The coupling between the digital traces and the bias trace has to be minimized to improve the noise performance. To achieve this, the high voltage trace runs in the fourth metal layer (ground plane, see Fig. 11) and below the analog power supply trace. The high voltage electrically connects to the sensor bias window through gold epoxy. An insulator layer in the bottom of

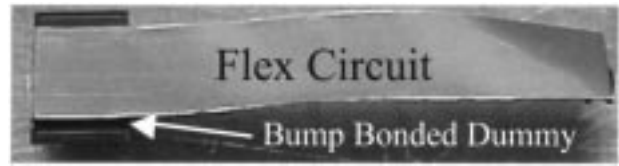


Fig. 13. Dummy bump bond structure.

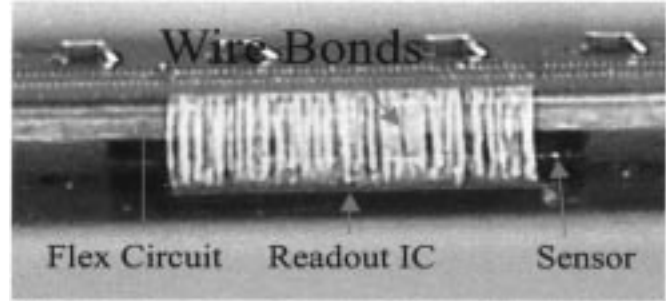


Fig. 14. Pixel module with SINTEF sensor.



Fig. 15. Pixel module without sensor.

the flex circuit isolates the ground in the fourth metal layer of the flex circuit from the high voltage of the pixel sensor.

B. Assembly

The interface adhesive between the flex circuit and the pixel sensor has to compensate for mechanical stress due to the coefficient of thermal expansion mismatches between the flex circuit and the silicon pixel sensor. Two alternatives are being pursued. One is the 3M thermally conductive tape [7]. The other is the silicone-based adhesive used in [8].

The present pixel module prototypes were assembled using the 3M tape with a thickness of 0.05 mm. Before mounting the flex circuit onto the sensor, a set of dummies with bump-bond structures were used to evaluate the assembly process. This assembly process led to no noticeable change in the resistance of the bumps. Fig. 13 shows a picture of the dummy.

V. PIXEL MODULE EXPERIMENTAL RESULTS

Two pixel module prototypes were characterized. One of these modules is a single readout IC (FPIX1) bonded to a SINTEF, Oslo, Norway, sensor (Fig. 14) using indium bumps. In the second pixel module, the readout IC is not bump bonded to a sensor (Fig. 15). In this latter prototype, the flex interconnect is located on the top of the sensor (as in the baseline design).

The pixel modules have been characterized for noise and threshold dispersion. These characteristics were measured by injecting charge into the analog front end of the readout chip

TABLE IV
PERFORMANCE OF THE PIXEL PROTOTYPE MODULES
(IN INPUT e^- EQUIVALENT)

<i>Without Sensor</i>				<i>With Sensor</i>			
μ_{Th}	σ^2_{Th}	μ_{Noise}	σ^2_{Noise}	μ_{Th}	σ^2_{Th}	μ_{Noise}	σ^2_{Noise}
7365	356	75	7	7820	408	94	7.5
6394	332	78	12	6529	386	111	11
5455	388	79	11	5500	377	113	13
4448	378	78	11	4410	380	107	15
3513	384	79	12	3338	390	116	20
2556	375	77	13	2289	391	117	21

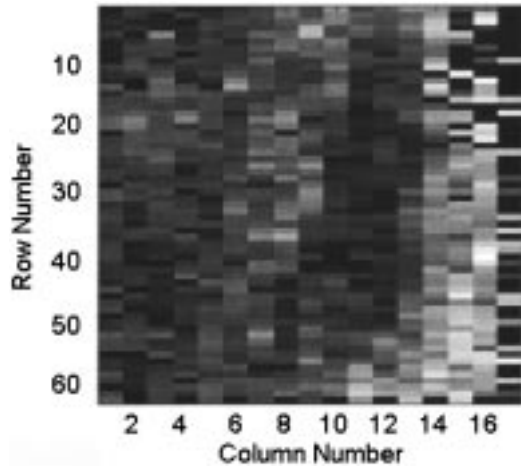


Fig. 16. Pixel hit map.

with a pulse generator and reading out the hit data through a PCI based test stand. The results for various thresholds are summarized in Table IV.

The comparison of these results with previous results (single readout IC without the flex circuit on top) shows no noticeable degradation in the electrical performance of the pixel module [9]. Fig. 16 shows the hit map of the pixel module with sensor using a radioactive source (Sr 90), confirming that the bump bonds remain functional.

VI. RESULTS OF THE HYBRIDIZATION OF SENSOR AND READOUT CHIPS

The hybridization approach pursued offers maximum flexibility. However, it requires the availability of highly reliable, reasonably low cost fine-pitch flip-chip mating technology. We have tested three bump bonding technologies: indium, fluxed solder, and fluxless solder. Real sensors and readout chips were indium bumped at both the single chip and the wafer level by Boeing, NA, Inc., Anaheim, CA, and Advanced Interconnect Technology, Ltd., Hong Kong, with satisfactory yield and performance.

We have recently received a new batch of single chip detectors and modules bumped bonded at AIT. Fig. 17 is a scanning electron micrograph showing the indium bumps deposited on the readout chip. The bumps are about $10\ \mu\text{m}$ high and $12\ \mu\text{m}$ wide at the base. Fig. 18 is a picture of our new five-chip module.

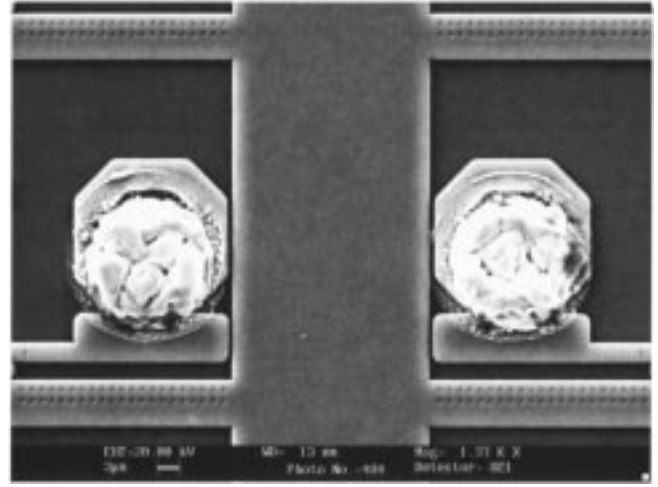


Fig. 17. Indium bumps on the readout chip.

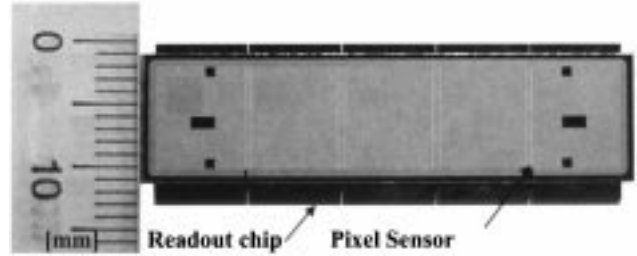


Fig. 18. Five-chip pixel module mated using indium bumps.

We have also conducted tests on dummy detectors (Fig. 13) to evaluate eutectic Pb/Sn solder. The vendor, MCNC, Research Triangle Park, NC, together with UNITE Electronics, Research Triangle Park, NC, produced the dummy parts, and then continued with the bumping process. The detectors are composed of channels that are a number of daisy-chained bumps at $50\ \mu\text{m}$ pitch connected to probe pads at an edge of the dummy detector. We characterized the bump yield by measuring the resistance of each channel, and (to check for shorts) the resistance between neighboring channels.

Both fluxed and fluxless solder bumps have been studied. We found much better results using the fluxless process. The yield from the fluxed process is poor. For the fluxless assemblies, a process called plasma assisted dry soldering (PADS) [10] is used. The bumped chip wafer (top plates of the dummies) and un-bumped substrate wafer (bottom plates of the dummies with only under-bump metallization put on) were diced and tacked together (flip-chip assembly) before being treated in the PADS process. The solder was then reflowed at $250\ ^\circ\text{C}$. After being reflowed, the detectors were rinsed with methanol and dried in air. The diameter of the bumps is approximately $40\ \mu\text{m}$, and the height is approximately $15\ \mu\text{m}$ after mating. The single solder bump resistance is estimated to be less than $1\ \Omega$.

In the fluxed process, flux was introduced to the bumped parts before the reflow. The purpose of the flux is to break through the oxide barrier that is formed on the surface of the bumps which, if left untouched, will prevent a good connection. Due to the corrosive nature of the flux, it has to be washed away with solvents after mating. Problems occurred when rinsing away the

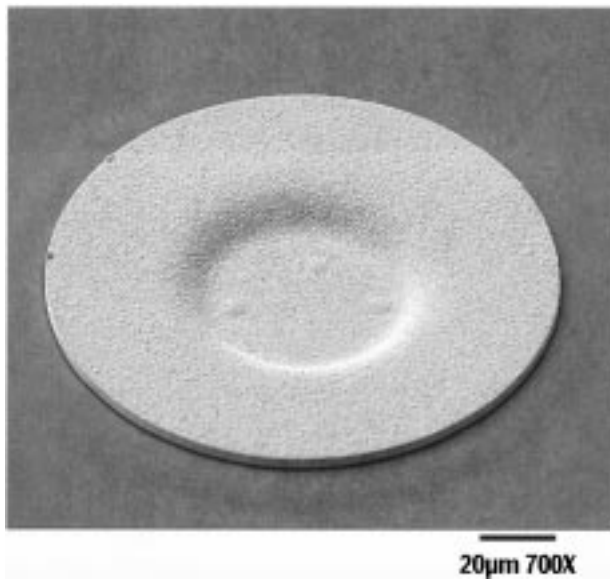


Fig. 19. Gold plated pad.

flux residue because the bumps are small ($15\text{ }\mu\text{m}$ high) and the bump pitch is fine ($50\text{ }\mu\text{m}$). Inspection of the fluxed parts showed that the bumps are dirty, with stain marks and with flux residue spread around the part. Incomplete removal of the flux residues leads to formation of dry joints. Furthermore, the flux residues may attack a good joint.

We have previously reported [11] a bump yield of 99.95% or 4.5×10^{-4} failure/bump. The causes of the failures have been identified and solutions have been adopted to overcome these problems. This has led to changes in the bumping process.

One of the main problems identified was the oxidation of the under bump metallization (UBM) before the solder bumps were put on the part. This thin oxide layer prevents the formation of a good joint until it is “broken” through by the application of an electrical voltage. To overcome this, the vendor has developed a process of gold plating the UBM that prevents the oxidation. Fig. 19 shows an example of the gold plating process.

VII. CONCLUSIONS

The baseline design of a pixel multichip module designed to handle the data rate and other requirements required for the BTeV experiment at Fermilab has been described. The assembly process of a single chip pixel module prototype was successful. A five-chip pixel module prototype (Fig. 18) was assembled using the same process. The characterization of the two single-chip modules showed no degradation in the electrical performance of the pixel module when compared with previous prototypes.

Indium bump bonding is proven to be capable of successful fabrication at $50\text{ }\mu\text{m}$ pitch on real detectors. For solder bumps at $50\text{ }\mu\text{m}$ pitch, good results have been obtained with fluxless PADS-processed dummies. The results are adequate for Fermilab’s pixel module needs, and tests have validated these two processes as viable bump-bonding technologies.

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