

# A Formal Design Methodology for Synthesizing a Clock Signal with an Arbitrary Duty Cycle of $M/N$

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**Abstract**—Nowadays, the emerging research topic on synthesizing logic functions with *chemical reaction networks* (CRNs) have drawn intensive attentions from both academia and industry. By making use of its advantages in power, spontaneity, robustness, and parallelization, a lot of amazing applications of this research topic have been proposed and therefore give this field a promising future. However, in order to properly synthesize sequential logics with CRNs, the difficulties in construct a clock signal with an arbitrary duty cycle turns out to be a bottleneck. To this end, this paper devotes itself in constructing a formal design methodology, which can conveniently generate clock signals with any duty cycle of  $M/N$ . In order to achieve this goal, we put our efforts in steps. First, clock signal with duty cycle of  $1/N$  with  $N \geq 3$  is introduced. Then, the case of  $1/2$  duty cycle is taken care of. Finally, clock signal with duty cycle of  $M/N$  is constructed in a nice manner with the aid of *circle map* representation.

**Keywords**—Clock signal, chemical reaction networks (CRNs), synthetic biology, molecular computing, sequential logic.

## I. INTRODUCTION

Considering the inherent limits of silicon-based technologies, both academia and industry are seeking alternative implementation approaches which are less energy-hungry, more fault-tolerant, more body-akin, and highly parallel. Being one of the most promising candidates, DNA computing has drawn a lot of research interests and therefore triggers a tremendous amount of achievements. Existing literatures [1, 2] have proved that DNA strand displacement technology could be an appropriate experimental basis in mapping an arbitrary *chemical reaction networks* (CRNs) into real DNA reactions. In the 1st step, species like  $X_1, X_2, \dots, X_n$  are employed to construct targeted CRNs. In the 2nd step, those CRNs are synthesized into DNA reaction systems. The 1st step is viewed as the counterpart of “front end” in silicon-based technologies, whereas the 2nd step as the “back end”. Since almost CRNs can be conveniently compiled into real DNA reactions with the aid of tools like *Visual DSD* [3] and *NUPACK* [4], we are safe to only focus on CRNs rather than real DNA reactions.

Without any doubt, clock signal plays an important role not only in traditional electronics but also in “molelectronics”. For traditional electronics, the quartz clock is widely used in electronic computers as the main clock signal to standardize and distribute tasks for modular components. Furthermore, various clock periods could be regenerated by frequency dividers to meet different requirements. For molelectronics, under the instruction of biological clocks, rhythms abound in biological systems, varying from seconds to hours, decide the cellular behaviours like cell division, directed mitosis, apoptosis, as well as evolution. More specifically, when solving the sequential

logic problems in synthetic biology, a biological clock signal, which is tunable in amplitude, period, and duty cycle, turns out to be critical also. By borrowing ideas from the well-established traditional electronics, several interesting works have been introduced recently. In [5], a method to implement a biological oscillator with positive feedback transitions is proposed. Authors of [1] successfully emulated an *Oregonator* (limit cycle oscillator) and the *Lotka-Volterra* chemical oscillator. [6] proposed various biological oscillators with molecular implementation. In [7–9], the authors presented an RGB or RGBY phase clock, addressing the implementation of synchronization and delay elements in sequential computation. Unfortunately, none of those literatures provides us a formal approach to synthesize a biological clock tunable in certain parameter such as duty cycle, amplitude, period, and so on. Since in molelectronics, duty cycle always plays an important role in activity-representation, regulation, and synthesis, this paper devotes itself in synthesizing a biological clock signal with an arbitrary duty cycle of  $M/N$ , where  $M < N$ .

In this paper, we first present a general method to implement a clock signal with the duty cycle of  $1/N$  ( $N \geq 3$ ), based on the works done by researchers from University of Minnesota. After revealing the hidden transference properties behind the RGB(Y) phase clock, we further generalize our method to design a clock signal with duty cycle of  $M/N$ . For better understanding, a *circle map* representation is also proposed. Design examples are also given in this paper. All of the proposed approaches are validated via numerical simulations of the chemical kinetics based on *ordinary differential equations* (ODEs). It is worthy noting that the scaled system of lower rate constants and concentrations maintain the same, albeit scaled, and behavior. Thus, both involved concentration and time are unitless, which will be scaled in an appropriate way for experiments. For more details, please refer to [1, 7].

The remainder of this paper is organized as follows. Section II briefly reviews the preliminaries of RGB(Y) phase clock. Section III presents the proposed (*circle map*)-aided method to generate a clock signal with duty cycle of  $1/N$ . The transference property is pointed out in the same section. Section IV, two different schemes are provided to implement clock signal with duty cycle of  $1/2$ . The latter approach is then generalized the case of  $M/N$  duty cycle clock generation in Section V. Finally, Section VI concludes the entire paper.

## II. PRELIMINARIES OF RGB(Y) PHASE CLOCK

### A. Simulation Model

In order to properly emulate the dynamic behaviours of certain CRNs, the simulation model of ODEs is introduced.

This ODE-based approach is convenient and can perfectly imitate the time-varying evolution of chemical kinetics. The details of extracting ODEs from a CRN is well-described in [10]. Key factors are reactants, rate constants, and products. It is worth noting that although [1] requires each chemical reaction has no more than two reactants, in the rest part of this paper, this constraint is ignored for design convenience. Because we can always decompose reactions with more than 2 reactants into cascaded bimolecular or unimolecular ones [7].

### B. RGB(Y) Phase Clock

The RGB(Y) is used as a shorthand for *red-green-blue-(yellow)*, denoting colors of three or four different equivalent phases. It brings us convenience to distinguish different phases by their colors among simulation waves.

The RGB three-phase clock is a chemical oscillator first presented in [8] by researchers of University of Minnesota. This clock is then better depicted in [7] to deal with challenges aroused by asynchronism in binary counters. Figures in [7] effectively help us to get a quick understanding of this idea. In this paper, our method is illustrated with a similar but more sophisticated way, called *circle map* representation. The RGBY four-phase clock is proposed in [9] by the same authors to implement the stable storage with interference in synchronous sequential combination. For RGBY oscillators, only the dual phases of  $R$  and  $B$  are selected as two phases of the targeted clock signal. Reactions of both the RGB and RGBY oscillators are listed in Table I. Please refer to [7][8][9] for more details.

TABLE I. REACTIONS OF BOTH THE RGB AND RGBY OSCILLATORS.

Clock	Absence	Phase signal	Threshold	Main power
RGB	$\phi \rightarrow r$	$R+r \rightarrow R$	$R+b \rightarrow G+b$	$R+2G \rightarrow 3G$
	$\phi \rightarrow g$	$G+g \rightarrow G$	$G+r \rightarrow B+r$	$G+2B \rightarrow 3B$
	$\phi \rightarrow b$	$B+b \rightarrow B$	$B+g \rightarrow R+g$	$B+2R \rightarrow 3R$
RGBY	$\phi \rightarrow r$	$R+r \rightarrow R$	$R+y \rightarrow G+y$	$R+2G \rightarrow 3G$
	$\phi \rightarrow g$	$G+g \rightarrow G$	$G+r \rightarrow B+r$	$G+2B \rightarrow 3B$
	$\phi \rightarrow b$	$B+b \rightarrow B$	$B+g \rightarrow Y+g$	$B+2Y \rightarrow 3Y$
	$\phi \rightarrow y$	$Y+y \rightarrow Y$	$Y+b \rightarrow R+b$	$Y+2R \rightarrow 3R$

Here, we would like to emphasize two important concepts here: *absence indicator* and *phase signal*. To put it simple, the former concept refers to species written in lowercase letters, namely  $r$ ,  $g$ ,  $b$ , and  $y$ . Whereas the latter concept refers to those written in uppercase letters, namely  $R$ ,  $G$ ,  $B$ , and  $Y$ . Further explanation will be given in the following section.

### III. PROPOSED (Circle-Map)-AIDED $1/N$ DUTY CYCLE CLOCK SIGNAL DESIGN APPROACH

In this section, the proposed (*circle-map*)-aided  $1/N$  duty cycle clock signal design approach is given in detail. It will be shown that this approach comes from the existing RGB(Y) oscillator, but in a simpler and more general way.

#### A. Further Discussion on RGB(Y) Clock

As mentioned above, what an RGB(Y) oscillator realizes is the transference among three or four phase signals. The implementation is based on the following three theorems.

*Theorem 1:* Two concepts of *absence indicator* and *phase signal* are sufficient to construct the logic relationship as a complementary pair.

The proof is immediate and omitted. We provide an example here. When phase signal  $R$  is present, the corresponding absence indicator  $r$  will be absent, and *vice versa*. Thus, their complementary relationship is: phase signal  $R$  represents presence and  $r$  represents absence.

*Theorem 2:* For phase signal species, only the concentration of one initial species is non-zero, whereas the others are all zero.

*Proof:* Quantity transference behind an RGB(Y) oscillation requires the sum concentration remains constant. Hence, only one phase signal species has non-zero concentration. ■

*Lemma 1:* Theorem 2 results in both “absence” and “phase signal” reactions.

*Proof:* Note that the concentration of absence indicator  $r$  is from external injection and fast consumed at the existence of  $R$ . The resulted reactions are  $\phi \rightarrow r$  and  $R+r \rightarrow R$ , listed in the first and second columns of Table I, respectively. ■

*Theorem 3:* Another two kinds of reactions, which are listed in the third and fourth columns of Table I, are required to construct the targeted transference.

*Proof:* For the transference from  $R$  to  $G$ , reactions  $R+b \rightarrow G+b$  and  $R+2G \rightarrow 3G$  are constructed. In the former reaction, absence indicator  $b$  fires the transferring process from  $R$  to  $G$ . No matter how small the concentration of  $b$  is, this reaction will proceed all the way as long as  $b$  exists. During the accumulation of phase signal  $G$ , two  $G$  rapidly interact with one  $R$  to produce three  $G$ . Both concentrations of  $R$  and  $G$  are changed. The sum of their quantities remains the same as the initial concentration of  $R$ . ■

In order to further understand the functions of those reactions we care about, the ODE results without them will be analyzed. In RGB(Y) oscillation, reactions listed in the same column in Table I have the same function, and differ from those in other columns. Since functions of reactions listed in the first and second columns have been well studied, we only focus on reactions in the third and fourth columns. Simulation results without those reactions are illustrated in Figure 1 for further function exploration.

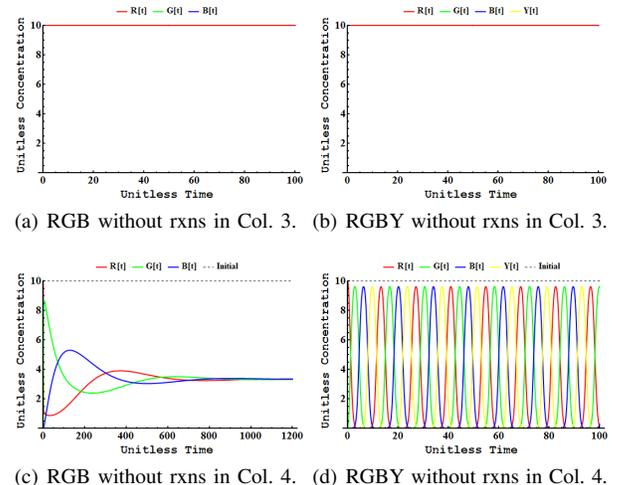


Fig. 1. Simulation results without reactions in the 3rd or 4th column.

*Lemma 2:* Threshold reactions are the key to the wanted transference.

*Proof:* According to Figure 1(a) and 1(b), it is clear that no oscillation exists if reactions in the third column are missing. To this end, those reactions can be treated as the key to start the oscillation. The function of those reactions is similar as the threshold voltage in traditional electronics. Therefore, we call them “threshold reactions”. ■

*Lemma 3:* Reactions in the fourth column are the main power of transference, named “main power reactions”.

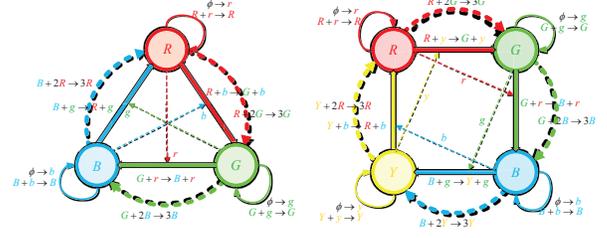
*Proof:* If the reactions in the fourth column are missing, both oscillators will show an attenuation. Illustrated in Figure 1(c) and 1(d), the RGB oscillator has no oscillation after a long time, whereas the RGBY oscillator still oscillates but with a decreasing amplitude. Furthermore, if we check one single phase in detail, we will find that there are actually two phase signals. That means transference from one species to the other is incomplete. However, if we take back reactions in the fourth column, their products will combine with original species, transferring “raw material” to targeted products. Since they help a lot in making the expected transference fast and complete, reactions in the fourth column are viewed as “main power reactions” of the transference. ■

The last but most important issue we would like to point out is, each phase is transferred one by one in a loop, while the concentration of the current phase signal remains constant. Take the phase signal  $R$  as a standing point, the transference process starts from and returns to  $R$  repeatedly in a loop manner. This transference loop will never stop as long as no interruption is introduced. The duration of a single loop is actually the period of the oscillation, which depends on the number of different phase signals participating in it. A single phase signal holds just a fraction of one loop duration. In this manner, one phase signal of RGB or RGBY oscillator realizes a clock with  $1/3$  or  $1/4$  duty cycle, respectively. In general, if there are a total of  $N$  phase signals, each single phase signal implements nothing but a clock with duty cycle of  $1/N$ .

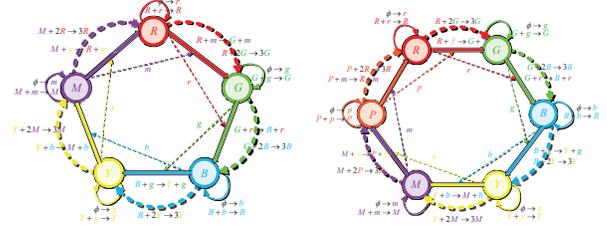
### B. General Construction Approach Based on RGB(Y) Clock

Based on previous analysis, in order to implement a  $1/N$  duty cycle clock signal, we need a total of  $N$  species as the phase signals to transfer quantity. In this sub-section, we will present a simple method based on *circle map* (Figure 2) to make this into reality.

In order to incorporate more phase signals into the clock system, we need to pay more attentions to the reactions in the third column. The key is to choose an appropriate absence indicator species as an *instructor*, which instructs the “threshold” reactions. This instructor should not be the absence indicator of either the “current raw material” or the “current targeted product”. For example, in the reaction  $R+b \rightarrow G+b$ ,  $b$  is an absence indicator of phase signal  $B$ , which is irrelevant of the transference from  $R$  to  $G$ . Now the strategy is immediate: choose the absence indicator of the “raw material” of previous transference as an instructor. This proposed strategy can safely guarantee the quantity has been completely transferred from previous phase signal, and is now or will be changed during the current transference.



(a) Circle map for duty cycle  $1/3$ . (b) Circle map for duty cycle  $1/4$ .



(c) Circle map for duty cycle  $1/5$ . (d) Circle map for duty cycle  $1/6$ .

Fig. 2. Circle maps for clock signals with different duty cycles.

The *circle map* arranges the trace of the entire quantity transference in a round circle, which is partitioned into  $N$  equal segments by  $N$  nodes. Since all the nodes are in equivalent status, rate constants of in the same column stays the same. The round circle illustrates one loop of the oscillation mechanism. The nodes denote  $N$  species participating in the transference. With the help of various colors and arrows shown in the *circle map*, reactions could be easily obtained.

In the equally divided *circle map*, every colored node represents a single phase signal, which is producing or receiving various arrows. The arrow direction indicates the quantity transference flow, while different colors indicate different species are transferred. Still take  $R$  as a starting point.  $R$  node produces four red arrows, respectively: 1) **Arrow.1** (starting from and returning back to the  $R$  node with a curved solid line), 2) **Arrow.2** (towards targeted  $G$  node with a straight solid line), 3) **Arrow.3** (towards targeted  $G$  node with a curved thick dashed line), and 4) **Arrow.4** (towards the next Arrow.2 produced by  $G$  node with a straight dashed line). Those arrows are associated with the four reactions of each single phase: absence indicators injection, phase signal duration, threshold, and main power reaction, respectively.

Now, we would like to point out detailed relationship of four arrows and reactions. Combining **Arrow.1** with its cell-shaped node, logic of presence and absence is well established: the external environment continuously injects the absence indicator at a slow speed, which is fast consumed as soon as the phase signal exists, otherwise a slow accumulation of indicator occurs. Thus **Arrow.1** together with the cell-shaped node are associated with two reactions. Under the instruction of another uncorrelated absence indicator transferred by the previous **Arrow.4**, the transference between two phases is triggered. Therefore **Arrow.2** denotes the start of a threshold reaction. After that, targeted phase species, which is already produced, further accelerates the transference to be complete. For **Arrow.3**, this bold line indicates the corresponding reac-

tion is a main power reaction. **Arrow.4** means if the phase signal is absent, the absence indicator will be released as an instructor for the next transference. Actually, **Arrow.4** aids us in selecting an appropriate instructor. It is not directly related to any explicit reaction but reflects a logic relationship. For better understanding of the proposed *circle map* representation, four clock examples along with all reactions are illustrated in Figure 2. The duty cycles of them are  $1/3$ ,  $1/4$ ,  $1/5$ , and  $1/6$ , respectively. The numerical results are illustrated in Figure 3.

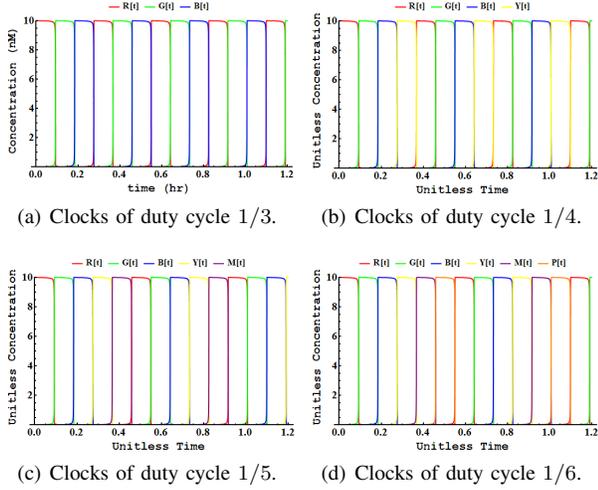


Fig. 3. Numerical simulation results for clocks with different duty cycles.

To sum up, each phase signal requires only four reactions. Therefore, in general a total of  $4N$  reactions are needed to implement a  $1/N$  duty cycle clock signal.

#### IV. IMPLEMENTATION OF $1/2$ DUTY CYCLE CLOCK

Now, we can easily implement  $1/N$  ( $N \geq 3$ ) duty cycle clock signal based on the proposed *circle map*. In both electronics and molectronics,  $1/2$  duty cycle clock signal is very popular and plays an indispensable role. To this end, two different implementation schemes for  $1/2$  duty cycle clock signal are proposed in this section. One scheme is based on RGBY oscillation, and the other one is a novel method based on transference idea. The latter one also provides us the basis of constructing  $M/N$  duty cycle clock in Section V.

##### A. $1/2$ Duty Cycle Based on RGBY

As mentioned in Section II.B, RGBY oscillation is used to produce a non-overlapped two phase clock signal. However, its duty cycle essentially remains  $1/4$ .

Note the denominator 2 of duty cycle indicates that there are two species participating in the transference loop. Therefore, we hope to use two phase signals to realize  $1/2$  duty cycle based on a *circle map* with two nodes. However, it couldn't be implemented without an "instructor" species. Theoretically, we could still obtain the  $1/2$  duty cycle from a RGBY oscillation. Selecting  $R$  and  $B$  phase as the presence and absence of a clock signal, it is desired that the durations of phase signal  $G$  and  $Y$  are extremely close to zero. To this end, the transference processes from  $R$  to  $G$  and  $B$  to  $Y$  should be faster than other two transference processes. In other words, there should be

only two phase signals existing in the entire loop. Therefore, rate constants of the four reactions should be modified to slow down the speed of transference from  $G$  to  $B$  and  $Y$  to  $R$ . In this paper, the speed of transference is slowed down by two orders of magnitude. In addition, the durations of  $R$  and  $B$  in a loop should be the same because of the  $1/2$  duty cycle. This scheme requires a total of **16** reactions.

The corresponding reactions are very similar to those listed in Table I. But the rate constants should be fine-tuned according to what mentioned above. Numerical simulation results are illustrated in Figure 4.

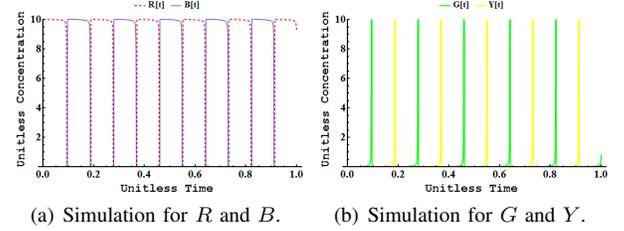


Fig. 4. Numerical simulation results for clocks with 50% duty cycle.

##### B. $1/2$ Duty Cycle Clock Based on Transference Properties

In this subsection, we present a novel method to realize the transference just between two phase signals. The idea of transference is still in use, as well as the tweaking *circle map*. The key step of realizing the transference between two phase signals is how to construct appropriate instructors. To this end, a feedback mechanism is introduced.

Preparations are required first. We use  $clk_0$  and  $clk_1$  to denote the absence and presence of targeted clock signal. These two species are also selected as phase signals in an oscillator.  $in_0$  and  $in_1$  are the corresponding absence indicators for  $clk_0$  and  $clk_1$ , respectively. Instructors are also introduced in this mechanism:  $t_{01}$  instructing the transference from  $clk_0$  to  $clk_1$ , and  $t_{10}$  instructing the transference from  $clk_1$  to  $clk_0$ . For initialization, the quantity of  $clk_1$  is set as non-zero, whereas that of  $clk_0$  is set as zero.

The proposed feedback is implemented as follows. Suppose the initial phase is  $clk_0$ , we need to seek for the instructor  $t_{01}$  as a result. Note that  $clk_1$  doesn't exist, while its absence indicator  $in_1$  exists. We transfer  $in_1$  to  $t_{01}$  with the current phase  $clk_0$  as a catalyst. This process implies the next phase signal will occur because its corresponding absence indicator  $in_1$  is transferred to  $t_{01}$ . Then the produced  $t_{01}$  will instruct the transference from  $clk_0$  to  $clk_1$ , and the presence of  $clk_1$  will rapidly consume  $in_1$  without any effects on  $t_{01}$ . Similarly,  $t_{10}$  is produced with raw material " $in_0$ " with the help of  $clk_1$ . Since the required amount of the instructor species is not high, this method could successfully introduce the wanted instructors in the original system.

Then, we make a further analysis from a standpoint of chemical reactions. Take  $in_0$  as a starting point. Similar to the general implementation, logic should be well established at first. So comes the former two reactions in both two columns. Note that  $in_0$  exists in the  $clk_1$  phase and we hope to transfer this phase to  $clk_0$ . With the help of phase signal  $clk_1$ , one

molecules of  $in_0$  is consumed to produce one molecules of instructor  $t_{10}$ , transferring  $clk_1$  to the next phase signal  $clk_0$ . Under the instruction of  $t_{10}$ , both “threshold” and “main power” reactions will be fired. However, the instructor  $t_{10}$  will be accumulated during the transference and excessive  $t_{10}$  will hinder the next transference from  $clk_0$  to  $clk_1$ . Theoretically, in the  $clk_0$  phase, we hope  $t_{10}$  will not exist. So comes the last reaction in the left column. Similarly, we could obtain reactions shown in the right column.

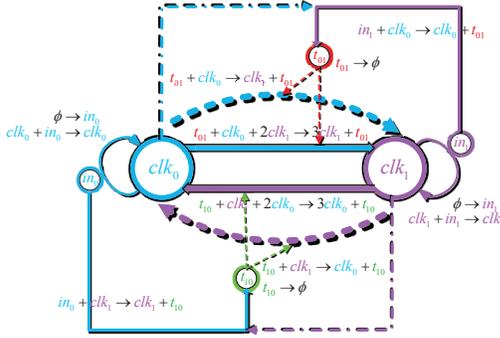


Fig. 5. Circle map for duty cycle 1/2.

Finally, we illustrate the reactions in the modified circle map in Figure 5. The numerical results are given in Figure 6. Four small nodes are added into our map to represent absence indicators or instructors. This modified circle map helps us in understanding and constructing chemical reactions. This scheme requires a total of 12 reactions.

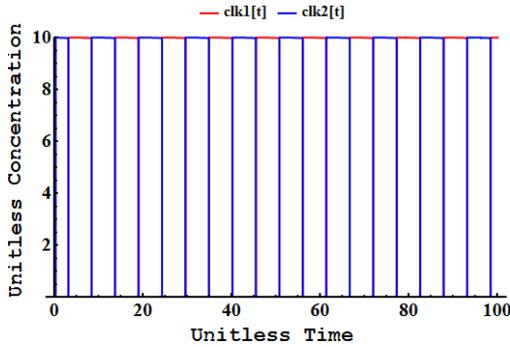


Fig. 6. Numerical results for our novel 1/2 duty cycle clock.

## V. PROPOSED (Circle-Map)-AIDED $M/N$ DUTY CYCLE CLOCK DESIGN

### A. Combined Two-Circle Map Approach

A clock signal is represented by two molecules:  $clk_0$  and  $clk_1$ . The oscillation will be realized via repeated transference between them. Since different duty cycles mean various durations of  $clk_0$  and  $clk_1$ , adjustment of the two durations will result in arbitrary duty cycle in principle. Therefore, the transference between  $clk_0$  and  $clk_1$  is the basis of the construction of  $M/N$  duty cycle. Here we propose a *phase-signal-controlling-duration* method to produce both denominator  $N$  and numerator  $M$  by circle map, respectively.

The proposed method is based on the implementation of  $1/N$  duty cycle. A total of  $N$  nodes are required to implement

the denominator  $N$ . Suppose the initial phase signal is  $clk_1$ . The required  $M/N$  duty cycle means  $clk_1$  keeps its current state for  $M$  time units if one loop of the entire transference consumes  $N$  time units. Therefore, the transference towards  $clk_0$  is required at the end of  $M$ -th time unit. At the end of the  $N$ -th time unit, transference towards  $clk_1$  will be triggered. This periodic transference between  $clk_0$  and  $clk_1$  readily constructs the required clock.

Here a total of two combined circle maps are required. The first map (**C-map1**) with  $N$  nodes gives the entire period of  $N$  time units, successfully implementing an  $N$ -phase oscillator. The second map (**C-map2**) is the same as the one mentioned in Section IV.B, which realizes the transference between two logic states of one clock signal. Construction approach is based on the theoretical analysis mentioned above. During the operation of the  $N$  phase oscillator, time is measured by an  $N$ -segmented loop repeatedly. In the  $M$ -th segment, we use the  $M$ -th phase signal in **C-map1** to instruct and control the transference from  $clk_1$  to  $clk_0$  in **C-map2**. Similarly in the  $N$ -th segment of a loop, we use the  $N$ -th phase signal in **C-map1** to control the reverse transference back to  $clk_1$  phase. The durations of two phase signals in **C-map2** will be respectively controlled by the  $N$ -th and  $M$ -th phase signal, respectively. This is how the name of *phase-signal-controlling-duration* comes from. Therefore, with the operation of both two maps, we successfully make the duty cycle of  $clk_1$   $M/N$ . Meanwhile, clock signal with duty cycle of  $1-M/N$  is also obtained by checking  $clk_0$ . To sum up, the basic idea of our method is to use an  $N$ -phase map to decide when the required transference occurs, and another map to decide how the clock signal transference is implemented.

Take a 3/8 duty cycle clock signal as an example. We use an 8-phase RGBYMPQF oscillator in **C-map1** (Figure 7) to divide the loop duration of the clock signal in **C-map2** into 8 equal segments. Take  $R$  phase in **C-map1** as a starting point. Since all 8 phases are labelled in order,  $B$  and  $F$  are the 3rd and 8th phases, respectively. Combining reactions in both maps, we need a total of 44 ( $= 8 \times 4 + 12$ ) reactions. The corresponding four selected reactions are listed here.

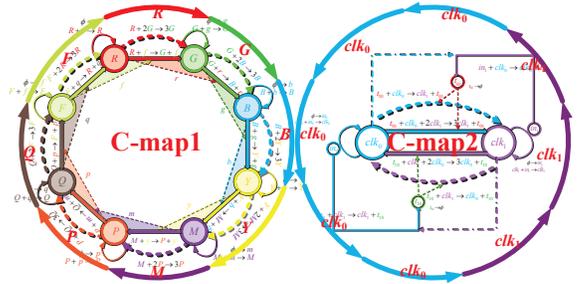
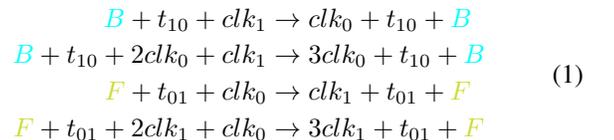


Fig. 7. Circle map for the 8-phase RGBYMPQF oscillator.



As mentioned above, we could obtain 5/8 duty cycle clock by detecting the complimentary signal  $clk_0$ . Similarly, shown

TABLE II. REACTIONS FOR OUR NEW 1/2 DUTY CYCLE CLOCK.

State	$clk_1$	$clk_0$
Absence	$\phi \rightarrow in_1$	$\phi \rightarrow in_0$
Phase signal	$clk_1 + in_1 \rightarrow clk_1$	$clk_0 + in_0 \rightarrow clk_0$
Instructors	$clk_1 + in_0 \rightarrow clk_1 + t_{10}$	$clk_0 + in_1 \rightarrow clk_0 + t_{01}$
Threshold	$t_{10} + clk_1 \rightarrow clk_0 + t_{10}$	$t_{01} + clk_0 \rightarrow clk_1 + t_{01}$
Main power	$t_{10} + 2clk_0 + clk_1 \rightarrow 3clk_0 + t_{10}$	$t_{01} + 2clk_1 + clk_0 \rightarrow 3clk_1 + t_{01}$
Annihilation	$t_{10} \rightarrow \phi$	$t_{01} \rightarrow \phi$

in Figure 8 we could implement clock signal with 1/8, 2/8, 4/8, ..., and even arbitrary  $M/N$  duty cycle.

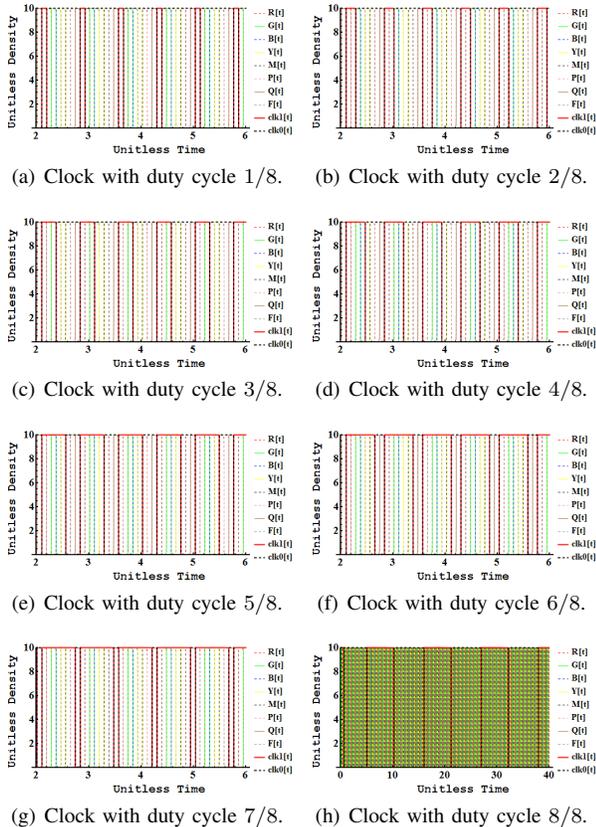


Fig. 8. Numerical simulation results for clocks with  $M/8$  duty cycle.

### B. Further Remarks

Actually, the method we proposed here is not only suitable for adjusting duty cycle. We can further adjust amplitude and period of clock signals by changing the corresponding concentration (quantity), order of the  $M$ -th and  $N$ -th phases, and the absolute value of denominator  $N$ , respectively.

Another thing is, like we can divide the frequency or clock period in traditional electronics, we can do similar thing to clock generated here by accumulating the duration of  $N$  phase oscillator. For example, to implement both 1/2 duty cycle, we could use 1/2, 2/4, 4/8, ...,  $N/2N$ . The only difference among them is the duration of a loop transference in **C-map2**.

## VI. CONCLUSION

This paper proposes a formal design methodology to synthesize a clock signal with an arbitrary duty cycle. Approaches

to generate clock signals with duty cycles of  $1/N$  ( $N \geq 3$ ),  $1/2$ , and  $M/N$  are introduced in step. Based on the transference idea, a novel *circle map* representation is introduced to simplify the construction of required CRNs. Numerical results have shown that the proposed methodology is efficient.

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