Optimal Voltage Signal Sensing of NAND Flash Memmory for LDPC Code

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Abstract—**Low-density parity-check (LDPC) code can provide stronger error correcting performance in NAND flash memory. LDPC decoder requires accurate soft-decision log-likelihood ratio (LLR) information which demands fine-grained flash memory threshold voltage sensing operations. The threshold voltage sensing operations incur energy consumption and access latency penalty. Therefore, it is important to minimize the flash memory sensing operations without noticeable error correcting performance decreasing. We propose a new flash memory sensing strategy Ununiform-SOR (ununiform sensing in overlapping region) which can reduce 20% flash memory sensing operations than traditional non-uniform threshold voltage sensing without reducing the error correcting performance of LDPC code in NAND flash memory noise channel. The new Ununiform-SOR sensing strategy can reduce more than 20% reading energy consumption than the non-uniform sensing strategy. The abstract goes here.**

I. INTRODUCTION

NAND flash memory has been prevailed in billions of electronic products such as laptops, mobile phones and the promising solid-state drives (SSDs). NAND flash memory is divided into single-level cell (SLC, 1 bit/cell), multi-level cell (MLC, 2 bits/cell), and three-level cell (TLC, 3 bits/cell). The n bits in the NAND flash memory can be represented by using 2^n non-overlapping threshold voltage windows and a voltage window represents a storage state. The threshold voltage of each flash memory cell can be obtained by flash memory reading operation. Hard-decision information is obtained by using only one quantization level between two adjacent storage states. While soft-decision information must use more than one quantization levels between two adjacent storage states. NAND flash memory cells become smaller feature size. Meanwhile, NAND flash memory is disturbed by different kinds of noises so that the reliability and endurance of NAND flash memory are greatly reduced. It must use more and more sophisticated fault-tolerance techniques such as error correcting codes (ECC) to ensure the data integrity of NAND flash memory device.

The advances in semiconductor process technology increases the storage density of NAND flash memory device. However, the quality of threshold voltage signal sensed from memory cell is also reduced. The error correcting capability of BCH [1] code with hard-decision information is not sufficient to meet the reliability requirements of MLC NAND flash memory. Low-density parity-check (LDPC) [2], [3] as one of the promising candidates has been widely researched. In the NAND flash memory noise channel, LDPC decoder with soft-decision information requires accurate soft-decision LLR information which demands fine-grained flash memory threshold voltage sensing. The threshold voltage sensing will incur energy consumption and access latency. Therefore, it is important to minimize the flash memory threshold voltage sensing without reducing the error correcting performance of LDPC codes in NAND flash memory noise channel.

In this paper, we propose a new flash memory threshold voltage sensing strategy (Ununiform sensing in overlapping region-Ununiform-SOR) as the input information of LLR computation for LDPC code in the NAND flash memory. The new Ununiform-SOR sensing strategy carries out ununiform threshold voltage sensing whithin the three mainly overlapping regions in MLC NAND flash memory channel. While the traditional non-uniform sensing strategy [4] applies an uniform sensing within the overlapping regions. The new Ununiform-SOR sensing strategy can effectively reduce the memory sensing operations nearly 20% than the traditional non-uniform sensing strategy without the error correcting performance of LDPC code decreasing. Furthermore, we derive a reading energy mathematical model about NAND flash memory and compare the reading energy consumption between the new Ununiform-SOR sensing strategy and non-uniform sensing strategy.

The rest of the paper is organized as follows. In Section 2, we give a description of the non-uniform sensing strategy of MLC NAND flash memory. Then, the proposed new threshold voltage sensing strategy is introduced in Section 3. The reading energy comsumption model is given in Section 4. Section 5 concludes the paper.

II. NON-UNIFORM STRATEGY FOR NAND FLASH MEMORY NOISE CHANNEL

The threshold voltage sensing of NAND flash memory is strongly affected by various noises, such as cell-to-cell coupling (CCI) [5], [6], data retention errors [7], random telegraph noise (RTN) [8]. These noises are mainly affected by
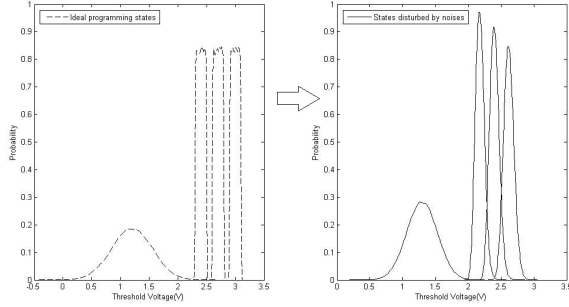
Fig. 1. Threshold voltage distribution of MLC NAND flash memory. The left is ideal threshold voltage distribution. The right is threshold voltage distribution disturbed by noises.
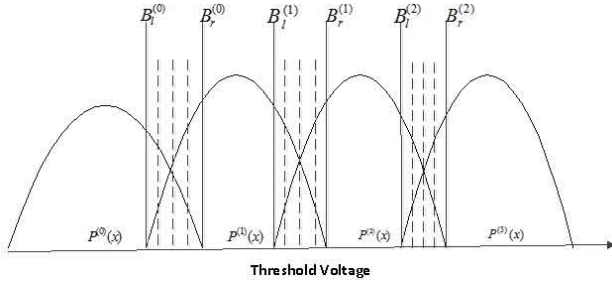

Fig. 2. Non-uniform sensing strategy. Three dominating overlapping regions have uniform 15 threshold voltage sensing operations. $P^i(x)$ denotes the PDF of storage state 0, 1, 2, 3.

the data retention time and the number of program-erase (PE) cycles. Fig. 1 showns that the ideal flash memory programming states which four storage states have gap each other. Because each storage state corresponding to the flash memory threshold voltage is different, this ideal state has no threshold voltage signal sensing error occurring. After disturbed by various noises, the four storage states in MLC NAND flash memory intersect each other. When we carry out threshold voltage signal sensing, storage state determination through threshold voltage sensing will occur error within the three mainly overlapping regions in the NAND flash memory noise channel.

Non-uniform sensing strategy [4] is proposed in order to reduce the number of flash memory threshold voltage sensing levels when soft-decision LDPC code is used in NAND flash memory. It carries out a uniform fine-grained soft-decision memory sensing within overlapping voltage regions while no sensing outside of overlapping regions as shown in Fig. 2.

The implementation of non-uniform sensing strategy is based on different entropy values for the given threshold voltage. The paper found that the entropy value of threshold voltage within the overlapping region is higher than that of outside of overlapping regions. Then it adopted more uniform threshold voltage sensing operations within overlapping region while no threshold voltage sensing outside of overlapping region in the NAND flash memory channel. The non-uniform sensing strategy reduce the number of threshold voltage sensing compared with the uniform threshold voltage sensing.

The entropy [4] of a given threshold voltage V_{th} can be obtained as

$$H(V_{th}) = -\sum_k (P(state = k|V_{th})) \log_2 P(state = k|V_{th})$$

(1)

For MLC NAND flash memory, a page consists of a LSB page and a MSB page. A flash memory cell stores 2 bits. Therefore, a flash memory cell has four storage states. The four storage states are 11, 01, 00 and 10. We use 0, 1, 2, 3 to represent the four storage states. $P(state = k|V_{th})$ denotes the probability density function (PDF) of storage state k for a given threshold voltage V_{th}. For the given threshold voltage V_{th}, the LLR information of the i-th bit stored in a cell is computed as

$$LLR(b_i) = ln \frac{P(b_i = 1|V_{th})}{P(b_i = 0|V_{th})}$$

(2)

The LLR information are inputted to the LDPC decoder as initial soft-decision information.

The key of non-uniform sensing strategy is how to get the borders of three overlapping regions. The border $B_l^{(i)}$ and $B_r^{(i)}$ are obtained [4], [9] by solving

$$\frac{P^{(i)}(B_l^i)}{P^{(i+1)}(B_l^i)} = \frac{P^{(i+1)}(B_r^i)}{P^{(i)}(B_r^i)} = R$$

(3)

R is a constant. $P^{(i)}(x)$ is the threshold voltage distribution of the storage state i. In addtion, the length of the overlapping region is reduced as the R decreases. On the other hand, the threshold voltage distribution will change according to the PE cycle and the data retention time. In fact, it is impossible to estimate the exact threshold voltage distribution. In this paper, $P^{(i)}(x)$ is assumed as a Gaussian function as shown in Fig. 1.

III. NEW UNUNIFORM-SOR SENSING STRATEGY

The error correcting performance of soft LDPC decoding is closely related to the precision of LLR information. Therefore, the way of increasing the precision of LLR information becomes very important. As mentioned above, the non-uniform memory sensing strategy [4] is desired which gives a high precision threshold voltage signal sensing in NAND flash memory. The reason is that the entropy value within the threshold voltage overlapping region is larger than that outside of the overlapping region.

For the non-uniform sensing strategy, the threshold voltage sensing is uniformly implemented within the three mainly overlapping regions as shown in Fig. 2. However the entropy values are different in the three threshold overlapping regions. When the entropy value is big, the error occurring rate is higher which needs more threshold voltage signal sensing in the overlapping region. Therefore we propose a new Ununiform-SOR threshold voltage signal sensing strategy which carries out ununiform voltage signal sensing within the mainly three overlapping regions.
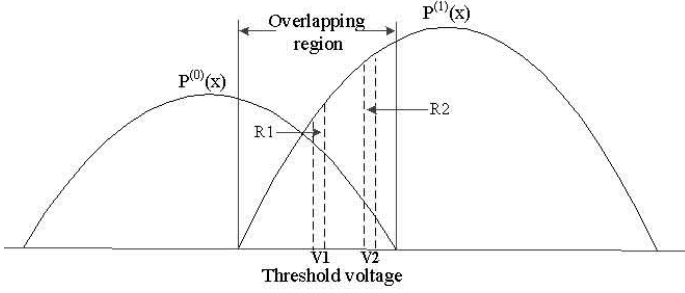
Fig. 3. Entropy computation illustration in the first overlapping region.

Fig. 4. Entropy of threshold voltage in the first overlapping region.

A. Different entropy within overlapping region

We use the first overlapping region as an example to illustrate the entropy computation for different threshold voltages as shown in Fig. 3. According to the equation 1, the entropy of a given threshold voltage is the related items sum of all four storage states. A cell of MLC NAND flash memory has 4 storage states 0, 1, 2, 3. The storage state 0 represents the erasing state 11, and the storage states 1, 2, 3 represent the programming state 10, 00, 01, respectively. In the first overlapping region, the entropy of two storage states 0, 1 are not zero and the entropy of other two storage states 2, 3 are zero. In order to compute $P(state = k|V_{th})$ (k=0, 1, 2, 3) for a given threshold voltage V_{th}, we compute the integration of $P^{(i)}(x)$ of storage state k to get $P(state = k|V_{th})$. We define a small region Ri which the given threshold voltage Vi is located in the region Ri. The width of R1 is equal to that of R2.

$$P(state = k|V1) = \int_{R1} P^{(k)}(x)\,dx \qquad (4)$$

$$P(state = k|V2) = \int_{R2} P^{(k)}(x)\,dx \qquad (5)$$

For the given threshold voltage $V1$ and $V2$, their entropies are computed as

$$H(V1) = -\sum_{k=0}^{3}(P(state = k|V1))\log_2 P(state = k|V1) \qquad (6)$$

$$H(V2) = -\sum_{k=0}^{3}(P(state = k|V2))\log_2 P(state = k|V2) \qquad (7)$$

According to equation 4 and 5, in the first overlapping region of NAND flash memory channel, the entropy of storage states 2, 3 are zero. The equation 6 and 7 can be simplified as

$$H(V1) = -(\log_2 P(state = 0|V1)^{P(state=0|V1)} \\ + \log_2 P(state = 1|V1)^{P(state=1|V1)}) \qquad (8)$$

$$H(V2) = -(\log_2 P(state = 0|V2)^{P(state=0|V2)} \\ + \log_2 P(state = 1|V2)^{P(state=1|V2)}) \qquad (9)$$

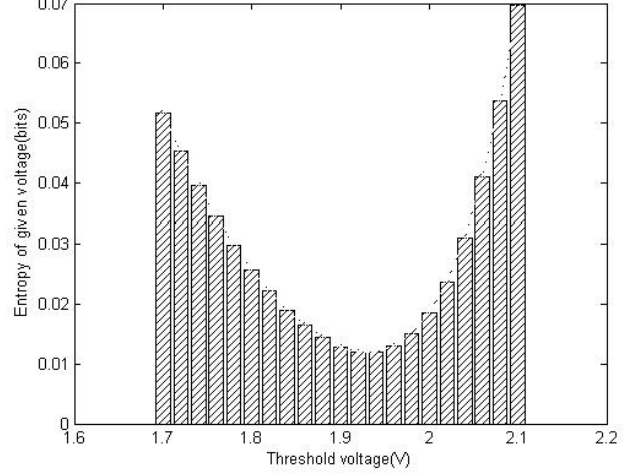If we know $P^{(i)}(x)$ of storage state k, the entropy will

be obtained according to the above equations. Because the two PDF $P^{(0)}(x)$ and $P^{(1)}(x)$ are different after disturbed by various noises, the entropy of two different threshold voltage $V1$ and $V2$ are different.

Given the two Gaussian PDF in the first overlapping region, $P^{(0)}(x) = N(1.1, 0.4^2)$ and $P^{(1)}(x) = N(2.5, 0.2^2)$. The threshold voltage overlapping region is $[1.7, 2.1]$ between $P^{(0)}(x)$ and $P^{(1)}(x)$. The width of Ri is 0.02 V. According to the above equations 4-7, we can get the entropy of the given threshold voltage in the first overlapping region as shown in Fig. 4. We find that the entropy of threshold voltage in the center of overlapping region is smaller than that of threshold voltage on the edge of overlapping region. For example, the entropy of the leftmost threshold voltage 1.7 V in the first overlapping region is 0.0518 bit and the entropy of the rightmost threshold voltage 2.1 V is 0.069 bit. The entropy of the central threshold voltage 1.9 V is 0.0126 bit. The entropy of the right border in the first overlapping region is more than 5 times that of the central voltage. Furthermore, the entropy of the left border in the first overlapping region is also more than 4 times that of the central voltage. Therefore, according to the above analysis, we should adopt more threshold voltage signal sensing near the border of overlapping region as shown in Fig. 5. Meanwhile, we carry out less threshold voltage sensing in the center of the overlapping region.

B. Eorr correcting performance of LDPC code using new Ununiform-SOR sensing strategy

In this section, we will verify the error correcting performance of LDPC code using the new Ununiform-SOR sensing strategy.

A MLC NAND flash memory cell has 2 bits which are mapped to two papes: least significant bit page (LSB) and most significant bit page (MSB) respectively. The threshold volatge level is discriminated by the number of electrons stored in the flash memory cell. With the developing of flash memory
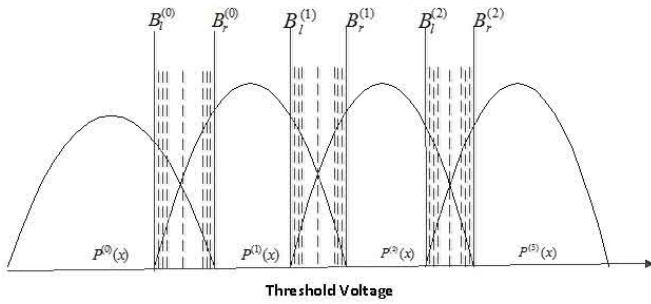
Fig. 5. Ununiform sensing strategy in the three threshold voltage overlapping regions.
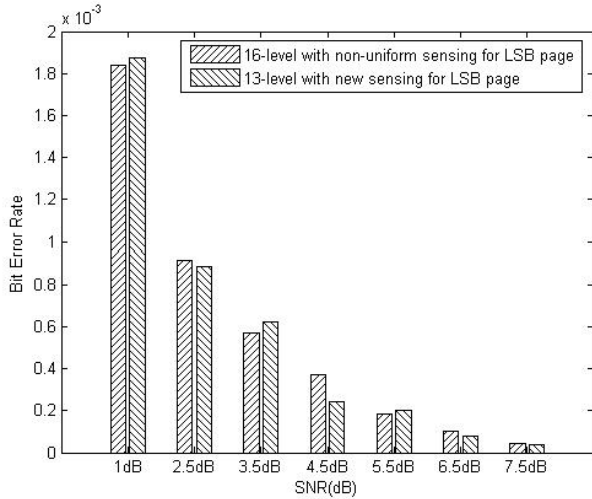

Fig. 6. BER Performance of LDPC code between 16 levels non-uniform sensing and new 13-level sensing for LSB page.

Fig. 7. BER Performance of LDPC code between 16 levels non-uniform sensing and new 13-level sensing for MSB page.

technology, the number of electron in a cell is reduced. The threshold voltage margin is also decreased. Therefore, Various noises caused by PE cycles and data retention time will cause a substantial change in the threshold voltage distribution. Different PE cycles and data retention time cause different threshold voltage distribution of flash memory which generate different threshold voltage sensing error. LDPC code [2] with soft-decision information have better error correcting performance than that using hard-decision information. The error correcting performance of LDPC code is dependent on the accuracy of the signal-to-noise (SNR) ratio according to [10]. To provide reliable SNR information to LDPC decoder, it is important to estimate the threshold voltage distribution accurately of NAND flash memory. In this paper, the threshold voltage distribution of actual NAND flash memory is modeled as a Gaussian mixture [11] [12] as shown in Fig. 1. By conducting multiple flash memory voltage sensing operations and computing the LLR information according to the equation 2, LDPC code can get the input soft-decision information for decoding. The threshold voltage distribution of four storage states is not only widened but also shifted to the negative direction due to CCI, data retention, RTN noises. Therefore,
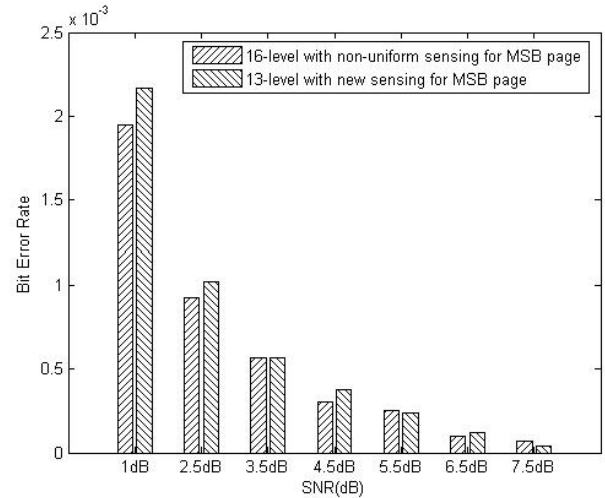
it will occur error voltage sensing information and furtherly result in the error LLR information. LDPC decoder can correct these errors.

In this paper, the size of flash memory page is 2 K. Because a page consists of LSB page and MSB page, the size of LSB page and MSB page is 1 K. The number of PE cylces is changed from 1 k to 10 K times which generate different noises, while the data retention time is fixed to 10 years. We use 16-level non-uniform threshold voltage sensing strategy as a baseline which requires 15 flash memory threshold voltage sensing operations. For the proposed new sensing strategy, we use 13-level threshold voltage sensing to compare with 16-level non-uniform sensing in the error correcting performance of LDPC code. A (9102, 8192) Random LDPC code with min-sum [9], [13] decoding algorithm is used and the LDPC code rate is 0.9. The number of threshold voltage sensing operation is reduced from 15 to 12.

The error correcting performance of LDPC code using the new Ununiform-SOR sensing strategy is not significantly affected as shown in Fig. 6 (LSB page) and Fig. 7 (MSB page). At some SNR points, the bit error rate (BER) performance after LDPC decoding using new sensing strategy is better than the 16 levels non-uniform sensing strategy. For example, the BER performance after LDPC decoding for LSB page with the new sensing strategy exceeds that of non-uniform sensing strategy at SNR 4.5 dB point as shown in Figure 6. With the increasing of SNR, the BER performance gap between the non-uniform sensing strategy and new sensing strategy is gradually reducing due to the reduced noises. Since the number of threshold voltage sensing using the new Ununiform-SOR sensing strategy is reduced by 20% compared with that using the non-uniform sensing strategy, the energy consumption of threshold voltage sensing operation is also reduced.

TABLE I
THE PARAMETERS OF NAND FLASH ENERGY CONSUMPTION.

V_{cc}	3.3V
V_{ccq}	1.8V
I_{cc}	25mA
I_{io}	20mA
T_R	12.5 us
N_s	15 or 12
T_{clk}	10ns
T_{RC}	$0.5T_{clk}$
$N_{bytes-page}$	2048 bytes
N_b	4(16level) 3.8(13level)

IV. READING ENERGY CONSUMPTION

For NAND Flash memory, the reading unit is a page. The process of reading data out from NAND Flash memory involves *addressing*, *flash array access* and *reading data output*. The first *addressing* time is five clocks. The second *flash array access* time is related to the number of threshold voltage memory sensing levels. The last *reading data out* time is proportional to the number of bits per page. According to the paper [14]–[16], the reading energy consumption of NAND Flash memory is computed as

$$E_{addressing} = 5V_{cc}I_{cc}T_{clk} \qquad (10)$$

$$E_{access} = V_{cc}I_{cc}T_R N_s \qquad (11)$$

$$E_{readingout} = V_{ccq}I_{io}T_{read} \qquad (12)$$

$E_{addressing}$, E_{access}, $E_{readingout}$ denote the energy consumption of *addressing*, *flash array accessing*, *reading data output* per page (LSB & MSB page), respectively. V_{cc}, V_{ccq} denote the core and I/O voltages respectively. I_{cc}, I_{io} represent the core and I/O currents. T_R represents NAND Flash memory access time per threshold voltage memory sensing level. T_{read} denotes data output time which is related to the number of bits per page and NAND Flash memory clock. $T_{read}=T_{RC}\times N_b\times N_{bytes-page}$, T_{RC} denotes read cycle time. A voltage sensing is stored in N_b bits, where $N_b = \log_2(N_s + 1)$. $N_{bytes-page}$ represents the number of bytes of a NAND Flash page. N_s denotes the number of threshold voltage memory sensing.

NAND Flash memory has asynchronous mode and synchronous mode. In this paper, we adopt synchronous data output mode which has the minimum energy consumption of the data output operation. We assumes that NAND Flash memory operates at 100 MHZ, so the NAND Flash clock period T_{clk}=10 ns. Table I shows some parameters in 34-nm MLC NAND in synchronous mode from Micron technology [14].

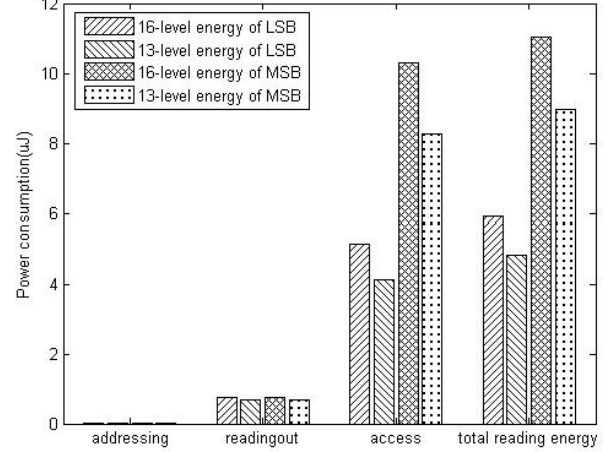A NAND Flash memory page consists of LSB page and

Fig. 8. Reading energy consumption of 16-level non-uniform sensing and new 13-level sensing for a LSB/MSB page.

MSB page which are read simultaneously. Moreover, the number of threshold voltage sensing of MSB page is two times that of LSB page [15], the energy consumption of *flash array access* from LSB page is one-third of that from a NAND flash memory page, and the remaining two-thirds of the *flash array access* energy consumption is from MSB page. The energy consumption of *reading data out* from LSB and MSB page are equal which are half of the energy consumption from a NAND flash memory page. Therefore, we can get the reading energy consumption of LSB and MSB page as follows:

$$E_{lsb} = \frac{E_{access}}{3} + \frac{E_{readingout}}{2} + \frac{E_{addressing}}{2} \qquad (13)$$

$$E_{msb} = \frac{2E_{access}}{3} + \frac{E_{readingout}}{2} + \frac{E_{addressing}}{2} \qquad (14)$$

Based on the above equation 10-14 and parameters in Table I, we can compute the reading energy consumption of LSB/MSB page as shown in Fig. 8.

The energy consumption of *addressing* is not related to the memory voltage sensing. Moreover, its energy consumption makes up a very small proportion of the total reading energy consumption of NAND flash memory page which is negligible. Only the energy consumption of *access* and *readingout* are related to the threshold voltage sensing operation. The energy consumption of *access* is especially affected by the number of flash memory sensing. For a MSB page, the energy consumption of 16-level using non-uniform sensing strategy is 25% higher than that of 13-level using new Ununiform-SOR sensing strategy. In addtion, the energy consumption of 16-level sensing is also 20% higher than that of 13-level sensing for a LSB page. Howerver, the energy consumption of *readingout* is not affected seriously by the number of flash memory sensing. For the total reading energy consumption of a flash memory page, the energy consumption decreasing rate can reach 23% for a MSB page when it use the new Ununiform-SOR sensing

strategy. Meanwhile, the energy consumption decreasing rate can reach 20% for a LSB page using the new Ununiform-SOR sensing strategy.

V. CONCLUSION

In this paper, we are concerned about how to reduce the number of threshold voltage signal sensing without reducing the error correcting performance of LDPC code in NAND flash memory. The error correcting performance of soft LDPC code is closely related to the threshold voltage sensing distribution in NAND flash memory. The rule of different entropy values within the overlapping region is verified based on the definition formula of entropy. We propose a new threshold voltage Ununiform-SOR sensing strategy which carries out ununiform threshold voltage signal sensing within the three mainly threshold voltage overlapping regions of MLC NAND flash memory. The new threshold voltage sensing strategy can effectively reduce the number of flash memory threshold voltage signal sensing compared with the traditional non-uniform threshold voltage sensing strategy. The error correcting performance of LDPC code using the new voltage sensing is almost same as that using non-uniform voltage sensing. The experimental results show that the new voltage sensing strategy can reducing nearly 20% voltage sensing operations while keeping the error correcting performance of LDPC code in NAND flash memory channel. In addtion, the reading energy consumption of the new sensing strategy can be declined by more than 20% compared with the non-uniform sensing strategy.

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