Advanced Multichip Module Packaging of Microelectromechanical Systems

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SUMMARY

Multichip module (MCM) packaging provides an efficient solution to integration of MEMS with microelectronics. In this paper, new methods of packaging MEMS using two advanced MCM foundry processes are described. A special purpose surface micromachined MEMS packaging test chip was designed and fabricated. The MEMS test die was packaged with CMOS electronics die using the "chips first" General Electric high density interconnect (HDI) technology and the Micro Module System MCM-D process.

Keywords: multichip modules, packaging, micro-electro-mechanical systems

INTRODUCTION

Monolithic integration of MEMS and microelectronics can be complicated by incompatibilities in the fabrication of MEMS and integrated circuits. An alternative approach to the integration and packaging of MEMS and electronics is to use multichip modules (MCMs). MCM technology has significantly improved over the last decade in response to requirements for better packaging and performance in microelectronics [1]. MCMs offer an attractive approach to integrating and packaging MEMS because of the ability to support a variety of die types in a common substrate without requiring changes or compromises to either the MEMS or electronics fabrication processes. Furthermore, MCMs offer design flexibility by providing packaging alternatives to handle a host of applications envisioned for microsystems.

One of the primary goals of the research described in this paper is to explore methods of leveraging the advances in microelectronic MCM technology for the packaging of MEMS. In particular, the interest is in using foundry fabricated MEMS and MCM technologies which will provide a means for volume production of microsystems as these products make the transition from research and development to commercial manufacturing.

MEMS PACKAGING TEST DIE

The MEMS packaging test die was designed to provide a disciplined method of evaluating the compatibility of MEMS with MCMs. Sandia National Laboratory developed the concept of using specially designed chips for evaluating the impact of assembly and packaging on microelectronics [2]. Their Assembly Test Chip (ATC) series of test die are designed to monitor the health and performance of integrated circuits during manufacturing, packaging, and operation. Our MEMS packaging test die incorporates a variety of devices and test structures designed to assess the impact of foundry MCM packaging on MEMS. The MEMS packaging test chip was fabricated using the Multi-User MEMS Processes (MUMPs). The MUMPs process is a three layer polysilicon surface micromachining technology sponsored by the Defense Advanced Research Projects Agency (DARPA) [3]. Silicon dioxide is the sacrificial material in this MEMS process and is removed with a wet etch in hydrofluoric acid.

The test die contains a variety of devices and test structures designed to monitor the ability of the surface micromachined MEMS devices to survive a foundry packaging process. Among the test structures are breakage detectors to monitor excess force and polysilicon resistors to monitor excess heating. Other devices on the die are representative of MEMS structures which might be used in an actual application. Table 1 lists general categories of devices on the MEMS packaging test die.

Table 1. MEMS Device Categories Included on Test Die.

Device Category
Breakage Detectors
Polysilicon Resistors
Variable Capacitors
Thermal Actuators
Flip-Up and Rotating Devices
Electrostatic Piston Mirrors
Electrostatic Comb Drives

MCM TECHNOLOGIES

High Density Interconnect Process

The standard high density interconnect (HDI) process consists of embedding bare die into cavities milled into a base substrate and then fabricating a thin-film interconnect structure on top of the components. Each layer in the HDI interconnect overlay is constructed by bonding a sheet of dielectric film on the substrate and forming via holes through a laser ablation process. The Ti/Cu/Ti metallization used for the die interconnects is then created through sputtering and photolithography. This process is repeated for each layer in the overlay [4]. Figure 1 shows the HDI process flow.

The HDI process has several attractive features for MEMS and electronics packaging. The die interconnects have very

low parasitic capacitance and inductance due to the use of direct metallization as opposed to wirebonds. HDI packaged systems can operate at well over 1 GHz [5]. Other benefits include extensions to three dimensional packaging, the ability to locate bond pads virtually anywhere on the die, and MCM reparability [4].

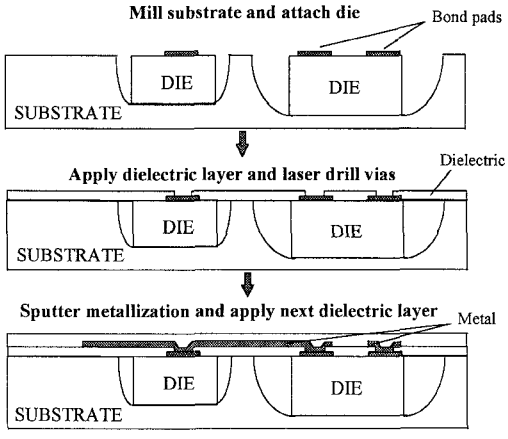

Figure 1. Standard HDI process (after W. Daum, et al. [4]).

MCM-D Process

The Micro Module System (MMS) MCM-D process is a more traditional packaging approach where the interconnect layers are deposited on the substrate and the die are mounted above the interconnect layers. The interconnect between the die and the substrate is made through wirebonding. The MMS MCM-D is one of three foundry processes offered by MIDAS [6]. We chose the MMS process because its substrate and wiring materials are most compatible with the release procedure for MUMPs die as explained in the following section.

MCM PACKAGING AND POST-PROCESSING

HDI Packaging

For MEMS packaging, the standard HDI process was modified to allow physical access to the MEMS die. The MEMS test die and a generic CMOS electronics die were packaged at the General Electric Corporate Research and Development Center using the standard HDI procedure. The MEMS die were not released before packaging due to concerns that the fragile MEMS devices would not survive the packaging process. After passivation, windows in the dielectric overlay above the MEMS die were selectively opened using laser ablation. The ablation was accomplished with a continuous argon ion laser (350 nm wavelength). The initial laser power was approximately 1.6 W. After the bulk of the overlay material was ablated, the laser power was reduced to minimize the likelihood of device damage due to the laser.

Figure 2 shows the HDI/MEMS package before release, and Table 2 lists package characteristics.

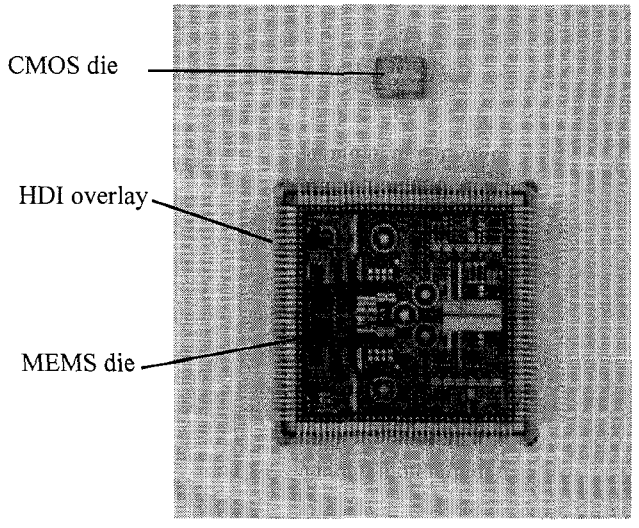

Figure 2. HDI/MEMS MCM package prior to release of MEMS die.

Table 2. Characteristics of HDI/MEMS Package.

Property	HDI
Substrate material	Alumina
Signal/power wiring layers	Variable (1 layer used in this research)
Overlay dielectric material	Kapton
Conductor metallization	Ti/Cu/Ti
Die attach adhesive	Ultem
Die interconnect method	Direct metallization
Die edge-to-edge spacing	> 375 μm
Max operating frequency [4]	> 1 GHz

After HDI packaging, the MEMS die were released using the procedure shown in Table 3. Material compatibility tests conducted prior to packaging indicated that the Kapton dielectric, adhesives, and alumina substrate used in the HDI package would survive the MEMS release procedure. The release of the packaged MEMS die was successful with no evidence of MEMS device 'stiction' to the substrate or deterioration of the HDI package.

Table 3. MEMS/MCM Release Procedure.

1. Etch in 49% hydrofluoric acid for 2 min. 15 sec.
2. Rinse in deionized water for 5 minutes
3. Rinse in 2-propanol for 5 minutes
4. Dry on hot plate at 50 °C

Most of the MEMS devices on the packaged test die performed electrically and mechanically the same as devices on unpackaged control die. Rotating, hinged and flip-up

devices moved freely and operated as designed. In addition, some of the devices were operated through the HDI pads which demonstrated good continuity through the overlay and onto the MEMS die. Finally, the HDI overlay protected the CMOS die from the release etch as predicted by the material chemical compatibility tests. Figure 3 shows a close-up view of selected MEMS devices.

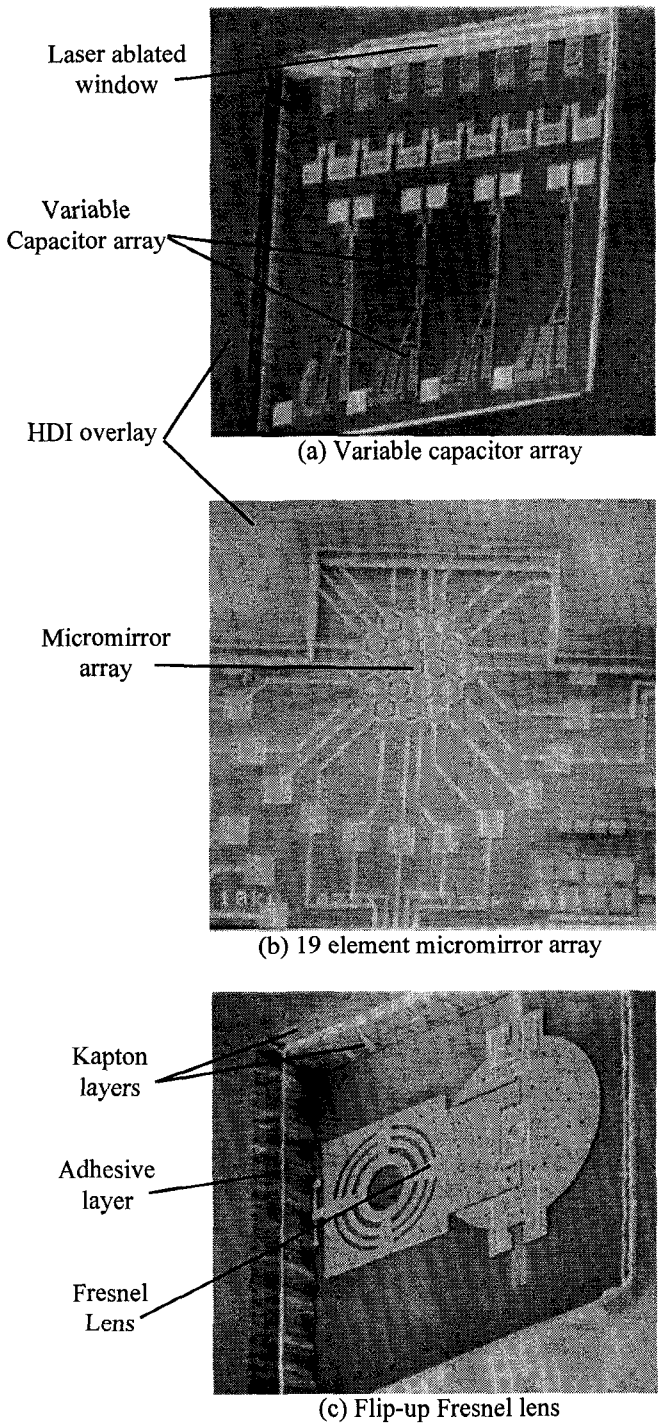

Figure 3. Scanning electron micrographs of HDI packaged MEMS devices.

Each layer of Kapton dielectric is nominally 25 μm thick, and the adhesive layer thickness is typically 2-3 μm. Therefore, the depth of the laser ablated windows is approximately 50-55 μm. The Kapton and adhesive layers can be discerned in Figure 3 (c).

The most serious problem discovered during testing was MEMS device warping or failure due to excessive heating from laser ablation. Devices most susceptible to overheating were long, thin structures with poor heat loss paths to the substrate such as the thermal actuators shown in Figure 4. Polysilicon resistors in areas which received high laser ablation power also showed resistance drops of 10-15% which is consistent with the change in resistance typically encountered during polysilicon resistor trimming [7].

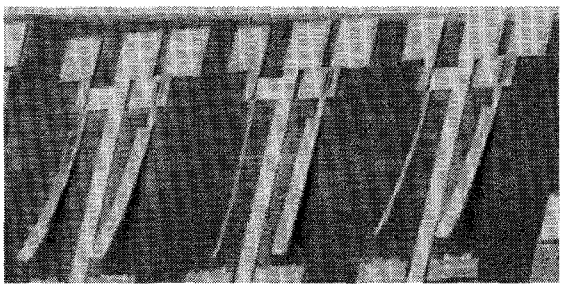

Figure 4. Polysilicon lateral thermal actuators warped due to excessive laser ablation power.

MCM-D Packaging

MEMS packaging test chips were also sent to the DARPA sponsored MIDAS Foundry Access Service for MCM-D packaging. Figure 5 shows a photograph of the MCM-D/MEMS package, and Table 4 lists the characteristics of the MCM-D/MEMS package.

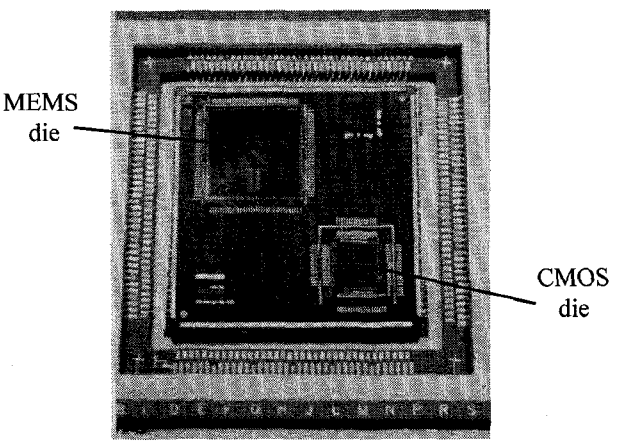

Figure 5. MCM-D/MEMS package.

As opposed to the HDI process where the CMOS die is protected by the overlay, the CMOS die in the MCM-D package is on the surface of the module. Consequently, this

die required a mask for protection from the hydrofluoric acid used in the MEMS release etch. Testing of various encapsulants and photoresists demonstrated that Waycoat HR-200 negative photoresist is an effective mask against the etch used for releasing MUMPs die. The CMOS die was coated with the Waycoat HR-200 photoresist, and the module was soft baked for 20 minutes at 60 °C. The procedure in Table 3 was then used to successfully release the devices on the MEMS die with no impact to the CMOS chip or MCM wiring.

Table 4. Characteristics of MCM-D/MEMS Package.

Property	MMS MCM-D
Substrate material	Aluminum
Signal/power wiring layers	3/2
Dielectric material	Polyimide
Conductor metallization	Copper
Die attach adhesive	Ablebond 789-3
Die interconnect method	Wirebond
Die edge-to-edge spacing	> 500 μm
Max operating frequency [6]	100 - 400 MHz

CONCLUSIONS

The "chips first" General Electric (GE) high density interconnect (HDI) technology and the Micro Module System (MMS) MCM-D process were used to demonstrate the feasibility of packaging surface micromachined MEMS in foundry MCM processes. Both HDI and MCM-D packaging of the MEMS test die was generally successful; however, the potential for device damage in HDI processing due to laser ablation is a concern. The use of a specially designed MEMS packaging test die was particularly useful in identifying and diagnosing this problem.

The outcome of this research has several implications for MEMS and microsystems. First, integrating MEMS and microelectronics in advanced MCMs can be a flexible alternative to monolithic fabrication. This is particularly important for spaceborne applications which have unique qualification requirements that may be difficult to achieve with a monolithic process. In addition, advanced MCM packaging such as HDI can improve the performance and capabilities of MEMS when the packaging environment is factored into the design of the overall microsystem. For example, the HDI overlay can be used to create multilevel wiring over the MEMS die without the need to modify or compromise the MEMS fabrication process.

Finally, the importance of test structures dedicated to the effects of packaging and assembly was affirmed. Failure modes of MEMS devices can differ significantly from macroscale devices and microelectronics. More work is needed to identify MEMS specific structures for examining packaging effects on microsystems.

On-going research includes improvements to the HDI/MEMS packaging process, MCM packaging of LIGA and bulk micromachined devices, and functional integration of MEMS and CMOS electronics in MCMs.

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