Total Ionizing Dose Radiation Effects on 14 nm FinFET and SOI UTBB Technologies

Harold Hughes, Patrick McMarr, Michael Alles, Enxia Zhang, Charles Arutt, Bruce Doris, Derrick Liu, Richard Southwick and Philip Oldiges

Abstract-- **14 nm technology node bulk silicon FinFETs and SOI FinFETs and 14 nm SOI Ultra-Thin-Body and BOX nFETs were irradiated under bias using a 10 keV X-ray source. Irradiation resulted in significant changes in the threshold voltages of the SOI devices and large changes in the off-state current of the bulk FinFETs.**

I. INTRODUCTION

CMOS downscaling beyond 32 nm is proceeding to either FinFET technology for high performance, or Ultra-Thin-Body and BOX (UTBB) planar technology for low power applications. In this paper we present total ionizing dose (TID) radiation effects data for 14 nm UTBB and 14 nm bulk silicon FinFET and SOI FinFET technologies.

During the past decade channel length downscaling of partially-depleted (PD) CMOS/SOI has resulted in technology progressively less sensitive to TID effects. Commercial 32 nm PD CMOS/SOI nFET transistors are 300 times less TID sensitive than nFET transistors from earlier commercial 150 nm PD CMOS/SOI technology [1-3]. These trends are shown in Fig. 1.

As shown in Fig. 1, scaling from 32 nm to 14 nm results in an increase in TID sensitivity or a turnaround in the TID vulnerability trend. 14 nm bulk and SOI FinFETs and SOI UTBB FinFETs show this turnaround in the TID response. For example, the TID-induced increase in off-state current for 14 nm SOI FinFET technology is nearly the same as 90 nm PD CMOS/SOI.

In addition to reduced doping to manage short-channel effects, scaling to 14 nm high performance technologies requires a major change in architecture, from a planar two dimensional (2D) layout to a three dimensional (3D) FinFET geometry. Before this change in geometry, and due to the partially-depleted aspect of technologies prior to the 14 nm node, channel doping was high and resulted in reduced TID sensitivity from radiation induced charge in isolation oxides. With lower channel doping required for scaled generations of UTBB and FinFETs, radiation-induced charge trapping in dielectric spacers, shallow trench isolation oxides and the buried oxides of SOI devices can have a significant impact on threshold voltage and off-state current [4].

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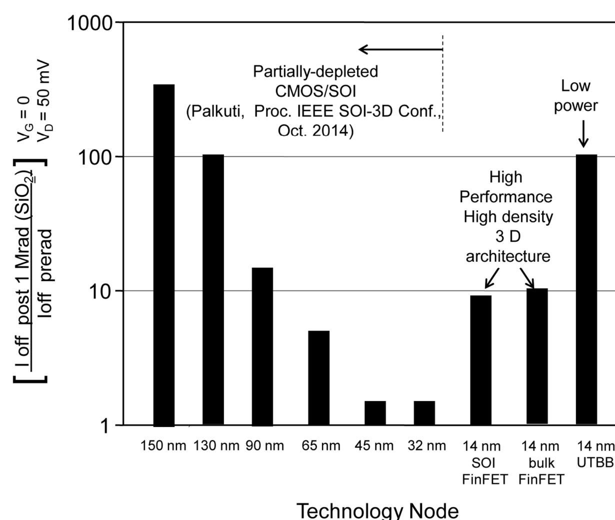

Fig. 1. Commercial Technology TID response of off-state current for a dose of 1 Mrad (SiO_2) versus technology scaling showing vulnerability turnaround after 32 nm.

II. TID RESULTS-SOI FINFETS

14 nm SOI FinFET technology was evaluated using nFETs consisting of 24 fins, each fin 50 nm high and 10 nm wide. The channel length of the FinFET was 20 nm. These nFETs were irradiated using a 10 keV X-ray source (ARACOR Model 4100) at a dose rate of 517 rad(SiO_2/s) to a total dose of 1 Mrad(SiO_2). Three bias conditions were used; ON, OFF and pass gate (PG).

Fig. 2 shows the SOI FinFET current/voltage curves for ON bias during irradiation (V_G = +0.85 V, V_D = V_S = V_B = 0 V), Fig. 3 shows the current/voltage curves for OFF bias (V_D

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= +0.85 V, $V_G = V_S = V_B = 0$ V) and Fig. 4 shows the results for PG bias ($V_D = V_S = +0.85$ V, $V_G = V_B = 0$ V).

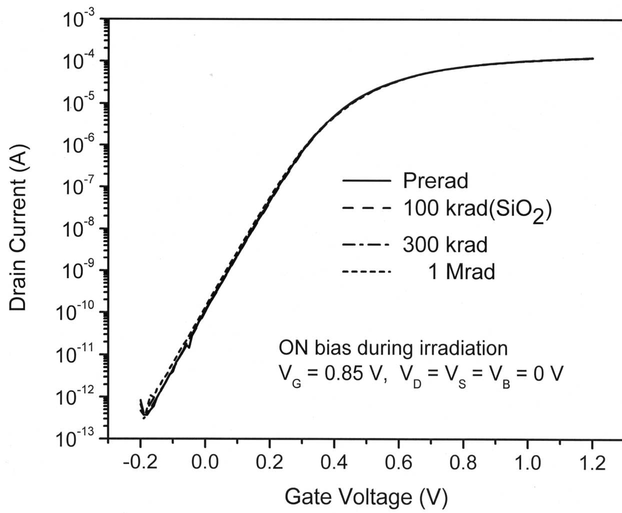

Fig. 2. Current-voltage characteristics versus 10 keV X-ray dose (517 rad(SiO_2)/s) for 14 nm SOI nFinFETs (V_D = +50 mV). ON bias during irradiation.

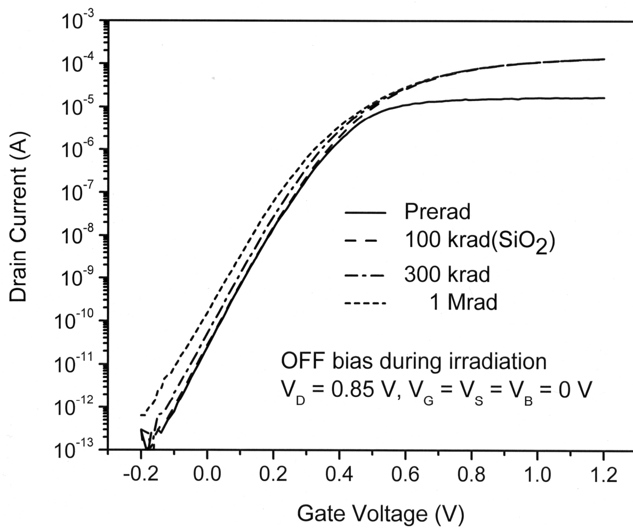

Fig. 3. Current-voltage characteristics versus 10 keV X-ray dose (517 rad(SiO_2)/s) for 14 nm SOI nFinFETs (V_D = +50 mV). OFF bias during irradiation.

Fig. 5 is a summary of the threshold voltage shifts of SOI FinFETs as a function of TID in the linear region (V_D = +50 mV) for the three bias conditions during irradiation. Worse case is OFF bias with a threshold voltage shift of -39 mV at 100 krad(SiO_2), -52 mV at 300 krad(SiO_2) and -63 mV at 1Mrad (SiO_2).

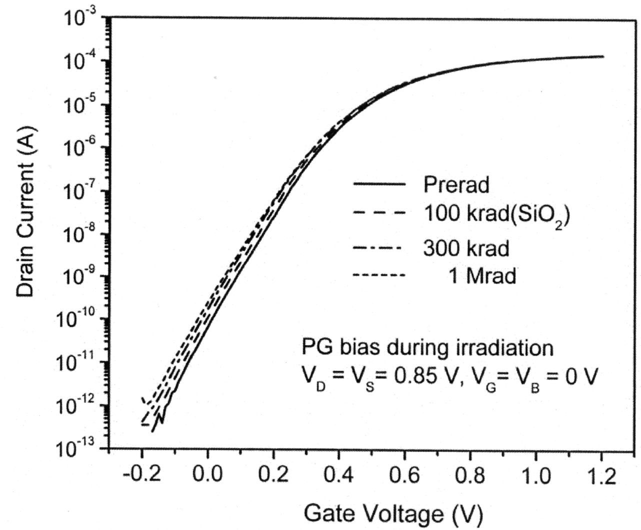

Fig. 4. Current-voltage characteristics versus 10 keV X-ray dose (517 rad(SiO_2)/s) for 14 nm SOI nFinFETs (V_D = +50 mV). PG bias during irradiation.

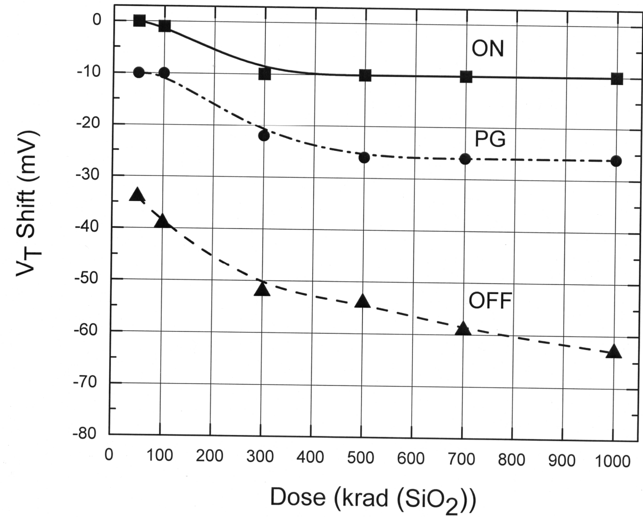

Fig. 5. Threshold voltage shifts versus 10 keV X-ray dose (517 rad(SiO_2)/s) for 14 nm SOI FinFETs biased ON, OFF and PG during irradiation.

III. TID RESULTS-BULK FINFET

14 nm bulk silicon FinFET technology was evaluated using nFETs consisting of 24 fins, each 50 nm high and 10 nm wide. The device channel length was 20 nm. These nFETs were irradiated to a total dose of 1 Mrad(SiO_2) using the 10 keV X-ray source. Two bias conditions were used; ON and OFF. Figs. 6 and Fig. 7 show the bulk silicon FinFET current/voltage curves for ON bias during irradiation in the linear (V_D = +50 mV) and saturation (V_D = +800 mV) regions. Figs. 8 and Fig. 9 show characteristic curves for OFF bias during irradiation.

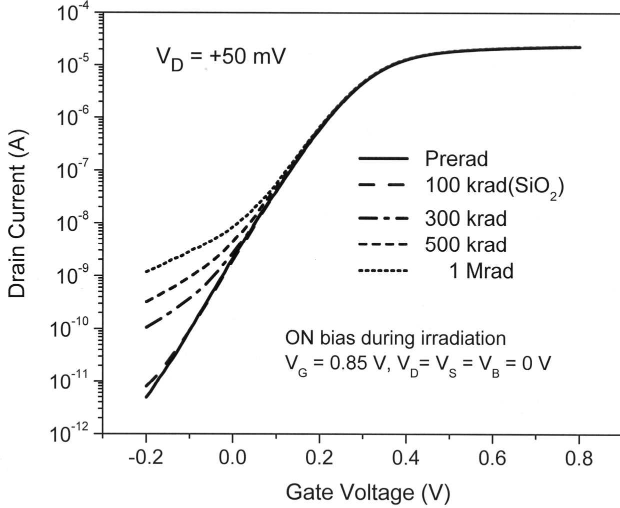

Fig. 6. Current-voltage characteristics versus 10 keV X-ray dose (517 rad(SiO_2)/s) for 14 nm bulk nFinFETs in the linear region (V_D = +50 mV). ON bias during irradiation.

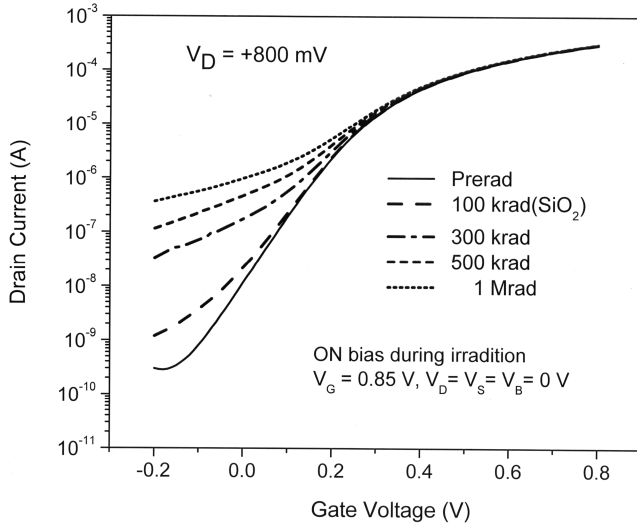

Fig. 7. Current-voltage characteristics versus 10 keV X-ray dose (517 rad(SiO_2)/s) for 14 nm bulk nFinFETs in saturation (V_D = +800 mV). ON bias during irradiation.

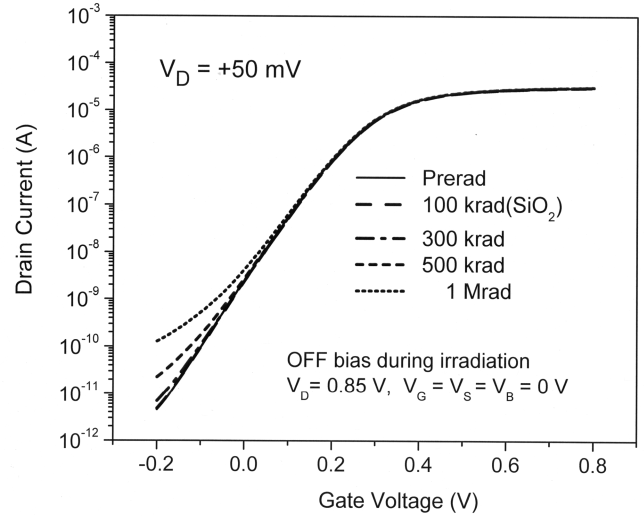

Fig. 8. Current-voltage characteristics versus 10 keV X-ray dose (517 rad(SiO_2)/s) for 14 nm bulk nFinFETs in the linear region (V_D = +50 mV). OFF bias during irradiation.

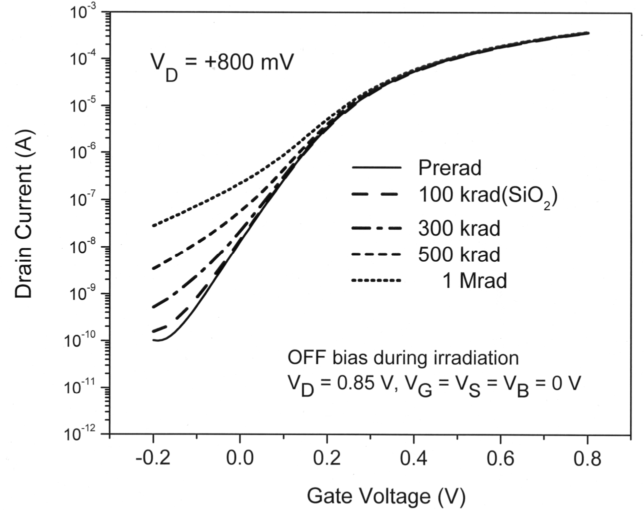

Fig. 9. Current-voltage characteristics versus 10 keV X-ray dose (517 rad(SiO_2)/s) for 14 nm bulk nFinFETs in saturation (V_D = +800 mV). OFF bias during irradiation.

As shown in Fig. 6 and Fig. 8 there is no significant change in threshold voltage (determined from the linear region) following irradiation for the two bias conditions, but large increases in off-state current as shown in Fig. 7 and Fig. 9 (saturation). Fig. 10 is a summary of off-state current as a function of X-ray dose for the bulk silicon FinFETS. ON bias is the worst case for off-state current increase.

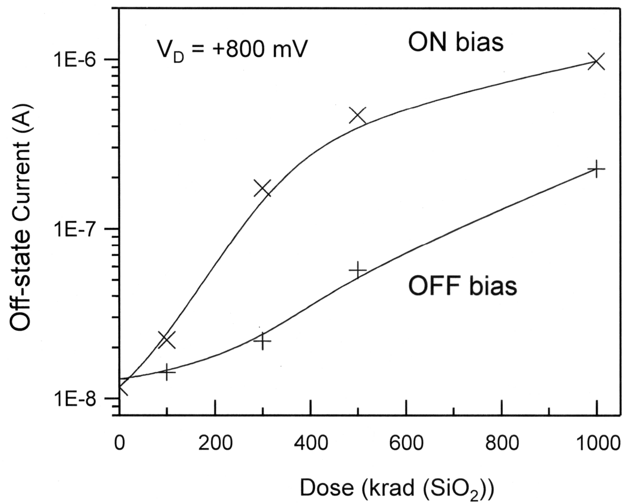

Fig. 10. 14 nm bulk FinFET off-state current increase following 10 keV X-ray irradiation (517 rads(SiO_2)/s) for ON and OFF bias during irradiation (saturation V_D = +800 mV).

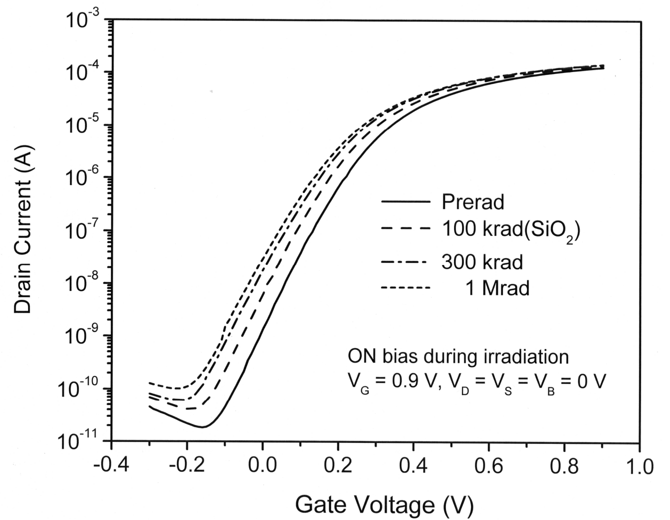

Fig. 11. Current-voltage characteristics versus 10 keV X-ray dose (517 rad(SiO_2)/s) for 14 nm SOI UTBB nFETs (V_D = +50 mV). ON bias during irradiation.

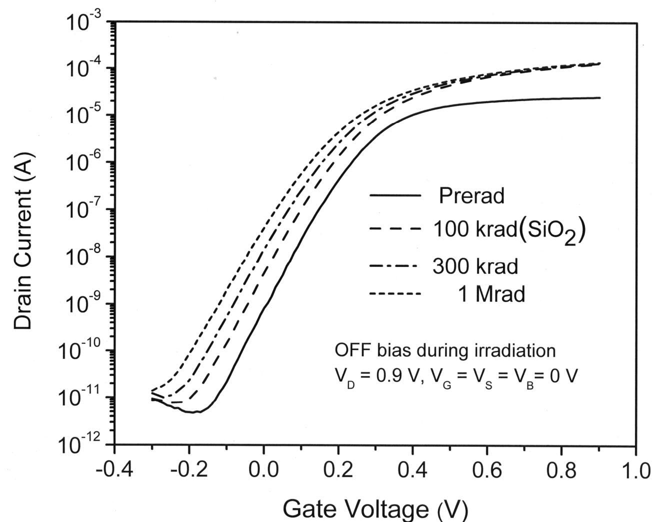

Fig. 12. Current-voltage characteristics versus 10 keV X-ray dose (517 rad(SiO_2)/s) for 14 nm SOI UTBB nFETs (V_D = +50 mV). OFF bias during irradiation.

IV. Discussion TID Results-FinFETs

The TID responses of bulk silicon and SOI FinFETs are significantly different in terms of radiation-induced threshold voltage shift and radiation-induced off-state current increase. Bulk silicon FinFET radiation tolerance is reduced due to an increase in off-state current, and SOI FinFET radiation tolerance is reduced due to threshold voltage shifts.

For SOI FinFETs, OFF bias during irradiation results in the largest threshold voltage increase. For the bulk silicon FinFETs, ON bias during irradiation results in the largest increase in off-state current and this occurs when the device is operated in saturation.

V. TID Results-SOI UTBB FETs

The use of fully depleted (FD) UTBB for scaling CMOS/SOI technology below 32 nm provides a number of major advancements over partially depleted (PD) CMOS/SOI: short-channel electrostatic control, reduced stage delay time, and reduced single event transients. As a planar technology, compared to 3D FinFET technology, UTBB also provides a way for backside threshold voltage control.

The UTBB nFETs were fabricated on SOI substrates with a top silicon thickness of 6 nm and a BOX thickness of 25 nm. These nFETs have a channel length of 22 nm and channel width of 1.2 microns. The nFETS were irradiated using the 10 keV X-ray source in ON, OFF and PG bias. The results are shown in Fig. 11, Fig. 12 and Fig. 13 with a summary shown in Fig. 14.

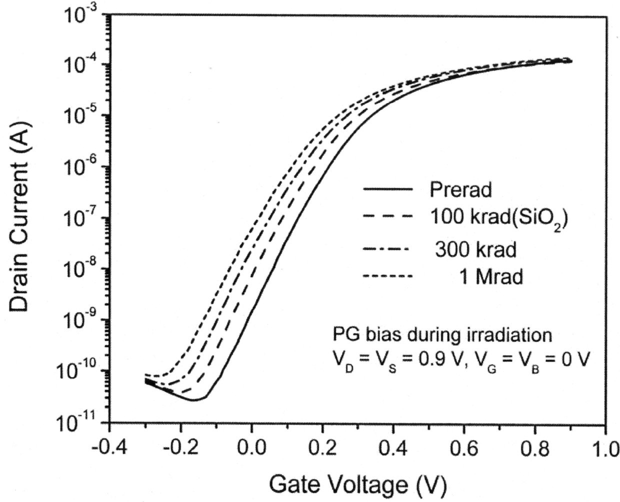

Fig. 13. Current-voltage characteristics versus 10 keV X-ray dose (517 rad(SiO_2)/s) for 14 nm SOI UTBB nFETs (V_D = +50 mV). PG bias during irradiation.

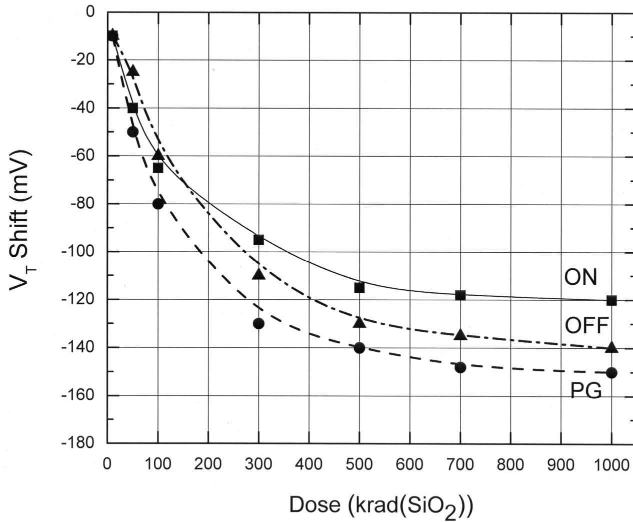

Fig. 14. Threshold voltage shifts for 14 nm SOI UTBB nFETs biased ON, OFF and PG during X-ray irradiation (V_D = +50 mV).

The largest threshold voltage shifts for UTBB are observed for PG bias during irradiation. In this case a fringing field extends from the source and drain through the buried oxide to the channel. During irradiation this field results in holes, created in the buried oxide, being driven to the channel/box interface and being trapped there. This trapped charge is coupled to the top gate resulting in threshold voltage shifts.

The effect of charge coupling from the BOX to the top gate transistor for fully-depleted technology is calculated using the following equation [5]:

$\Delta V_{top\ gate} = k\ \Delta V_{back\ gate}$

Voltage shift of top gate = k times voltage shift of back gate

Where the coupling factor k

$k = [(C_{BOX}\ C_{S)i}/(C_{BOX} + C_{Si)}\ ]/C_{top}$

C_{BOX} = buried oxide capacitance = $\varepsilon_o\varepsilon_{BOX}/t_{BOX}$

C_{Si} = silicon channel capacitance = $\varepsilon_o\varepsilon_{Si} / t_{Si}$

C_{top} = top gate dielectric capacitance = $\varepsilon_o\varepsilon_{top\ gate} / t_{top\ gate}$

$\varepsilon_o = 8.86 \times 10^{-14}$ F/cm

thickness of BOX (t_{BOX}) = 145 nm or 25 nm

equivalent oxide thickness of top gate dielectric ($t_{top\ gate}$) = 2.8 nm

thickness of silicon channel (t_{Si}) = 60 nm

dielectric constant of SiO_2 BOX (ε_{BOX}) = 3.9

dielectric constant of top gate equivalent oxide ($\varepsilon_{top\ gate}$) = 3.9

dielectric constant of silicon channel (ε_{Si}) = 11.7

The above equation was used to produce a plot of front gate threshold voltage shifts vs. back gate voltage shifts for two different BOX thicknesses. Fig. 15 shows the results from this calculation for BOX thickness values of 25 nm and 145 nm and measured results from nFETs with these thickness values.

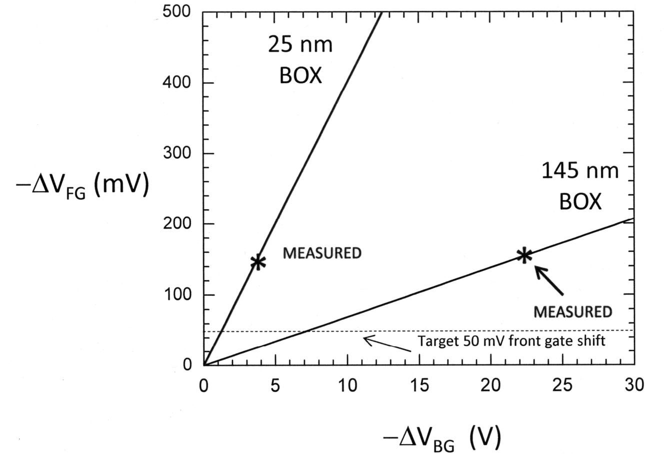

Fig. 15. Fully-depleted calculated charge coupling of front gate (FG) threshold voltage shifts to back gate (BG) threshold voltage shifts for two BOX thicknesses.

For nFETs built on 145 nm BOX, the top gate shift was -140 mV and the back gate shift was -22 V, in good agreement with the calculated values shown in Fig. 15. For nFETs built on 25 nm BOX the front gate shift was -150 mV (Fig. 14) and the back gate shift was -3 V, again in good agreement with the calculated values. This is strong evidence that the top gate threshold voltage shifts result from coupled radiation-induced positive trapped charge in the BOX.

VI. Summary

TID vulnerability is found to increase when CMOS technology nodes scale below 32 nm. Depending on design, radiation induced threshold voltage shifts from -25 mV to -50 mV can be tolerated, and off-state current increases from 5 X to10 X of prerad values can be tolerated [6]. Using these

values, the results of the present work can be used in a very preliminary sense to define the radiation tolerance of the14 nm technologies. For designs that can function with threshold voltage shifts of -50 mV, the radiation tolerance of bulk silicon FinFETs is 200 krad(SiO_2), while the SOI FinFETs have a radiation tolerance of 300 krad(SiO_2). The UTBB devices have a radiation tolerance of 50 krad(SiO_2).

VII. References

[1] N. Rezzak, E. X. Zhang, M. L. Alles, R. D. Schrimpf, and H. L. Hughes, "Total-Ionizing-Dose Radiation Response of Partially-Depleted SOI Devices," *Proc. IEEE Int. SOI Conf.*, Oct. 2010.

[2] S. T. Liu, A. Hurst, H. L. Hughes, P. McMarr, J. Benedetto, and C. Capasso, "Total dose radiation response of a 45nm SOI Technology," *Proc. IEEE Int. SOI Conf.*, Oct. 2010.

[3] L. Palkuti, M. Alles and H. Hughes, "The Role of Radiation Effects in SOI Technology Development," Proc. IEEE SOI-3D Conf., Oct. 2014.

[4] M. L. Alles, H. L. Hughes, D. R. Ball, P. J. McMarr, R. D. Schrimpf, "Total-Ionizing-Dose Response of Narrow, Long Channel 45 nm PDSOI Transistors," IEEE Trans. Nucl. Sci., 61(6), 2945 (2014).

[5] W. C. Jenkins and S. T. Liu, "Radiation Response of Fully Depleted MOS Transistors Fabricated in SIMOX," IEEE Trans. Nucl. Sci., 41(6), 2317 (1994).

[6] B. Doris, IBM Research, private communication.