A Fast Low Noise CMOS Charge Sensitive Preamplifier For Column Parallel CCD Readout.

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Abstract—A fast, low noise charge sensitive preamplifier for column parallel CCD readout application is presented. This prototype has been implemented on a commercial CMOS 65nm process. This preamplifier consists of a two stage transconductance amplifier with capacitive feedback to accommodate two gain ranges and a second transconductance amplifier to reset the circuit. An equivalent noise charge of 37 electrons for a 100ns readout cycle time is achieved for a power consumption of 5mW. Novel design techniques used in this circuit will be presented in detail along with measurement results obtained on the prototype.

I. INTRODUCTION

THERE is increasing scientific interest in the use of X-ray light sources for imaging of dynamic processes. This will require advanced detectors and low-noise cameras operating at unprecedented frame rates with pixel rates exceeding 100 Gpixel/s [1].

A fast, low noise charge sensitive preamplifier for column parallel CCD readout application is presented. This prototype has been implemented in a commercial CMOS 65nm process. This circuit is used as the front end amplifier of a 16 channel mixed mode digitizer. This preamplifier consists of a two stage trans-conductance amplifier with capacitive feedback to accommodate two gain ranges and a second trans-conductance amplifier to reset the circuit. An equivalent noise charge of 37 electrons for a 100ns readout cycle time is achieved. Novel design techniques have been used in this circuit to reach this performance. This paper is organized as follows: Section II presents the preamplifier requirements. Section III describes the circuit architecture and details the schematic. Chip layout is discussed in Section IV. Experimental results are presented in section V.

II. PREAMPLIFIER REQUIREMENTS.

Fig. 1 shows the output stage of a column parallel CCD recently designed in our laboratory. One notable aspect of this CCD is its lack of an output source-follower. The $\Phi_{1,2,3}$ terminals transfer the charges along the serial register while the terminal Φ_{out} , called transfer gate, brings the signal to a floating diffusion. As these terminals are clocked, a large amount of charge injection is created by the Φ_{out} clock transitions. The preamplifier reads out the charge deposited on the floating diffusion. This charge is the sum of the video

signal and the transfer gate charge injection. These CCDs will be clocked at a column rate of up to 10 MHz.

Fig. 1. Conceptual diagram of a column parallel CCD output structure.

Instead of a buffer amplifier, the output of the CCD is a floating diffusion, which means that the preamplifier reads out the signal charge packet destructively. In order to do this successfully at the requisite 10 MHz rate, the input stage must be charge-sensitive, fast, low-noise, and capable of accepting from and returning to the CCD large amounts of charge during its transfer phase (the transfer gate charge injection), while still sensing small signal charge packets. To meet anticipated interfacing and imaging performance requirements, the preamp must satisfy the specifications in Table 1.

TABLE I. PREAMPLIFIER REQUIREMENTS

Full scale input charge	$50 \cdot 10^3$ e- and 10^6 e-
Transfer gate charge injection	> 200000 e-
Input capacitance	500 fF or less
Settling time	< 15 ns
Reset time	< 15 ns
Charge loss due to finite DC gain	1%
Linearity	> 10 -bit
Readout cycle time	100ns, 150ns, 200ns
Preamplifier pitch	50 μ m

III. CIRCUIT ARCHITECTURE.

The preamplifier block diagram is shown in Fig. 2. The circuit consists of a low noise, high DC gain core amplifier labeled A1. A set of switches, S_{1a} and S_{1b} , change the gain setting from 50ke- to 1Me- ranges.

A second switched trans-conductance amplifier labeled A2 resets the feedback capacitor Cf50k and Cf1M and is activated by the switch S2. Two external reference voltages V_{ref1}

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A. Core Amplifier.

$$v_{out} = \frac{1}{PSRR_{vdd}} \frac{C_p}{C_f} v_{dd} + \frac{1}{PSRR_{vss}} \frac{C_p}{C_f} v_{ss} \quad (1)$$
[illegible]

The output of the differential pair is folded to increase swing and then drives common-source amplifier MN6 and MP5. The output is then buffered by the source follower consisting of MN7 and MN8. The feedback capacitors $C_{\text{comp}1,2}$ are used to implement cascoded compensation by feeding back a portion of the output signal to the folding node. This technique greatly improves high frequency negative power supply noise reduction [2]. To preserve the loop stability and keep the preamplifier rise time independent of gain setting, a switched Miller capacitor network has been added.

The conversion gain of the circuit, in the limit of large open-loop gain, is approximately $1/C_f$. In reality the output voltage is given by

$$v_{out} = \frac{Q_{in}}{C_f + \frac{C_p}{A_0}} \quad (2)$$

B. Reset transconductance amplifier.

As the reset time allowed for the preamp in the highest channel rate case (10MHz) case has to be less than 15ns, an active reset circuit is required. The OTA uses half of a symmetrical architecture [3] and the current mirror outputs are energized by the Reset and Resetb switches only when the preamplifier is being reset. Because a low transconductance is required here for stability and noise purposes, the differential pair MP1 and MP2 is biased with a large I/G_m ratio, where G_m is the differential pair transconductance and is the tail current of the differential input pair. Two banks of current sources with different aspect ratios have been implemented depending on the preamplifier gain settings. They are controlled by the G1M and G1Mb switches.

C. Correlated double sampler and gated integrator.

To remove the reset noise from the reset amplifier A2 in Fig.2, a correlated double sampler (CDS) with a gated integrator has been implemented on chip. This is a powerful, widely used technique to suppress reset noise in solid-state imagers [3]. It also reduces the thermal and 1/f noise of the preamplifier. The basic concept is to take two samples of the preamplifier output: the first after the preamplifier is reset and the second when the signal charge packet is available at the CCD output. Since the charge injection from the reset operation is common to both samples, taking their difference can reject the charge injection while retaining the signal. The dual-slope CDS technique is conceptually simple to implement. The input after preamplifier reset is integrated in one direction. Then, the output charge packet (which includes both charge injection and signal) is read out. The output voltage of the integrator is then proportional to the signal charge, and the reset noise is canceled. A block diagram of this circuit is shown in Fig.5.

Fig. 5. Correlated double sampler (CDS) and gated integrator block diagram. The CDS is implemented using fully differential circuits to improve both the signal-to-noise ratio at the integrator output and to be compatible with the digitizer which samples its output. The single-ended output of the preamplifier is converted to differential by sending the preamp output through two paths. One path goes directly to the integrator's inverting input and the other goes through a unity-gain inverting amplifier before it reaches the integrator's non inverting input. Because the inverting amplifier has finite bandwidth, the phase difference between the two signals is not exactly 180 degrees, but since the channel rate is limited to 10 MHz, the phase mismatch does not significantly affect the CDS performance. Three different integration periods are available: 25ns, 50ns and 75ns. These different integration periods provide the same level of reset noise rejection but provide thermal noise rejection proportional to the time spent integrating.

The noise power P after transmission through this filter is given by

$$P = \int_0^\infty |H(\omega)|^2 \left(W_0 + \frac{F_0}{\omega} \right) d\omega / 2\pi$$

$$\text{with } |H(\omega)|^2 = \frac{4 \sin^2 \omega\tau}{\omega\tau^2} \sin^2 \omega\tau (1 + \Delta) \quad (3)$$

where W_0 , F_0 indicate the relative magnitude of the white, 1/f preamplifier noise. τ is the reset and signal integration period and Δ the time interval in between them. With a thermal noise of 2nV/rt Hz and a 1/f noise of 3μV at 1Hz referred to the input of the core amplifier differential pair, a simulated total

noise referred to the preamplifier input for different integration periods is shown in Table II.

TABLE II. NOISE SIMULATION RESULTS.

Integration time:	Readout cycle	Noise (ENC)
2 X 25ns	100ns	37e-
2 X 50ns	150ns	26e-
2X 75ns	200ns	23.5e-

D. Simulation results.

Fig.6 shows a transient simulation of the preamplifier.

Fig. 6. Preamplifier transient simulation: 50ke- input signal, 200ke- transfer gate charge injection, 100ns cycle time.

The first plateau, shown on the lower trace, is the sum of the transfer gate charge injection and the video signal while the second plateau is the remaining signal to be read out. The upper trace is the output voltage of the preamplifier showing the image of the input charge along with its reset phase. The linearity performance of the preamp in 50ke- mode and with a 100 ns cycle time is shown Fig.7. The peak nonlinearity (at full-scale) is less than -0.15 bit at a 10-bit level, indicating that the preamp is capable of approximately 12-bit linearity performance in this mode. The linearity is degraded somewhat in the lower sensitivity mode and is about 10-bit.

Fig. 7. Preamplifier nonlinearity simulation: 200ke- transfer gate charge injection, 50ke- full scale, 100ns cycle time.

The simulated transfer function of the power supplies to the output is shown in Fig.8. Without the specialized design techniques discussed above to desensitize the circuit from noise in both ground and positive rail, there would have been significant power-supply gain, rather than the attenuation achieved here.

Fig. 8. Preamplifier power supply sensitivity.

IV. PREAMPLIFIER LAYOUT.

The circuit has been implemented in a CMOS 65nm mixed mode process. The active area is about 170um x 200um for each preamplifier. The two trans-conductance amplifiers are located on the upper part of the layout, while the switched capacitor banks are drawn on the bottom. Fig.9 shows the preamplifier layout. Four preamplifiers have been placed in a row with their input pads located on the left hand side to match the 50μm pitch of the CCD. Care have been taken to lower the trace resistance by using the top metal layers which have a low resistivity per square.

Fig.9. Preamplifier layout.

V. EXPERIMENTAL RESULTS

A photograph of the custom test board is shown in Fig 10. The circuit is functional. Fig. 11 shows an oscilloscope screenshot of the gated integrator output shown in Fig. 5 for a readout cycle time of 200ns. The upper trace corresponds to the charge injected to the preamplifier including the transfer gate charge injection. The lower trace is the gated integrator output for a full scale input charge in the 50ke- mode. Noise and linearity measurements haven't been performed by the time of this conference record.

Fig. 10. Test board photograph.

Fig. 11. Test board photograph.

They will be reported in one of the Transactions on Nuclear Science (TNS) issues.

VI. CONCLUSION

A fast, low noise charge sensitive preamplifier for column parallel CCD readout application is presented. An equivalent noise charge of 37 electrons for a 100ns readout cycle time is achieved. Novel design techniques have been used in this circuit to reach these performances. This prototype has been implemented in a commercial CMOS 65nm process. The total power consumption is 5mW with a power supply voltage of 1.8V as we are using quarter microns devices.

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