A 1.3- μ W 12-bit Incremental $\Delta\Sigma$ ADC for Energy Harvesting Sensor Applications

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Abstract—This paper presents an ultra-low power, incremental $\Delta\Sigma$ ADC for sensor applications. The ADC is integrated in an energy harvesting chip, and its power consumption has to be less than 2 μ W at temperatures ranging from -40°C to 85°C . The complete system including the ADC, interfacing sensors, and power management circuit is fabricated in 0.18 μm CMOS technology. The ADC works with a single on-chip reference voltage. The fabricated ADC occupies 0.21 mm^2 , and consumes 1.3 μW from the 1.2-V supply voltage at room temperature. Power consumption increases almost linearly with temperature and reaches 1.7 μW at 85°C . The sleep current is less than 10 nA. In free-running mode at 40 kS/s, the ADC achieves 68 dB peak SNDR with $\text{OSR}=200$. This corresponds to $\text{FoM}_w=1.58$ pJ/conv., which is comparable to the state-of-the-art incremental ADCs, while power consumption is at least 5X lower. Measurements with the on-chip temperature sensor verified the ADC's performance.

I. INTRODUCTION

The rapid growth of wireless electronic applications such as wireless sensor networks and portable electronic devices has made power consumption one of the most important parameters in electronic circuits performance. The large size and weight of batteries which limit the scaling of portable devices, as well as the difficulties associated with battery replacement in remote areas or in human body, highlight the need for alternative power supplies. In recent years, energy harvesting has received increasing attention for sensor applications. However, given the limited available harvested energy, ultra-low power data acquisition circuits must be developed to enable the use of energy harvesting in such applications.

Among existing data converter topologies, incremental delta-sigma ($\Delta\Sigma$) analog-to-digital converters (ADC) are one of the common choices in low power sensor applications with moderate or high accuracy. An incremental $\Delta\Sigma$ ADC is a $\Delta\Sigma$ ADC which is reset periodically. A decimation filter, which can be realized as a cascade of counters, provides the conversion result between two resets. This intermittent operation improves the sample-to-sample accuracy, and also enables a single ADC to be switched between multiple channels, thereby eliminating the need for additional ADCs in multi-channel applications [1]. Moreover, in incremental ADCs the oversampling ratio is defined as the ratio of the clock frequency, f_{CLK} , to reset frequency, f_{RST} , hence higher accuracy can be obtained at the expense of longer conversion time. This is particularly beneficial in sensor applications in versatile environments.

The $\Delta\Sigma$ ADC presented in this paper is designed to interface an integrated temperature sensor and a pressure sensor on an energy harvesting chip. The ADC operates with harvested energy provided by a photovoltaic cell. The maximum available power is 20 μW , from which 2 μW (10%) is allocated for the ADC in the worst case. The sleep current of the ADC is minimized for low-light situations. The energy harvesting techniques and power management circuits used in the chip are discussed in [2]. System-level design and detailed ADC implementation are described in section II. Measurement results with and without the on-chip temperature sensor are discussed in section III. Section IV concludes the paper.

II. PROPOSED ARCHITECTURE

A. System Overview

Fig. 1 shows the designed ADC with its peripheral circuits. The bias current of the ADC is supplied by the on-chip current source, and an all-CMOS voltage reference sets the feedback DAC output level in the $\Delta\Sigma$ modulator. The analog multiplexer connects the ADC either to the on-chip sensors or to external input signals. The temperature and the pressure sensor have differential outputs, but single-ended operation is also made possible by adding a reference voltage input (V_{ref}) to the multiplexer. The 1-bit output of the $\Delta\Sigma$ modulator is integrated by a counter which can be operated in 1st or 2nd order mode. A programmable 16-bit control word defines the length of the bit-stream to be integrated. Programmable bit-stream length and integration rate are used to allow for trading the accuracy with speed. The digital signal processing unit is used to correct the offset and gain error of the ADC, enabling the system to work accurately with different input sources and characteristics.

Fig. 1: Overall block diagram of the ADC and its peripherals.

B. ADC Architecture

Fig. 2 shows the conceptual block diagram of the designed ADC. In this design, a 2nd-order cascade of integrator architecture with a 1-bit quantizer is used. Given the long conversion time and idle-tone behavior of 1st-order modulators, and instability issues associated with higher order modulators, choice of a 2nd-order modulator is justified for the target application. The modulator has a distributed feedback structure with no feed-forward branches, which eliminates the need for an additional adder before the quantizer. Analytical calculations and macro-model simulations in MATLAB show that by proper choice of loop filter coefficients, this architecture can achieve an SQNR of 77 dB with OSR=200.

The switched-capacitor implementation of the modulator is shown in Fig. 3. The integrators have a fully differential architecture which requires differential feedback signals. Conventionally, these signals are generated by using two dedicated reference voltages (V_{ref}^+ and V_{ref}^-) in the feedback DAC, which results in large footprint, circuit complexity, and significant power overhead. In the presented design, the need for a second reference voltage is eliminated by using VSS and a single global reference voltage as feedback DAC output levels. Power consumption is further reduced by using single-ended comparator and digital logic.

The minimum capacitor size is chosen based on noise requirements and is equal to 72 fF. Total input capacitance is 144 fF. To reduce the offset and flicker noise of the system, chopper stabilization is used in the first integrator. In addition, bottom plate sampling is utilized to eliminate the harmonic distortion caused by switch charge injection. The non-overlapping clock signals required for switched-capacitor integrators ($CLK_{1,2}$), chopper stabilization ($CLK_{ch1,2}$), and bottom-plate sampling ($CLK_{a1,2}$) are generated by the non-overlapping clock generator shown in Fig. 4. In order to save power, the long delays (represented as gray inverters in Fig. 4) are implemented as cascaded inverters using longer transistors than the minimum length. As opposed to only increasing the load capacitance, this method additionally reduces the shoot-through current arising from the long rise/fall times.

C. Opamps

Due to stringent power constraints of the application, each opamp must draw less than 500 nA from the supply voltage. Based on macro-model simulations, for 70 dB SNDR at $f_{CLK} = 40$ kHz, the opamps must have a gain higher than 65 dB and a minimum GBW of 360 kHz. To meet these requirements, a fully differential folded-cascode structure with sub-threshold input pair was used (Fig. 5). Sub-threshold operation enables higher $\frac{g_m}{I}$ ratio. The required bias currents and voltages are generated using current mirrors and composite transistors. The opamps use a switched-capacitor common-mode feedback (CMFB) circuit. In post-layout simulations, the worst-case gain and GBW were 70 dB and 440 kHz, respectively, while the total current did not exceed 470 nA. The worst-case input-referred thermal noise is $0.2 \frac{\mu V}{\sqrt{Hz}}$, with a flicker noise cut-off frequency of 50 kHz.

Fig. 2: Conceptual block diagram of the ADC.

Fig. 3: Switched-capacitor implementation of the ADC.

Fig. 4: The non-overlapping clock generator.

Fig. 5: The folded-cascode opamp used in the integrators.

D. Quantizer

Thanks to noise shaping properties of $\Delta\Sigma$ modulator loop, quantizer design is not critical in 1-bit $\Delta\Sigma$ converters, and power consumption is determined based on speed requirements. In this design, the quantizer is implemented with a two-stage opamp followed by a D flip-flop. The opamp shows a worst-case gain of 60 dB in post-layout simulations, while drawing less than 100 nA from the 1.2-V supply voltage.

III. MEASUREMENT RESULTS

Fig. 6 shows the die micrograph of the complete system fabricated in 0.18 μm CMOS technology. The ADC including the non-overlapping clock generator occupies 0.21 mm^2 from the total die area of 7.92 mm^2 . In order to correctly characterize the ADC, measurements were done in a temperature chamber with off-chip reference and supply voltage. Three sets of simulations were performed: First, the ADC was tested in free-running mode and the SNR/SNDR curve was derived. Second, the ADC's transfer curve was obtained using off-chip dc inputs. These measurements were repeated at various temperatures within the $[-40^\circ\text{C } 85^\circ\text{C}]$ range. Finally, the on-chip temperature sensor was used to verify the ADC's performance in the target application.

A. The Stand-alone ADC

Fig. 7 shows the SNR and SNDR of the ADC in free-running mode as a function of input amplitude. At room temperature, a peak SNR of 70 dB and peak SNDR of 68 dB is obtained with $f_{\text{CLK}}=40$ kHz and $\text{OSR}=200$. The measured output spectrum of the ADC is depicted in Fig. 8. It can be clearly seen that despite the differential architecture of the ADC, total harmonic distortion is dominated by the second-order harmonic. In fact, single-ended measurements showed 3 dB difference in the SNDR obtained from the positive and negative inputs. This is suspected to be caused by layout asymmetries, although common-centroid geometry was applied to the switched capacitors and opamp transistors.

Fig. 9 shows the measured absolute error of the ADC as a function of input amplitude at room temperature. In these measurements, the ADC is operated in incremental mode with $\text{OSR}=200$, i.e. the $\Delta\Sigma$ modulator and the counters are reset after each 200 cycles. The ADC has acceptable accuracy within input range of ± 750 mV. Maximum absolute error at room temperature is less than ± 1.5 LSB, and the worst-case absolute error across the temperature range is ± 1.7 LSB. In these measurements, the second-order non-linearity manifests itself as higher absolute error for positive differential voltages compared to negative differential inputs.

Power consumption of the ADC was also measured in the temperature chamber. At room temperature, the ADC draws 1.11 μA from the 1.2-V supply voltage. By sweeping the temperature from -40°C to 85°C , the current increases from 0.78 μA to 1.41 μA . This is partly due to the variations in the on-chip current source which has a temperature coefficient of approximately $3.7 \frac{\text{nA}}{^\circ\text{C}}$, resulting in 0.46 μA change in the bias

Fig. 6: Die micrograph of the complete system. The unmarked area is used for energy harvesting and voltage regulation.

Fig. 7: SNR and SNDR vs. input signal amplitude. Full-scale is 0.9V.

Fig. 8: Measured 65536-point output spectrum in free-running mode with $V_{\text{in,diff}}=0.6$ V and $f_{\text{CLK}}=40$ kHz.

current over the temperature range. The remainder can be due to threshold voltage variations. The worst-case sleep current was less than 10 nA. The measurements in free-running and incremental modes indicate negligible power consumption in the counters. It is worth noting that in this application the supply voltage must be high enough to enable high SNR and provide robustness against PVT, thus it could not be further reduced to decrease the power.

Table I summarizes the performance of the ADC along with the results from recently published incremental $\Delta\Sigma$ ADCs.

Fig. 9: Measured ADC's absolute error at room temperature.

TABLE I: Measured Performance Summary and Comparison

	This Work	[3]	[4]	[5]	[6]	[7]
Technology (μm)	0.18	0.16	0.15	0.13	0.09	0.15
Supply Voltage (V)	1.2	1	1.6	0.25	1.2	1.6
Power (μW)	1.3	20	96	7.5	6.75	83
BW (kHz)	0.2	NA	2	10	1	1.67
Peak SNDR (dB)	68	81	64	61	74	85
FOM _w [*] (pJ/conv)	1.58	1.48	14.7	0.41	0.99	1.71

$$*FOM_w^* = \frac{Power}{2 * BW * 2^{\frac{SNDR-1.76}{6.02}}}$$

B. Measurements with the Temperature Sensor

The transfer curve measurements were also performed with the on-chip temperature sensor with differential output. In these measurements, the ADC is operated in free-running mode, and the 1-bit output of the ADC is read using a logic analyzer and averaged. The ADC transfer curve and the corresponding absolute error are shown in Fig. 10. The figure shows an increase in the error with temperature, which is not in line with the results obtained from the stand-alone ADC. The observed non-linearity is mainly due to the change in the ADC's gain and offset with temperature. Since the ADC's absolute error is calculated based on the best fitted line after gain and offset correction, temperature variance does not affect the dc measurement results. Besides, as shown in the bottom plot in Fig. 10, the output of the temperature sensor lies within [320 780] mV, and it goes beyond ADC's acceptable input range at 85°C. The error caused by gain and offset variations can be reduced using the on-chip DSP unit.

IV. CONCLUSION

A 1.3- μW 12-bit incremental $\Delta\Sigma$ ADC was implemented using a single global reference voltage. Ultra-low power consumption is achieved through use of sub-threshold devices in the opamps, and exploiting the relaxed quantizer requirements in the 1-bit modulator. The ADC maintains its accuracy across the temperature range. At room temperature, the peak SNDR is 68 dB and FoM_w=1.58 pJ/conv. is obtained. This is comparable to recently published incremental $\Delta\Sigma$ ADCs, while power consumption is at least 5X lower. The ADC is also characterized with an on-chip temperature sensor.

Fig. 10: Measurement results with the on-chip temperature sensor.

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