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Vanadium Dioxide (VO_2) is also a Ferroelectric: Properties from Memory Structures

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***Abstract*—This work claims that VO_2, of interest currently for its metal-insulator phase transition properties, is also a ferroelectric material. Using a VO_2 film sandwiched between two silicon dioxide layers, memory transistor structures with substantial and useful properties have been fabricated. Threshold voltage shifts are opposite of charge trapping phenomena and consistent with ferroelectric polarization switching phenomena. Hysteresis memory window of ~1 V is obtained in -4 to 4 V gate voltage cycling. We argue that the effects observed are due to the ferroelectricity of VO_2. Its remnant polarization of ~0.53 μC/cm^2 and coercive field of ~450 kV/cm are extracted from the saturation behavior of threshold voltage shift. Similar to other ferroelectric memory structures, depolarization effects are observed. The state of memory devices decays gradually and retention times of approximately 15 minutes are obtained at room temperature. These ferroelectric properties do not vanish above metal-insulator phase transition temperature.**

***Index Terms*—DRAM, Depolarization field, Ferroelectric, VO_2, Memory, Polarization**

I. Introduction

MEMORIES based on use of ferroelectricity have been of interest and use for considerable time [1], [2]. Some of this attraction is due to their possibilities as a universal memory with a small cell size in a single element, fast transition time, low power consumption, and nonvolatility [3]. In spite of many attempts, however, the ideal form of a ferroelectric memory at very small dimensions has not become a reality. A fundamental issue with the use of ferroelectric materials placed on a semiconductor, or anything non-metallic, is the existence of depolarization field [3], which slowly degrades stored information. Therefore, ferroelectric memories are expected to be more adequate for dynamic random access memory (DRAM) applications. Indeed, ferroelectric dynamic random access memory (FeDRAM) technology has been proposed as an alternative to the conventional DRAM [4], [5].

In the operation of a FeDRAM, memory window is determined by the remnant polarization (P_r), the thickness (t) and the dielectric constant (κ) of a ferroelectric film as the below [6].

$$\Delta V_{th} = \pm P_r t / \kappa \varepsilon_0 \quad (1)$$

where the ± sign denotes the direction of the polarization. Hence, to increase the memory window, one employs a ferroelectric material with high remnant polarization and low dielectric constant. Most inorganic ferroelectric materials have high remnant polarizations, but have high dielectric constants. So, ferroelectric polymers have recently been studied as alternatives to perovskite ferroelectric materials because of their low dielectric constants [6].

VO_2 is a representative correlated electron oxide material with phase transition close to room temperature. The transition takes place rapidly – about the order of picosecond [7]. Vanadium has numerous oxidation states (+2, +3, +4 and +5), and among these oxides, V_2O_5 is the most stable and common oxide compound. It is known that V_2O_5 is a ferroelectric material with Curie temperature (T_c) of 230 °C [8]. Meanwhile, VO_2 has been studied extensively for its metal-insulator transition and their possible use because of the change in properties arising from changes in conductivity, reflectivity, etc. Ferroelectricity of VO2 has not been studied seriously, although suspected [9], because the metal-insulator phase transition properties are so profound and

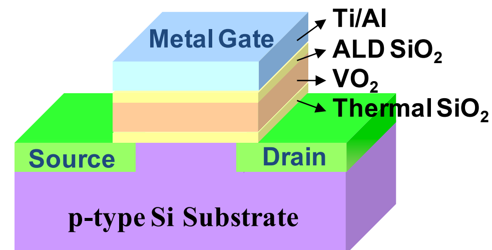

Fig. 1. Schematic view of a ferroelectric memory device with a VO_2 film as a gate insulator.

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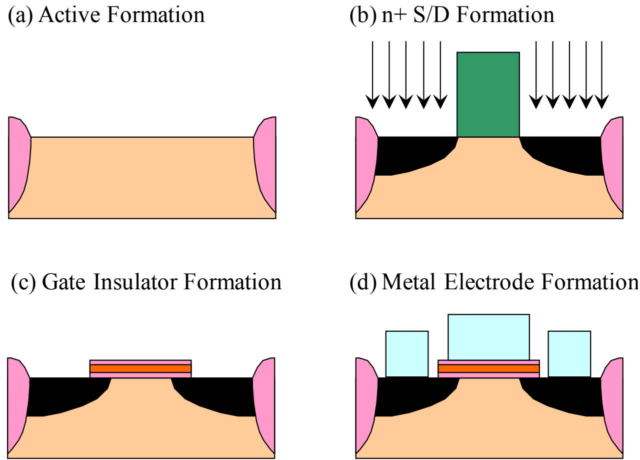


Fig. 2. Fabrication sequences for a VO_2 memory transistor: (a) Active regions formed by LOCOS process, (b) n+ S/D regions formed by As IIP, (c) Gate insulator patterns formed by CHF_3/O_2 etch and CF_4 etch, and (d) Gate and S/D metal electrodes formed by lift-off processes.

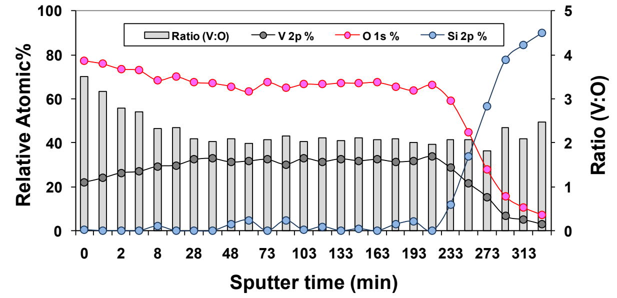


Fig. 3. Relative atomic composition ratio of V(2p) to O(1s). The ratio of V(2p) and O(1s) is 1:2.1 and 1:3.3 in the middle and surface of the film, respectively.

accessible and different from other materials. Like the ferroelectric polymers, VO_2 has a low dielectric constant of around 40 [10], and so is of special interest.

II. Experiments

Ferroelectric memory devices with VO_2 films as insulators were implemented using conventional CMOS processing technology. As shown in Fig. 1, the device structure is very similar to that of a Flash memory and composed of a transistor with a gate stack of metal-insulator-ferroelectric-insulator-semiconductor (MIFIS), where the VO_2 film is employed as an intermediate gate insulator. VO_2 is sandwiched between thermal SiO_2 and ALD SiO_2 on a p-type silicon substrate wafer.

Fabrication sequences for a VO_2 memory transistor are illustrated in Fig. 2. Active area is defined by i-line lithography and LOCOS process, and a 40 keV Boron implantation for channel doping was performed at a dose of $2x10^{12}$ cm^{-2}. After PR patterning, a 30 keV Arsenic implantation was performed at a dose of $3x10^{15}$ cm^{-2} to define source and drain (S/D) regions. After annealing the wafer, thermal SiO_2 (30 nm) was grown, followed by the deposition of sputtered VO_2 film (200 nm) and 110 ˚C plasma ALD process for SiO_2 dielectric layer (60 nm). For the S/D contact, CHF_3 with O_2 gas was used to etch the SiO_2 layers and CF_4 gas was used to etch the VO_2 film. 50 nm Ti and 300 nm Al were evaporated for the lift-off process of gate and S/D electrodes.

III. Results and Discussion

A. Composition Stoichiometry Analysis

To confirm the composition stoichiometry of the deposited VO_2, X-ray photoelectron spectroscopy (XPS) analysis was performed. The metal-insulator transition of VO_2 was also directly measured through conductivity measurement. Super-saturation multi-phase effects here are reflected in the thermal hysteresis observed. The atomic composition ratio of V(2p) to O(1s) is shown in Fig. 3. The ratio is around 1 to 2.1 in the middle of the film and 1 to 3.3 on the surface. This implies that the vanadium oxide film in our experiments is composed of the family of various vanadium oxides depending on the sputtering temperature and oxygen gas flow rate.

Although the atomic composition ratio acquired from the XPS analysis is not exactly 2, the film has a typical thermal hysteresis behavior of the resistance of VO_2 as shown in Fig. 4. The phase transition occurs at around 70 ˚C, which is the typical phase transition temperature of VO_2. In addition, the current induced phase transition effect commonly measured in stacked structures (here laterally) is also observed as shown in Fig. 5. This is the Mott transition property of VO_2 [11]. The phase transition of VO_2 happens at the high current injection state even at room temperature. From the above results, it is obvious that VO_2 oxide phase dominates the other oxidation states in the film used in our experiments.

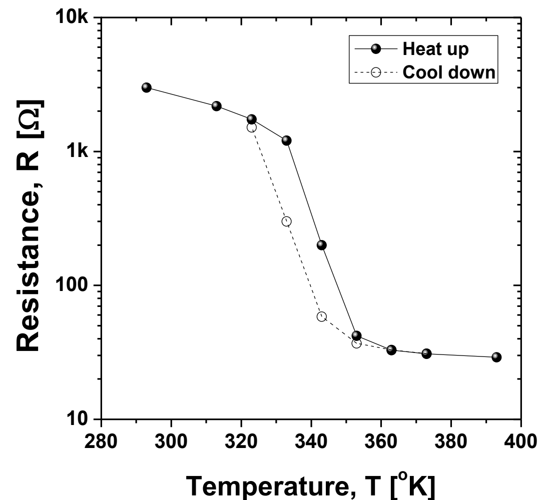


Fig. 4. Thermal hysteresis of the resistance of VO_2 film. The phase transition of VO_2 occurs at around 70 ˚C, which is the typical transition temperature of VO_2.

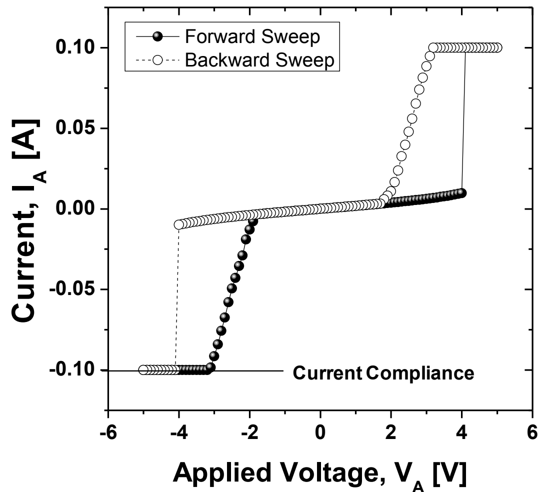
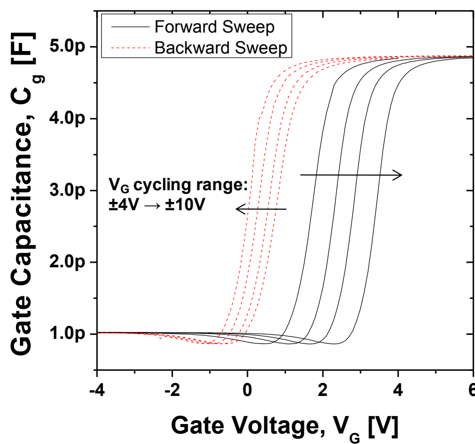


Fig. 5. Mott transition property of VO_2 film. Phase transition of VO_2 occurs at high current injection state even at room temperature.

B. Ferroelectric Properties

Fig. 6 (a) shows the hysteresis behavior of gate capacitance at room temperature in response to gate voltage in a fabricated device. As the gate voltage is cycled between ±4, ±6, ±8, and ±10 V, the capacitance cycled counterclockwise (starting from negative voltage) and the memory window increased linearly according to the cycling range of the gate bias. In -4 to 4 V gate voltage cycling, the memory window of ~1 V is obtained. This hysteresis behavior is consistent with ferroelectric polarization switching and opposite of the hysteresis resulting from charge trapping in the gate insulators. Fig. 6 (b) shows the threshold voltage shift after gate pulsing without source and drain biasing. After applying the negative gate voltage, the threshold voltage shifted positively and vice versa. These shifts occurred without channel current at room temperature, which means that this effect is independent of the phase transition of VO_2 film. These measurements, their existence at low temperatures, and their existence in the absence of heating, can be explained through postulating ferroelectric polarization mechanism in the VO_2 film.

The remnant polarization of a ferroelectric material is one of the most important properties that determine the memory window of a ferroelectric memory device as described in Eq. 1. So, to extract the remnant polarization of VO_2, the



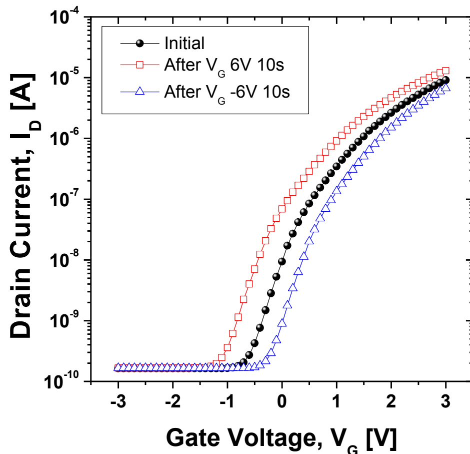
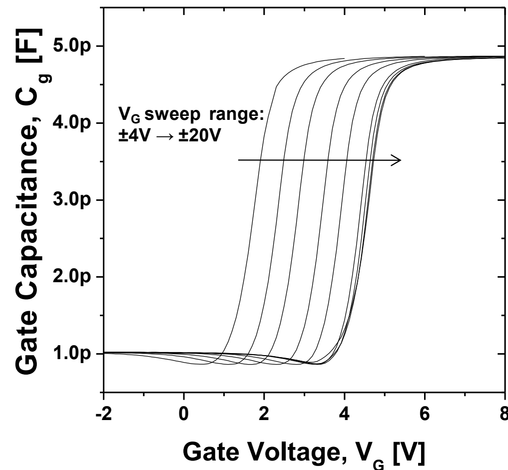


Fig. 6. Threshold voltage shift due to ferroelectric polarization switching: (a) Hysteresis behavior of gate capacitance in response to gate voltage and (b) Gate field dependency of threshold voltage shift.



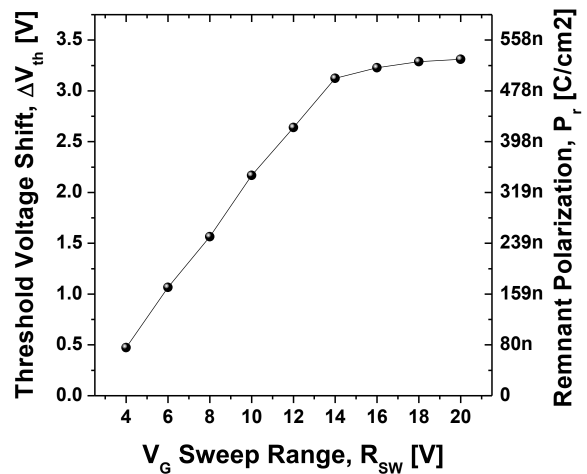


Fig. 7. Remnant polarization of VO_2: (a) C-V curves at various sweep ranges of gate voltage and (b) Trend of threshold voltage shift as a function of the sweep range.

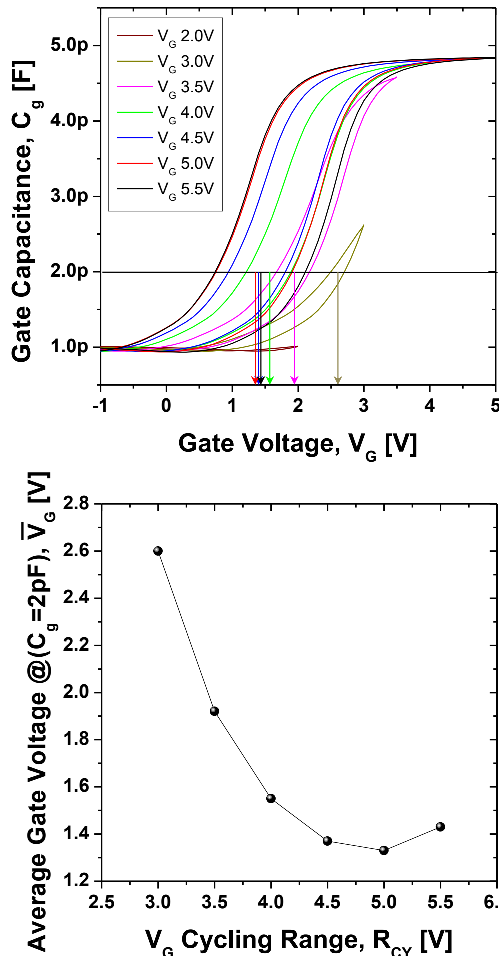


Fig. 8. Coercive field of VO_2: (a) C-V hysteresis at various cycling ranges of gate voltage and (b) Trend of average gate voltage when the gate capacitance is 2 pF as a function of the cycling range.

saturation phenomenon of threshold voltage shift was considered. Fig. 7 (a) shows C-V curves at the various sweep ranges of gate voltage and Fig. 7 (b) shows the trend of threshold voltage shift as a function of the sweep range. As shown in these figures, the threshold voltage shift saturated as the sweep range of the gate bias reached 20 V. This saturation implies that the polarization of VO_2 reached at its maximum value. That is, at that biasing condition, the saturation field is applied to the VO_2 layer and so, using Eq. 1, one can extract the remnant polarization of VO_2 from the threshold voltage shift at the sweeping gate voltage of 20 V. This is around 0.53 $\mu C/cm^2$. This value is comparable to the minimum polarization for the FeDRAM [4].

After application of the saturation field to VO_2, the hysteresis behaviors of gate capacitance in response to gate voltage was observed to extract the coercive field of VO_2, which is another important property of a ferroelectric material. Fig. 8 (a) shows C-V hysteresis behaviors at the various cycling ranges of gate voltage and Fig. 8 (b) shows the trend of average gate voltage when the gate capacitance is 2 pF as a function of the cycling range. As shown in these figures, the average gate voltage of forward and backward sweeps saturated as the cycling range of gate bias reached 5 V. This means that when the field input to VO_2 is below the coercive field, the threshold voltage is still higher due to the remnant polarization, and when the field is over the coercive field, the average threshold voltage stabilizes because the remnant polarization is removed whenever the gate voltage is cycled. Therefore, when the gate voltage is 5 V, the coercive field is applied to the VO_2 film. Using the structural factors of the gate stack and the gate voltage, one can calculate the coercive field of VO_2. This is around 450 kV/cm^2.

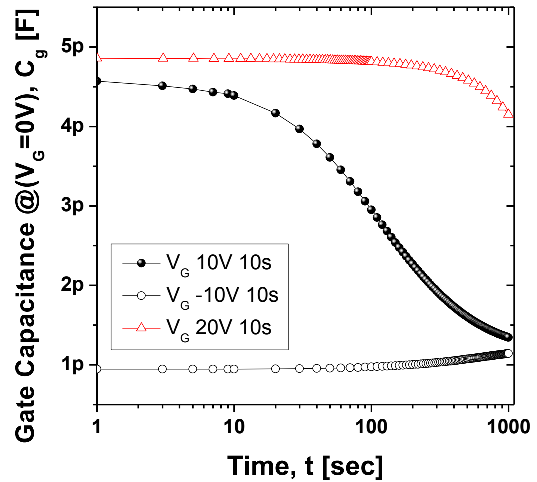


Fig. 9. Data retention time of a VO_2 memory device. In case of 20 V gate pulse, the retention time is around 15 minutes, which is three orders of magnitude longer than those of current generations of conventional DRAMs.

C. Data Retention Time

When a ferroelectric material is inserted between metal plates, there is no depolarization field due to the charge compensation by image charges in metal plates. On the other hand, in case of a ferroelectric field effect memory transistor, it is believed that depolarization field always exists due to the finite dielectric constant of a semiconductor [3]. Due to the depolarization field, information stored in a ferroelectric material will decay gradually.

Fig. 9 shows the data retention characteristics of an implemented device. To measure the retention time of VO_2 memory devices, the gate capacitance at zero gate bias is measured after applying a gate pulse to suppress data interference during the measurement. The retention time after a 10 V gate pulse is worse than after a 20 V gate pulse. This may be caused by the polarization instability of unsaturated ferroelectric film – the film is a polycrystalline structure with grains possibly in multiple orientations. In case of 20 V gate pulse, the retention time is around 15 minutes, which is three orders of magnitude longer than those of current generations of conventional DRAMs. This is a substantial improvement and therefore quite attractive at least for the high speed direction of volatile memories.

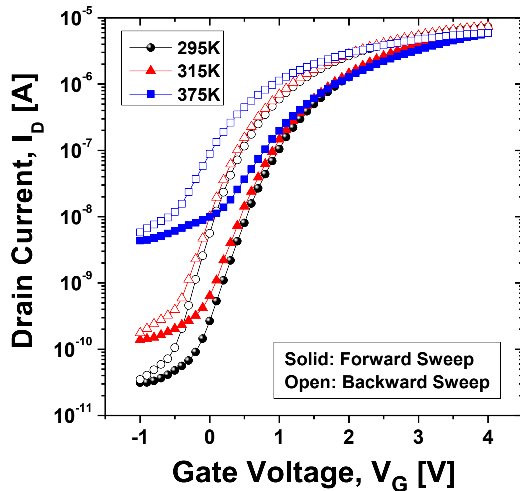


Fig. 10. Change of the hysteresis of drain current in response to the gate voltage according to temperature increase. Ferroelectric polarization does not disappear even at higher temperature than metal-insulator phase transition temperature.

D. Temperature Dependency

As shown in Fig. 10, the hysteresis of drain current in response to the gate voltage does not disappear even at the temperature higher than the metal-insulator phase transition temperature (~70˚C for these films). If the hysteresis is purely related to metal-insulator transition, the component should disappear above the transition temperature. The hysteresis, however, remains and the memory window increases all the more. This suggests the Curie temperature of this ferroelectric transition for VO_2 is different from the metal-insulator transition temperature – probably significantly higher. That is, the ferroelectric mechanism of VO_2 may be independent of the metal-insulator phase transition mechanism.

IV. CONCLUSION

This work has presented the results of the first implemented VO_2-based memory transistor that works like a dynamic memory with a hysteresis behavior in the threshold voltage in response to the gate field application. This effect is consistent with ferroelectric polarization. Owing to the low dielectric constant of VO_2, a large memory window was obtained. Using the saturation phenomena of the threshold voltage shift, the remnant polarization and the coercive field of VO_2 have been extracted. Due to the intrinsic depolarization field, the presented devices were volatile. Devices had retention times of approximately 15 minutes at room temperature, certainly attractive compared to the attributes now possible in conventional DRAMs. At higher temperature than the phase transition temperature, the ferroelectric effects were found to dominate the metal-insulator phase transition effects.

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