A CMOS Analog-to-digital Converter for a Digital RF Memory

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Abstract

This paper describes the design of a CMOS analog-to-digital converter (ADC) for use with the CMOS digital RF memory (DRFM) previously constructed at AFIT. The ADC is needed to digitize the incoming RF signal, which is bandlimited to 50 MHz, so that the DRFM can store and operate on the digital words instead of the analog signals. CMOS technology was used with the intent of eventually integrating the ADC into the same package as the DRFM.

Introduction

The purpose of the DRFM, when used as part of an EW system, is to provide a false target to an enemy radar. Kranz describes the design of a dual-port memory and a DSSM which implement the time delay and frequency shift functions, respectively [1]. However, Kranz did not address the A/D converter. A CMOS ADC was designed [2] that can be integrated into a monolithic CMOS DRFM, and that will approach the clock rate and resolution capabilities required by Kranz.

The conversion rate and resolution design goals for the DRFM ADC are determined by the maximum bandwidth (BW) and word size of the dual-port memory and DSSM. The word size and BW of the CMOS DRFM described by Kranz are 6 bits and 50 MHz, respectively.

ADC Architecture Comparison

Before the ADC was designed, various architectures were compared. The types of ADCs compared were staircase (also called counter or servo type), successive-approximation, dual-ramp (or dual-slope, the most common of the indirect type ADCs), flash (also called parallel type), two-step (or subranging), and pipelined ADCs.

The staircase ADC, successive-approximation

ADC, and dual-ramp ADC all have the advantage that they are small and could easily be fabricated on a monolithic DRFM [3]. However, they all have the disadvantage that they are slow [4,5].

On the other hand, the flash ADC is fast and simple. The disadvantages are that the chip area and power dissipation grow exponentially with the resolution of the ADC. These disadvantages can be partially overcome by use of a two-step architecture. The advantage of the two-step architecture is that it reduces the number of comparators needed for a given resolution when compared to the flash ADC. The disadvantages are that the time required for a conversion is more than twice that for a flash ADC, and the converter is more complex than a flash ADC. However, the conversion rate could be increased by pipelining. Therefore, the two-step architecture was chosen for this design.

It is unlikely that any of the six architectures considered, when implemented in CMOS, would be capable of completing a conversion in 10 ns. Therefore multiplexing (or interleaving) of two or more ADCs must be assumed.

Two-step ADC Architecture

The two-step ADC is based on the design in [6]. The basic block diagram is shown in Figure 1. The coarse flash ADC is composed of the coarse ADC encoder and the coarse ADC quantizer, which is composed of the seven comparators with outputs to the coarse ADC encoder. The fine flash ADC is composed of the fine ADC encoder and the fine ADC quantizer, which is the seven comparators connected to the fine ADC encoder. Both quantizers use the same reference voltage generator, which is a simple voltage divider. The DAC is composed of eight switches, S0 to S7, the switch control lines from the coarse ADC encoder, and taps from the reference voltage generator.

The reference voltage generator is a voltage

divider composed of 18 resistors and 17 voltage taps. A combined DAC/subtractor is used to provide the input to the fine flash ADC. The DAC is composed of 8 analog switches which are connected to the noninverting input of the subtractor and to 8 voltage taps from a voltage divider. The schematics for the coarse flash ADC encoder and the fine flash ADC encoder are contained in [2]. The comparator design is based on a two-stage, NMOS differential amplifier, as shown in Figure 2. The sample-and-hold circuit is based on a design presented in [6].

The multiplexed ADC system has three main blocks: two ranks of S&H circuits, a timing and control circuit, and an output block. The key to successful interleaving of several ADCs is ensuring that the input signal is sampled at known and regular points in time. An approach by Poulton to solve this problem is to use a two-rank S&H circuit [7], as shown in Figure 3. Now only the first rank S&H has the requirement to sample at regular intervals. The timing for the second rank S&H circuits may also be used to time the latching of the data from the ADCs. A modulo-5 ring counter was chosen to demonstrate the sample timing control between the first and second rank S&H.

CMOS DRFM ADC Design

After the architecture and high-level design had been determined, detailed design of the two-step ADC, the modulo-5 ring counter, and the data latch circuitry was required. Because the design of the analog circuits require that the substrates of the NMOS devices be biased at differing voltages, a p-well process is necessary. Details of the design are contained in [2].

Figure 4 is a schematic of the op-amp chosen for this design. The bias circuitry was sized by using the HSPICE optimization feature, with the results shown in Table 1. The subtractor uses the op-amp described above. The input and feedback resistors are chosen to be large to reduce the resistive loading on the op-amp. The resistor sizes are 10 k Ω . The sizing of the devices for the comparator, shown in Figure 2, were done using the HSPICE optimization feature. The results produced an average propagation delay of 4.7 ns. Device sizes are shown in Table 2.

The design of the digital circuitry does not involve the complicated calculations that were necessary for the sizing of devices in the analog circuitry. Digital device sizing criteria was based on minimizing device size, maximizing circuit speed, and ensuring proper signal level transmission.

The basic encoders are wired-OR encoders made up of four pseudo-NMOS inverters per bit-line. The sizing of the transistors is derived from methods described by Weste [8]. All devices are minimum size: $L = 2 \mu\text{m}$ and $W = 4 \mu\text{m}$. This flip-flop does not suffer from race problems or ones catching. All PMOS dimensions are $L = 2 \mu\text{m}$ and $W = 7 \mu\text{m}$. The NMOS device dimensions are $L = 2 \mu\text{m}$ and $W = 4 \mu\text{m}$. HSPICE simulation of the circuit produced propagation delays of approximately 1 ns.

Figure 5 shows a broad grounding scheme for the ADC. It is important to maintain as much separation as possible between the analog portions and the digital portions of the ADC. However, it is also important that V_{dd} and GND of both the analog and digital sections are equal. A capacitor between the V_{dd} and GND of the digital section may be necessary to minimize digital noise in the analog section.

The comparator, op-amp, D flip-flop, and wired-OR portion of the encoder were laid out in silicon. Based on the areas required by these circuits, the two-step ADC is estimated to require about 1,000,000 μm^2 .

Test Issues

ADC tests can be separated into tests that evaluate the static performance and tests that evaluate the dynamic performance. Static performance refers to how the ADC functions when a DC voltage is applied to the analog input. Dynamic performance refers to how well the ADC performs as a function of input signal frequency and amplitude, and as a function of ADC resolution and conversion rate.

Static performance can be measured in terms of offset errors, gain errors, and linearity errors. The offset error is the value of the input voltage that results in all zeros out [4]. Gain error is the difference in slope between the actual transfer function and the ideal transfer function [4]. Linearity errors can be divided into two types: integral linearity errors and differential linearity errors. The integral linearity error is the maximum deviation of a line through the center of the horizontal steps from the ideal input. Differential linearity error is the maximum difference between the adjacent horizontal steps.

The process of digitizing an analog signal introduces quantization errors, giving rise to a signal-to-noise ratio. Aperture errors are divided into three types: aperture delay, aperture uncertainty, and aperture

jitter [9]. The 3-dB BW is the frequency at which the output code representation of the peak amplitude is 3 dB down from the maximum for a full-scale input voltage.

Some of the more common dynamic tests for ADCs are the sine-wave histogram test, the sine-wave curve fitting test, the beat frequency test, and the locked histogram test.

The sine-wave histogram test, also called the code-density test, requires the storing of a large number of samples of a well-defined input signal [9]. The test uses a probability distribution to forecast the linearity of the ADC.

The curve fitting test, or algorithm, is used to measure the ADC SNR and effective bits. Like the sine-wave histogram test, this test involves the acquisition of large amounts of data. The algorithm involves using statistical calculations to fit a reconstructed function to the input data [9].

The beat frequency test is used to measure the full-power BW and slewing rate performance of the ADC [9]. A sine wave at a frequency slightly above the Nyquist frequency is applied to the ADC. Aliasing occurs and the resulting ADC output can be used to evaluate errors like noise effects, aperture uncertainty, and slewing limitations.

Summary

The design of a 6-bit two-step CMOS ADC with a two-stage BW-enhanced S&H circuit was described. A comparison of ADC types was done and the two-step architecture was chosen because an assumption was made that after successful completion of a working two-step ADC design, the design changes necessary to transform it into a pipelined ADC should be minimal. The theory of operation of the major circuits of the ADC and major multiplexing blocks was described. HSPICE simulations of the key ADC components was accomplished. Circuit layouts were done on the comparator, the op-amp, the D flip-flop, and the wired-OR portion of the encoder.

Acknowledgements

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Table 1. Op-amp device size.						
Device	M1 & M2	M3 & M4	M5	M6	M7	M8
Length (μm)	2	2	2	6	6	3
Width (μm)	110	5	16	6	25	83
Device	M9	M10	M11	M12	M13	M14
Length (μm)	2	4	5	3	6	4
Width (μm)	65	7	5	23	7	7

Table 2. Comparator device size.							
Device	M1 & M2	M3 & M4	M5	M6	M7	M8	R_{BIAS}
Length (μm)	2	2	2	2	2	3	97K Ω
Width (μm)	58	33	20	7	4	7

Figure 1. Basic block diagram of the two-step ADC.

Figure 2. Analog comparator.

Figure 3. Two rank S&H for interleaved ADC system.

Figure 4. Internally compensated CMOS operational amplifier.

Figure 5. Basic grounding and power supply connections.