TRANSLATION OF DIGITAL DESIGNS IN CMOS TO GALLIUM ARSENIDE

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Abstract

VLSI designs at the Air Force Institute of Technology have generally been fabricated in the CMOS technology. Although the CMOS technology supports high speed circuits, significantly faster circuits can be designed in the gallium arsenide (GaAs) technology. This paper describes the methodology in translating a CMOS digital design to a GaAs digital design. Risks in the process are highlighted. Logic elements translated include simple gates (AND, OR, NOR), and a full adder. Test chips have been successfully designed using this approach. A process test chip has been tested with results comparable to the HSPICE model parameters obtained from Vitesse Semiconductor. The test chips were packaged in 52-pin LDCC/LCC packages.

Gallium Arsenide Technology

The technology offers both the enhancement and depletion MESFET in n-type GaAs plus Schottky diodes, and n+ resistors. GaAs MESFETs offer several advantages over silicon for use in high-speed digital integrated circuits.

The key advantage is that GaAs circuits are generally 5 to 10 times faster than silicon circuits because electrons travel faster in GaAs than in silicon [1]. The electron mobility at low electric fields is 4,000 to 5,000 cm²/V-sec at 300°K as opposed to silicon which is 500 to 1200 cm²/V-sec at 300°K. This provides significant speed achievements in an enhancement/depletion (E/D) n-type process. Also, GaAs transistor channel lengths are "keeping pace" with silicon technologies. Channel lengths of 0.25 μm to 1.0 μm are common. The Vitesse Semiconductor GaAs E/D process has an effective channel length of 0.8 μm and an applied voltage range from 1 volt up to 3.5 volts [2]. One more factor affecting speed of operation is the parasitic capacitances in an integrated circuit. In GaAs, these parasitics are smaller as the entire substrate is considered an insulator.

Pure GaAs is semi-insulating with a high resistivity of 10⁷ - 10⁹ ohm-cm at 300°K, thus the substrate is effectively an insulator. With resistivity in this range, devices can be isolated for practical circuits with a separation of one or two microns on the surface of the

semi-insulating wafer. This results in a high layout packing density.

GaAs is typically thought to be radiation resistant [1]. This is true due to the higher bandgap electron voltage of 1.43 eV as compared to the 1.11 eV of silicon. Another fact supporting GaAs radiation resistance is the lack of a gate oxide which could trap charge.

A major limitation in GaAs is yield. The yields of large complex circuits are lower in GaAs than in silicon. The lower yield is partially due to the higher number of defects in the starting wafer. An additional limitation is a lower hole mobility compared to silicon, 400 cm²/V-sec versus 480 cm²/V-sec in silicon. This generally prohibits the use of complementary devices as used in CMOS.

N-Channel GaAs MESFET

The basic transistor made in the GaAs technology is the n-channel MESFET. Unique to the MESFET is the gate which forms a Schottky barrier with the channel. The following equation characterizes the MESFET for both regions, saturation and linear [1].

$$I_D = \beta(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \tanh(\alpha V_{DS}), \quad (1)$$
$$V_{GS} \geq V_T$$

The depletion MESFET threshold voltage, V_T , ranges from -0.3 to -3V. In enhancement MESFETs, V_T ranges from 0 to +0.3V. The channel-length modulation parameter, λ , is the same as for the MOSFET. The empirical hyperbolic tangent factor, $\tanh$, is determined by fitting to data. Coefficient α ranges from 0.3 for a long-channel ($L=20\mu\text{m}$) device to about 2 for a MESFET with $L=1\mu\text{m}$. The device transconductance parameter, β , is given in units of A/V² per millimeter width. In a typical digital GaAs circuit, the channel length, L , of all transistors is fixed at the minimum allowed value. For the circuit designer, the MESFET channel width, W , is generally the only variable.

The logic family of choice in the GaAs E/D technology is Direct-Coupled FET Logic (DCFL), and Source-Coupled FET Logic (SCFL). DCFL is a low power, single power supply family which uses both

enhancement and depletion MESFETs. It also gives a simple circuit design in a small area. Enhancement MESFETs current per unit device width is several times smaller than depletion MESFETs. This gives low power consumption (0.25 mW per circuit). DCFL has two disadvantages. One being low noise margins and the other being poor load drive current for capacitive loads. This is overcome by using SCFL circuits in the places which require high drive capability.

A typical two-input NOR gate transistor schematic is shown in Figure 1. It has a simple circuit design with only three transistors. Transistor Q3 is a load device and its size sets the current consumption for the logic gate. This NOR gate with gate width/length sizes of $10\text{ }\mu\text{m}/1.2\text{ }\mu\text{m}$ for the EFET and $4.8\text{ }\mu\text{m}/2.4\text{ }\mu\text{m}$ for the DFET can be made in less than $100\text{ }\mu\text{m}^2$.

Figure 1. DCFL 2-Input NOR Gate [1]

Source-coupled FET logic (SCFL) gives the capability to implement ultra-high-speed functions. The circuit topology is similar to ECL using only depletion mode FETs. Its speed is two to four times the speed of DCFL; however, it has a higher power dissipation. The source follower output buffer is used as a level shifter and high drive output. It requires a 5.2 volt supply voltage. Level translator cells are used to communicate between DCFL and SCFL on the same chip. An example of a SCFL inverter is shown in Figure 2.

Using GaAs technology for VLSI components dictates the DCFL family of logic elements. DCFL has the best speed-power product and the circuit techniques to attain the complexity of VLSI. Also, by designing with DCFL, other types of logic can be incorporated on the same integrated circuit substrate to accommodate special system requirements.

"Vitesse is currently capable of producing chips with over 300,000 gates at reasonable yields." [2] DCFL uses a constant power due to its current steering operation, hence, power supply noise caused by large current transients is eliminated.

Logic Design using DCFL

The basic logic elements in DCFL are the INVERTER and the two-input NOR gate. This is not to say that other functions cannot be realized. However,

Figure 2 SCFL Differential Inverter [2]

stacked n-channel MESFETs degrade circuit performance due to the critical control required for the threshold voltage of the EFET transistors, resulting in low noise margins [1]. A DCFL INVERTER, the simplest logic element, consists of one EFET and one DFET. The logic family operates from a single 2 volt power supply drawing a constant current from the positive supply rail. The DFET is a constant current load and the EFET acts as a current switch. Current from the load is steered through the pulldown switch or to the gate of the following switch.

DCFL tolerates a large variation in power supply voltage. Due to the characteristics of the load device, full switching speed can be achieved with a supply voltage as low as 1.2 volts. A critical factor which determines the performance of complex DCFL circuits is the uniformity of transistor threshold voltages (V_{TH}).

Inverter Layout Figure 3 shows a typical layout of an inverter.

Figure 3. Typical DCFL Inverter Layout

Full Adder Component The full adder logic element in DCFL demonstrates a design technique used when designing with GaAs. Recall that the basic logic

components in GaAs are the INVERTER and the NOR gate. The logic equations for a full adder are:

$$z_i = x_i \oplus y_i \oplus c_{i+1} \quad (2)$$

and

$$c_i = x_i y_i + x_i c_{i+1} + y_i c_{i+1} \quad (3)$$

Thus a full adder can be directly implemented from these equations using NAND and XOR gates. In GaAs, it is best to transform these equations to a full NOR implementation as shown in Figure 4

Due to the low supply voltage and low noise margin in DCFL, the NAND gate or logic using stacked EFETs cannot be easily produced. This leads to converting NAND logic to an equivalent logic implemented in NOR gates. This full adder is now designed using INVERTERS and NOR gates. The logic diagram is shown in Figure 4.

Unique to the GaAs technology is the drive characteristics of each logic element. In the full adder of Figure 4, the 2-Input NOR gates each must drive three loads. All other logic elements drive one load with the exception of the output buffers. To determine the drive required in the outputs, an estimate of the number of typical loads is made. If this full adder connects to an identical full adder, the drive requirement is four. There is a fan-in of four in this full adder for each input signal. The drive capability can be tailored for the specific cell used. However, this increases the customization of the layout and reduces the economies of scale factor for the circuit design. A drawback in selecting a higher than required drive capability is an increase in the direct current of the cell.

Figure 4. Full Adder Logic Diagram

Electrical Characteristics

Logic Swings / Voltage Levels The GaAs DCFL typically operates from a single voltage supply in a range from 1.2 to 2.5 volts. To interface to other technologies, translator cells and unique I/O cells are used on the GaAs integrated circuit. These unique cells for I/O require

additional power supplies. To interface to ECL, the power supply voltage V_{TT} requires -2 volts and V_{EE} requires -5.2 volts. To interface to TTL, the power supply voltage V_{TTL} requires 5 volts. Logic swing for DCFL is from 0.4 volts to 1.2 volts with a supply of 2 volts. TTL and ECL logic swings are accomplished with the appropriate I/O cell.

AC Characteristics The Vitesse E/D process is characterized as a high performance process with an operating frequency range from 300 MHz to 3 GHz. DCFL ranges from 300 MHz to 1.2 GHz with a gate delay less than 120 ps and a D-type Flip-Flop (DFF) Clk to Q delay less than 350 ps. SCFL covers the higher end of the operating frequency range from 1 GHz to 3 GHz with a DFF Clk to Q delay less than 180 ps [2].

Power Consumption GaAs DCFL has the lowest power consumption of all GaAs logic families consuming from 0.04 to 0.1 mW per gate. This is at a power supply level of 2 volts [1]. Higher power consumption is found in the SCFL cells (23 mW per complex cell) often used for interfacing to other technologies [3]. Care should be taken to minimize the total power consumption of the integrated circuit to less than 2 W due to package considerations. Additional power can be dissipated with cooling techniques, if required [3].

Die Size/Package Constraints In the Vitesse Semiconductor E/D GaAs process, the limit on the size of a die is given by the number of transistors which are incorporated on a single integrated circuit. Vitesse reports this number to be upwards of 300,000 [3]. When this number is calculated, the circuit design methodology must also be taken into consideration. Gate array, standard cell, full custom, and the amount of RAM all have a different impact on the maximum size a die can become. This is primarily due to the manufacturing yield. To reach a complexity of 100,000 gates, DCFL is required to minimize the power dissipation of the integrated circuit. The maximum power dissipation in a package should be kept below 2 watts [3]. Therefore, each integrated circuit design should have its power calculated prior to fabrication. If power dissipation is calculated to be greater than 2 watts, a smaller design or another form of packaging should be considered [3]. The circuit methodology (DCFL, SCFL) makes a significant difference in the power consumption. Special care should be taken to minimize the number of high power logic circuits and to minimize the power used in each cell.

Although power consumption is important, the package used is critical. The package limits the speed the die can operate by the inductances of the signal and power traces. These traces are from the external point of

contact with a printed circuit board or substrate to the bond wire which contacts the pad on the GaAs die. For this reason, special packages have been designed for packaging GaAs die. MOSIS supports the 28-pin LDCC (leadless chip carrier), 52-pin LDCC, and 132-pin LDCC packages. They also support the 52-pin LCC (leadless chip carrier) on request, plus many other pin grid array and LDCC packages which are supplied by Vitesse Semiconductor [4].

Design Methodology and Tools

The general methodology for digital circuit design employs the steps graphically described in Figure 5. Differences with CMOS design techniques will be described in detail. The tools used for CMOS which are not useful in GaAs design are also identified.

Many of the design tools presently used for CMOS designs are used for GaAs designs. These tools include VHDL, HSPICE, and the Berkeley CAD Tool Set which includes MAGIC. Unique aspects of each of these tools will be described as it applies to GaAs design.

Logic Simulation Logic simulation is accomplished in two steps using the VHDL simulator. The first is a high level design using the behavioral specifications in VHDL. This is the same technique as in CMOS and is technology independent. The result of the behavioral simulation is a specification for the desired logic design.

Once the behavioral specification is complete, a structural decomposition of the design is accomplished. The structural architecture of the design can be technology independent. In this case no timing specifications are included in the design. Once the technology base is defined for the design, timing constraints are included in the structural architecture. This is generally done at the lowest logic element, in this case, the INVERTER and the NOR gate. From the NOR gate and INVERTER, a standard cell library of logic elements is defined. Vitesse offers a standard cell library of military grade cells in their VCB50K Cell Library [3]. It is important to develop the full structural description of the GaAs circuit. This structural description is compared with the MAGIC layout for design verification.

Circuit Design The structural VHDL architecture of the design is defined using a particular set of logic cells or primitives. The power and timing budget for the design are used to select the logic family. Trade-offs are made among power dissipation, speed, pin count, and layout size in selecting the technology for the design. With a set of typical delay parameters for logic elements, the structural VHDL architecture simulation will report the full design timing. If this selection of logic family gives a timing beyond the allowed range, another logic family can be chosen and a simulation rerun.

Figure 5. GaAs Design Methodology

With a final simulation run of the structural VHDL architecture, a logic family is selected and a final power and timing is calculated. Transistor sizing is the next step in the design process. Transistor sizing is a critical step in the design process. This is done at the logic cell level and is also layout dependent.

Vitesse has supplied DCFL transistor sizing charts to assist in the initial selection of transistor sizes. These charts account for load and delay considerations, a 2 volt power supply, and 125°C temperature. Using the charts will yield transistor sizes satisfying the DC circuit operating requirements. These charts can be found in the UCSB GaAs Integrated Circuit Design Course Notes [5]. Once a set of transistor sizes are initially determined, refinement for a particular performance range is accomplished using HSPICE. The HSPICE model parameters are supplied by MOSIS for the Vitesse E/D GaAs wafer process. The model set includes a set of model parameters for typical enhancement and depletion MESFETs and half-sigma, one-sigma, two-sigma and three-sigma excursions in the fabrication process. Vitesse suggests it is sufficient to simulate prototypes with the typical-typical, one-sigma fast, and half-sigma slow parameter sets. Typical-typical refers to

the typical process parameters and typical thresholds. One-sigma fast refers to the one-sigma process parameter variation with the thresholds for a fast device. Half-sigma slow refers to the half-sigma process parameter variation with the thresholds for a slow device.

HSPICE by Meta Software is the circuit analysis program which is supported by Vitesse with a set of transistor and diode models for GaAs. The GaAs MESFET (a four terminal FET) is labeled by the letter J followed by a letter or a number. For example, a MESFET in the circuit being analyzed could be labelled J1. The four terminals are (in order) drain, gate, source, and body. Vitesse states [3],

"The backgate voltage (VBG) is set to 0.6 V above the most negative voltage. This voltage for VBG is the result of measurement and optimization and is standard for 2-volt operation. For 5-volt circuits, 2.0 V above the negative supply voltage should be used."

The model parameters supplied by Vitesse through MOSIS are supported through a hierarchy library and include typical model parameters plus models for the corners of the Vitesse process. Within the modes there are six choices of MESFET types. The model used should be the device closest in length to the MESFET being simulated. The standard EFET used is jfet04 (10x1.2μm) and the standard DFET load used is the jfet19 (10x2.0μm).

Five choices of diodes exist corresponding to the MESFETs above except for the jfet15 FET. They are attached the same as MESFETs (four terminals) with source and drain shorted. The width and length of the diodes must also be specified.

Layout

MAGIC The Berkeley CAD Tool Set which includes MAGIC is used for the layout of GaAs integrated circuits. MAGIC requires a technology file which specifies the mask layer definition and the design rules for feature spacing on the mask layers. The technology file used (edgaas.tech) was obtained from MOSIS and was developed by S. Butner at the University of California Santa Barbara VLSI Design Lab [5].

Two MAGIC commands crucial to the layout verification are *cif* and *ext*. The "design.cif" and "design.ext" files are used in the layout verification phase of the design methodology.

CIFPLOT CIFPLOT is an application which generates an electrostatic plot from the design.cif file. Once the design.cif file is generated on the Sun Sparcstations with MAGIC's *cif* command, it can be processed for a plot using CIFPLOT on a UNIX computer. The command for creating the electrostatic plot for GaAs is different than with a CMOS design as the stipple patterns and mask layers are different. Within

the command is the path for the GaAs specific stipple pattern file. Activate the CIFPLOT software by typing the following at the UNIX prompt, %:

```
%cifplot -P ~cad/lib/pat.gaas design.cif
```

The electrostatic plot of the design would then be generated. The stipple patterns for GaAs are defined in the file pat.gaas.

Extract The process of extraction is used to acquire the parasitic parameters from a specific MAGIC layout to use for resimulation in HSPICE. Once the *extract* (*ext*) command is used within MAGIC, the file "design.ext" is generated. This file is then acted upon with the *ext2sim* program to create a "design.sim" file from the extracted file information. The command from the UNIX prompt is:

```
%ext2sim design.ext
```

Normally this "design.sim" file is used for *esim*; however, *esim* does not function with GaAs, most probably due to the transistor designators. Next the *sim2spice* program is used to generate the "design.spice" file which contains the extracted parameters. The *sim2spice* program has a switch option, -h, which yields an HSPICE compatible file. The documentation states its compatibility with the SC MOS and GaAs technologies. The command from the UNIX prompt is:

```
%sim2spice -h design.sim
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This creates the "design.spice" file which holds the parasitic information about the MAGIC design. This version of *sim2spice* is the result of a request for the UCSB-modified 'sim2spice' program [5]. This program can also create input files for SPICE3 (default) by not using a switch option.

Layout Verification Using GES Layout verification using the Generalized Extraction System (GES) has been partially successful with GaAs [7]. GES has been used to verify a full adder layout. GES has been successful using the .sim file created by the *ext2sim* software. The commands used are identical to those for CMOS. The comparison to the structural VHDL description has been accomplished.

Testing

Logic Testing on IMS Tester Logic testing of GaAs devices on the IMS Tester uses the same methods as for CMOS. However, the user should be aware of the IMS Tester limitations. The fastest clock period is 10 ns with a minimum clock width of 4 ns. This may not be fast enough to determine the maximum clock frequency of many GaAs ICs. Voltage levels supported on the IMS Tester are fully compatible with GaAs requirements. However, the voltage levels must be limited to less than a 3 volt swing when testing DCFL GaAs. An electrical over stress causes the EFET to become open circuited resulting in a non-recoverable failure.

Packaging of GaAs Integrated Circuits

Size of Test Chips In many cases, the die size and corresponding package are dictated by the number of I/O signals and the equivalent gate count. For MOSIS submission, there are minimum size pad frames for the 52-pin leadless chip carrier package. The minimum is 2.16 mm [3]. The size of the test chips designed with 40 pads are approximately 2500 micron square.

Limitation of Packages The parasitic inductance and capacitance of the package traces and bonding wires impede the transmission of high speed edges from the GaAs die. Worst case is the power supply leads when multiple output devices are switching simultaneously as in a bus. When these outputs switch, "glitches" appear on the chip power buses. This problem must be minimized through the choice of the packages and circuit design techniques.

The MOSIS packages for GaAs have some of the necessary design techniques to maximize frequency of operation. They are designed with internal power and ground planes to minimize the inductance on the power pins. This is why there are dedicated power supply pins on the GaAs packages. Multiple power supply connections are also used to minimize power supply bounce due to output switching. Although not available through MOSIS at this time, some high pin count PGAs and LDCCs used by Vitesse have internal capacitors to reduce power supply noise. All Vitesse packages can be purchased separately, but are not stocked by MOSIS [4].

Design techniques can help minimize the effects of power supply noise by having one ground lead for every four output switching pads. The power supply for the output pads can be isolated from the internal supply connected to the logic cells. This power supply is thought of as a "dirty" supply. Power supply noise due to the outputs switching is isolated from the power supply lines used for the internal logic core. This would allow the internal logic core to continue to function. A feature of the Vitesse GaAs process is a third layer of metalization used exclusively for power and ground connections thus improving internal noise margins.

Vitesse has published measured bandwidths (highest signal frequencies) for their packages [4]. The 52-pin LCC/LDCC has a bandwidth of 2.46 GHz. With these packages, there are other methods to support higher bandwidths. Using two pads for every output, effectively making a parallel path to the outside of the package, is one method of removing the present operating frequency limitation.

All packages are cavity down, allowing access to the heat spreader built into the package cavity from the top of the printed circuit board or substrate. In order to cool the package and maintain the operating temperature limits for higher power circuits, a heat sink can be attached to the

heat spreader. Conversely, the cavity down package poses a problem during design analysis. It may be necessary to probe internal circuitry while testing the circuit. This is difficult to accomplish in a test mode with a cavity down package. At additional expense, the packages can be tooled cavity up. A cavity up package is necessary when the cooling method is built into the circuit board or substrate. A 256 pin LDCC cavity up package was tooled at government expense by ITT [6].

Package Diagrams The power pins are dedicated on the MOSIS supported GaAs packages. The power pin usage must be taken into consideration when designing the MAGIC layout of the GaAs integrated circuit die. MOSIS offers a 52-pin LDCC (leadless chip carrier) package for GaAs designs on Vitesse runs. This package is stocked by MOSIS or can be ordered from Vitesse. The package is 19.05 mm square and has a 5.3 mm by 4.7 mm cavity in a cavity down configuration. The leads are evenly distributed on all four sides on 1.27 mm centers. Figure 6 shows the top view of the 52-pin LDCC package. Table 1 shows the pin-to-function assignments for the 52-pin LDCC and 52-pin LCC packages.

Figure 6. TOP View of 52-pin LDCC/LCC Package [2]

Table 1. Pin-to-Function Assignments for the 52-pin LDCC/LCC Package [2]

Pin Number	Function
1-3,5-6,8,9,11-17	Input/Output
19-22,24-29,31-32	Input/Output
34-35,37-42,44,45	Input/Output
47,48,50-52	Input/Output
4,10,18,30,36,43,49	GND
7,46	(-)Supply 1
33	Supply 2
23	(substrate)

Figure 7 shows the bonding pad arrangement for the 52 LDCC/LCC packages. The bond fingers inside the package are arranged in two tiers. The first tier is a ring that connects to leads 4, 10, 18, 30, 36, 43, 49, and the bonding fingers for all other leads except 23 and 33.

Four corner bonding fingers are connected to leads 7 and 46. The second tier consists of a split ring. The top half is connected to lead 33; the bottom to leads 7 and 46. Lead 23 is connected to the package cavity. Seven pins are connected to external ground (GND), one pin to external positive supply, and two pins to the external negative supply. Thus, it has been optimized for ECL layout. Multiple bond wires can be attached to the outer rings for the positive and negative supplies. Also, multiple bonds can be connected to all of the GND pins. This leaves forty-one pins for signal connections.

Figure 7. Bonding Pad Arrangement for the 52-pin LDCC/LCC Package [4]

Input/Output Cells There are three sets of I/O cells available for use in designs. These are the GaAs, ECL, and TTL I/O cells. The GaAs I/O cells were designed at AFIT. The ECL I/O cells were designed at UCSB and were made available to AFIT by MOSIS. The ECL I/O cells have been used by UCSB in several designs [4].

The TTL I/O cells were designed at Vitesse Semiconductor and are part of their VCB50K Military Standard Cell Library [3]. Although these I/O cells were not designed at AFIT, they do conform to the MAGIC design rules. Technical data on the TTL I/O cells designed by Vitesse can be found in their Standard Cell Design Manual.

Summary

This paper presents the GaAs technology and the design methodology. The advantages and disadvantages of GaAs was reviewed for use in VLSI. The DCFL circuit family was chosen for VLSI use

The design methodology was presented and discussed in detail where it digresses from a CMOS design approach. The tools used to design with GaAs include VHDL, HSPICE, MAGIC, CIFPLOT, and GES. The MAGIC tool, sim2spice, was obtained from UCSB. Packages for GaAs die are different as the

operational frequencies can approach 3 GHz. Unique surface-mount packages are offered for GaAs die. Testing is a critical factor and can be accomplished on the IMS Tester.

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Biography

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