SILICON-HYBRID WAFER-SCALE INTEGRATION ACHIEVED

WITH MULTILEVEL ALUMINUM INTERCONNECTS

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ABSTRACT

A silicon-hybrid wafer-scale integration (WSI) technique has been developed to interconnect complementary metal-oxide semiconductor (CMOS) circuits. Electrical performance tests and processing diagnostics reveal that the interconnect design is very promising.

The wafer-scale integrated circuit was fabricated by mounting two CMOS integrated circuit die into etched wells and then planarizing the surface of the silicon wafer substrate. Next the wafer's surface was coated with a photosensitive polyimide and patterned with vias to accommodate the interconnecting conductors. The CMOS die were two-bit shift registers and were electrically interconnected with aluminum conductors using conventional silicon processing techniques. A diagnostic evaluation was accomplished to determine the electrical continuity of the conductors and via contacts. The functional conductors and via contacts were electrically characterized. When compared to a complementary wire-bonded interconnect scheme, the silicon WSI technology was found to be the superior performer at 1 MHz operating frequencies. Discontinuous interconnects were evaluated, and the failures were identified to occur at the severe topographical steps encountered on the substrate wafer's surface.

INTRODUCTION

Although the concept of wafer-scale integration (WSI) has existed for over twenty years, only recently have the benefits of this technology been seriously considered. In the 1960's, Texas Instruments pursued the first attempt at large scale integration using a WSI approach; however, it was discontinued for the more economical process of individually packaged circuit die [1]. For almost twenty years, WSI

was given little attention until the delays encountered in conventional printed circuit interconnects became intolerable [2]. Since conventional integrated circuit (IC) packaging increases the effective area consumed from two to ten times the actual chip area, interconnect lengths can be reduced by more economical packaging techniques [1]. Because WSI can eliminate individually packaged chips and result in faster systems, several organizations have embarked on developing this new technology [3].

In 1986, Donald Meyer, a consultant with New Technology Concepts, categorized all WSI techniques into two basic approaches -- "monolithic" or "hybrid" [4]. Monolithic WSI incorporates redundant copies of each circuit to improve wafer yield. The large-scale integration (LSI) practice of dicing and sorting circuits is not performed. Faulty circuits are left on the wafer and bypassed with "discretionary" wiring techniques. On the other hand, hybrid WSI uses only functional circuit die. These die are then mounted on a common wafer substrate where the interconnects are created [4].

FABRICATION PROCESS

The silicon-hybrid WSI technique was accomplished using three basic processing steps. First, a planarizing wafer substrate was prepared by etching wells to accommodate two CMOS IC die. Next, the die were mounted into the substrate's wells. Finally, the interconnect metallization pattern was deposited and patterned using alternating layers of a photosensitive polyimide and an aluminum (Al) film.

The WSI substrate was prepared by a method similar to the technique employed by the Auburn University researchers [5]. Two rectangular holes were etched into a (100) silicon wafer using the following processing steps:

1. The wafer was isotropically etched to a specific thickness with a 15:5:2 solution of nitric acid:acetic acid:hydrofluoric acid [6].

2. A thick silicon-dioxide layer (2.4 microns) was thermally grown over the wafer's surface.

3. Windows for the the IC die were photolithographically patterned with positive photoresist.

4. The windows were opened in the silicon dioxide layer using a buffered hydrofluoric acid etchant.

5. The IC die wells were anisotropically etched through the silicon wafer with a potassium hydroxide etchant (25% potassium hydroxide, 60% deionized water, and 15% isopropyl alcohol heated to 70°C).

The IC die were mounted into the etched substrate wells using three steps. First, the IC die were bonded into the substrate's wells. The technique used to achieve this step was similar to that derived by the Auburn researchers [5]. The die and the etched silicon substrate were placed face down onto an optical flat, and the adhesive was deposited in the gap between the die and the substrate (Figure 1a). The optical flat established a planar surface while the adhesive cured. Next, a supporting silicon substrate was attached to the bottom of the planarizing substrate. Adhesive was applied to the bottom surface of the planarizing substrate, and a clean unprocessed wafer was placed over the adhesive (Figure 1b). A constant force was applied to the support substrate while the adhesive cured. Finally, the entire wafer was subjected to a 250°C cure (Figure 1c). The adhesive (Master Bond EP34CA Special) for mounting the die is a dielectric-filled epoxy resin system synthesized to match

the temperature coefficient of expansion (TCE) of silicon ($2.5 \times 10^{-6}/^{\circ}\text{C}$).

After the IC die were mounted, they were interconnected with patterned Al conductors. These interconnects were fabricated with alternate applications of polyimide and Al film (Figure 2). A finished hybrid WSI circuit is shown in Figure 3.

EXPERIMENTAL

As part of the fabrication process development, the utility of the photosensitive polyimide as an intermetallic dielectric was evaluated. In addition, several photoresists were

screened for patterning the aluminum interconnect conductors.

The photosensitive polyimide utilized was Selectilux HTR 3-200 (EM Industries, Hawthorne, NY). Because the wafer-to-die transition region often experienced step height differentials as large as 18 microns, the polyimide was evaluated for its ability to planarize these severe topographical features. For planarization purposes, a thick polyimide layer (approximately 10 microns) was required. This thickness was achieved with one application of Selectilux HTR 3-200. However, reliable contact vias were difficult to produce through this thick film. Subsequent experimentation revealed that sloped sidewall vias resolved this problem.

As a negative-acting photoresist, Selectilux HTR 3-200 can be patterned with sloped vias using proximity printing. It has been shown that the difference between the size of a mask feature and the size of the feature printed on the photoresist ($2y$) is given by [7]:

$$2y = Nz^{1/2} [\ln(kE_i) - \ln(E_p)]$$

where

y is the projected runout of a mask edge (cm),

N is a parameter incorporating constants for the optics of the printer ($\text{cm}^{1/2}$),

z is the separation between the mask and the top surface of the photoresist (cm),

k is the value of (E_p/E_i) when $y = 0$,

E_i is the energy density incident on the mask (mJ/cm^2), and

E_p is the threshold energy density of the photoresist (mJ/cm^2).

Consequently, the size of the photoresist feature can be changed by varying the exposure energy density on the mask (E_i),

the separation between the mask and the top surface of the photoresist (z), or the threshold energy density of the photoresist (E_p).

With the exposure and threshold energy densities held constant, the polyimide layer was exposed for several separations (z) between the mask and the

top surface of the polyimide. Optimally, it was found that a 10 micron proximity separation and an exposure energy density

of 215 mJ/cm^2 incident upon a 20 micron thick layer of uncured polyimide produced vias with a sidewall slope of 135° . After a 250°C cure, the polyimide's thickness decreased to 10 microns.

The aluminum interconnects were fabricated by depositing a 1.2 micron thick film of evaporated aluminum over the patterned polyimide layer. The aluminum film was etched with a solution composed of 5 parts nitric acid, 2 parts phosphoric acid, and 5 parts acetic acid. Five photoresist mask materials for patterning the Al interconnects were evaluated using the following criteria: (1) line resolution, (2) step planarization, (3) compatible stripping and (4) resistance to the Al etchant. Shipley M1350J positive photoresist yielded optimum overall performance.

After each wafer-scale circuit was fabricated, the electrical continuity of the interconnects was evaluated. For the WSI circuits fabricated in this investigation, 12 of 16 transition crossings passed the continuity check, and 11 of 12 via sidewalls were covered with Al. The electrical performance of the successful interconnects were evaluated. This evaluation was accomplished by driving a single interconnect path between the IC CMOS shift registers. A schematic of this configuration is shown in Figure 4. When the circuit's output (A) drove the hybrid WSI configuration at 1 MHz, points B and C were probed to determine the effect of the interconnect between points B and C (these probe points are also highlighted in Figure 3). When compared to a complementary wire-bonded sample driven at 1 MHz, the WSI configuration displayed insignificant signal distortion (Figure 5a). However, the distortion in the wire-bonded configuration is distinctly featured between points B and C (Figure 5b). A rise time of 10 ns was measured in both cases.

DISCUSSION

The fabrication of a hybrid WSI circuit was not completely successful, and the primary failure can be attributed to open circuits in the interconnect conductors. These faults occurred predominantly in the transition region between the wafer and the die, and at the edge of the vias formed in the polyimide. Figure 6a illustrates an interconnect

that successfully traverses the transition region, while Figure 6b depicts an unsuccessful crossing. The severe step height differential has been attributed as the source of the fault. A void in the wafer-to-die transition region may create an abrupt step which may not be planarizable. As a result, the positive photoresist conductor patterning layer would likely exhibit the same behavior. Consequently, when the wafer is immersed in the aluminum etchant, the positive photoresist pattern will be distorted at the transition region and expose the underlying aluminum. Therefore, continuous interconnects could be compromised by three inadequacies in the processing schedule: (1) an uneven fill of epoxy in the wafer-to-die transition region, (2) poor step coverage by the polyimide dielectric in the transition region, and (3) inadequate planarization.

Very little can be done to prevent the uneven fill of epoxy in the wafer-to-die transition region. To resolve the incomplete fill of epoxy, a low-viscosity gap filler could be utilized to planarize the wafer-to-die transition region. Before depositing the bonding epoxy, a low-viscosity material could be deposited in the gap using a microsyringe. Because this material will interface with the planarizing polyimide, Selectilux HTR 3-200 is recommended. After this initial polyimide layer is completely cured (350°C), the bonding epoxy can be deposited into the gap. The support substrate can then be attached in the manner described earlier.

To preclude epoxy from flowing onto the top surface of the substrate wafer, irregularities in both the wafer and die surfaces must be minimized. It is recommended that 400 micron thick (100) silicon wafers be utilized as substrates (both surfaces polished). The uneven topography of the IC die surface is caused by the layers of CVD oxide, polysilicon, and aluminum used to fabricate the circuit. To minimize the effect of the die's uneven topography, a dielectric border could be fabricated around the perimeter of the die whose thickness equals that of the die's most significant feature excursion. This border will insure that the die will lay flat on the optical flat.

The evaluation results indicated that polyimide is a superior step planarization material. A thick layer for patterning the conductors is also highly desirable. EM industries produces a positive photoresist (Selectilux P2100-100) that can be applied in layers to achieve a thickness

of 3.6 microns [8].

CONCLUSION

A silicon-hybrid wafer-scale integration technique has been developed and evaluated. Two CMOS circuits were mounted in a host silicon wafer substrate which provided a planarizing surface and physical support for the wafer-scale interconnects. A photosensitive polyimide, Selectilux HTR 3-200, was used as an isolation dielectric to achieve the interconnects. In addition, the polyimide enhanced the planarization of the wafer's surface. As a result, this dielectric allowed the interconnect vias to be directly patterned into the polyimide. To interconnect the two IC die, aluminum conductors were patterned on the polyimide's surface using a positive photoresist mask and wet chemical etching process.

Electrical performance tests were conducted to evaluate the quality of these interconnects. The parametric tests showed that the signal delay, attenuation, and distortion were indistinguishable for a one centimeter interconnect path length. When compared to complementary wire-bonded interconnects, the WSI aluminum interconnects yielded lower signal distortion.

Several fractures in the interconnects were discovered at the wafer-to-die transition and at the via step edges. Fractures in the transition region can be attributed to (1) uneven fill of epoxy in the transition region, (2) inability of the polyimide to sufficiently planarize the transition steps, and (3) insufficient planarization provided by the photoresist as an aluminum etch mask.

REFERENCES

1. McDonald, Jack F. "The Trials of Wafer-Scale Integration", IEEE Spectrum, vol. 21, pp.32-39, 1984.
2. Blodgett, Albert J. "Microelectronic Packaging", Scientific American, vol. 249, pp.86-96, 1983.
3. McDonald, Jack F., et al. "Multilevel Interconnections for Wafer Scale Integration", Journal of Vacuum Science and Technology, vol. 4, pp.3127-3138, 1986.
4. Meyer, Donald E. "Wafer Scale Integration? Time to Get Serious", Semiconductor International, vol. 9, p.32, 1986.
5. Johnson, R. Wayne, et al. "Silicon Hybrid Wafer-Scale Package Technology", IEEE Journal of Solid State Circuits, vol. 21, pp.45-51, 1986.
6. Elliot, David J. "Microlithography--Process Technology for Integrated Circuit Fabrication", New York: McGraw-Hill Book Company, 1986.
7. McGillis, D.A. and Delmar L. Fehrs. "Photolithographic Linewidth Control", IEEE Transactions on Electron Devices, vol. 22, pp.471-477, 1975.
8. EM Industries, Inc., Advanced Chemicals Division, "Selectilux P2100 Positive Photoresist", Hawthorne, NY.

Figure 1. Three Fabrication Steps Resulting in a Dual Wafer Structure. (a) The IC die were mounted face down onto the optical flat, (b) the support substrate was attached to the bottom of the planarizing substrated, (c) the entire structure was subjected to a high-temperature cure cycle.

(a)

(b)

Figure 2. Interconnect Fabrication. The interconnects were fabricated with alternate applications of (a) polyimide and (b) aluminum.

Figure 3. Two CMOS IC Die Integrated by the Wafer-Scale Scheme. (1) Planarizing substrate, (2) integrated circuit die, (3) via alignment marks, and (4) aluminum interconnects.

Figure 4. Schematic of the Parametric Test Configuration. The interconnect is excited by the two-bit shift register (only the output inverter is shown) of the first die at point A. The interconnect is probed at points B and C. Point B is at the input of the two-bit shift register of the second die (only the inverter is shown), and point C is at the external pad of the wafer-scale circuit. These points are highlighted in Figure 3.

Figure 5a. The Output Signal Measured Along the Printed Interconnect at Points B and C at 1 MHz. These points are highlighted in Figure 4. There is less distortion in the waveform compared to the wire-bonded interconnect (Figure 5b). (Vertical axis: 2 volts/division, Horizontal axis: 200.0 nsec/division).

Figure 5b. The Output Signal Measured Along the Wire-Bonded Interconnect at Points B and C at 1 MHz. These points are highlighted in Figure 4. Note the signal degradation evidenced by the rise time of the waveform at C. (Vertical axis: 2 volts/division, Horizontal axis: 200.0 nsec/division).

Figure 6a. Interconnect Successfully Crossing the Wafer to-Die Transition Region. (SEM photograph at 400x magnification).

Figure 6b. Interconnect Fractured at the Wafer-to-Die Transisition. (SEM photograph at 400x magnification).