90° Hybrid-Coupler Based Phase-Interpolation Phase-Shifter for Phased-Array Applications at W-Band and Beyond

Sadia Afroz and Kwang-Jin Koh

Multifunctional Integrated Circuits and Systems (MICS) Group, ECE Department, Virginia Tech

Abstract — This paper presents a 90° hybrid-coupler based passive phase interpolator that is utilized to design a W-band 5-bit phase shifter in 0.13 µm SiGe BiCMOS process. In the proposed phase shifter, amplitude weighting is made first by VGAs. Then, a 90°-hybrid performs I/Q phase splitting and phase interpolation to synthesize all four quadrant phases. In this way, the accuracy of the phase synthesis is less vulnerable to an amplifier loading effect. Further, by cascading all building blocks with a low matched impedance the phase shifter will be less sensitive to parasitic capacitance, suitable for mm-Wave applications. The phase shifter is optimized for a transmitter application and the measured peak-to-peak gain variation for all 5-bit phase states is 4.8-9.7 dB at 94 GHz. The measured rms gain error is < 1.6 dB over 93-108 GHz. The measured RMS phase error is < 1.5° at 94 GHz. The input and output P_{-1dB} is -13 dBm and -4.7 dBm, respectively, at 94 GHz. The chip consumes 37 mW from 2.2 V supply voltage. The chip size is 1.87×0.75 mm².

Index Terms — BiCMOS, Hybrid coupler, W-band, phased array, phase shifter, Vector modulator.

I. Introduction

For phased arrays at microwave to low-end mm-Wave band, passive phase shifters based on switchable LC networks have been popular [1]. This is because the loss from inductor could be mild due to its smaller size as frequency increases. However, when implemented in silicon process the passive phase shifter (PS) loss will become dominated by a switch loss that could be substantial at W-band and higher frequencies due to a high NMOS switch turn-on resistance. Further, the passive PS suffers from ingrained tradeoff between phase resolution and loss: namely, higher phase resolution requires cascading more switched LC networks, increasing loss exponentially. This paper presents an original approach of interpolating phase in a passive way to synthesize a phase by utilizing quadrature phasing and power combining capability inherited in 90° hybrid-coupler. Unlike conventional vector modulators [2], in the proposed PS a VGA accomplishes real amplitude weighting first and then a 90°-hybrid establishes a complex weighting, creating all four quadrant phases with no suffering from the phase resolution and loss tradeoff. The proposed PS is favorable for single-ended signal processing and all building blocks can be designed with 50-Ω matched impedance, suitable for a large-scale array (# of element > 100's ~ 1000's) at W-band and beyond.

II. 90° Hybrid-Coupler Based Phase Interpolation

Fig. 1 shows conceptual diagram of synthesizing four quadrant phases by interpolating differential input phases in a 90° hybrid-coupler. Suppose the input is a narrowband signal

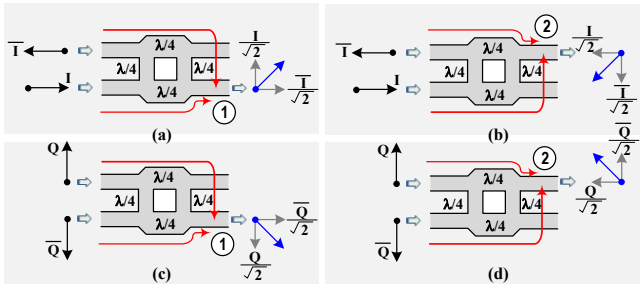

Fig. 1. 90° Hybrid-Coupler based phase interpolation to synthesize four quadrant phases with differential quadrature inputs.

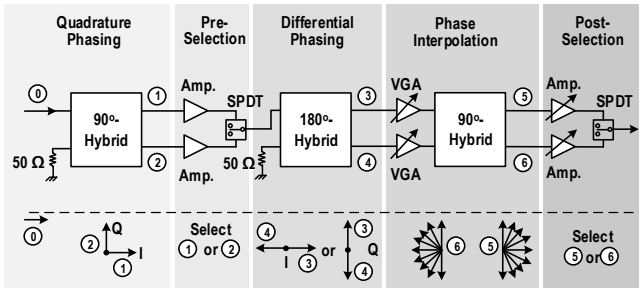

Fig. 2. Block diagram of the phase shifter employing the 90° hybrid-coupler based phase interpolation with representing vector signal phasing at each function block.

having λ-wavelength and all ports are terminated with a matched impedance. In Fig. 1(a) when the differential signals I and $\bar{I}$ are injected through two isolation ports, I and $\bar{I}$ are delayed by 90° and 180°, respectively, because of λ/4 and λ/2 path delays, and added together in power domain at the output port ①, creating 45° phase. When taking output at port ②, the phase will be inverted (Fig. 1(b)). Similarly, when applying quadrature differential (Q and $\bar{Q}$) input, the hybrid can synthesize 315° and 135° phase in Fig. 1(c) and (d), respectively. Basically, the hybrid performs quadrature phase splitting and phase interpolation simultaneously and can synthesize all four quadrant phases with quadrature differential inputs.

III. Phase Shifter Architecture

The block diagram of the proposed phase shifter leveraging the hybrid phase interpolation is shown in Fig. 2, where the functionality of each block is also illustrated using signal vector representation. Here, the passive 90°- and 180°-hybrids are interposed in between the cascaded amplifiers stages to create basis I/Q signals. The input signal will be split into I/Q vector signals in the first 90° hybrid coupler (① and ②). The in-phase (V_I) and quadrature phase (V_Q) component signal can be

expressed in terms of RF input signal (V_{in}) as $V_I = V_{in}/\sqrt{2}$ and $V_Q = -jV_{in}/\sqrt{2}$, respectively. One of the I/Q phases will be selected in the pre-selection stage and the 180º-hybrid generates differential phases based on each set of the I/Q vectors at ③ and ④, which are fed to the variable gain amplifiers (VGAs) for further fine phase processing. The second 90º-hybrid plays as a phase interpolator: i.e., it takes independently weighed differential inputs, changes the differential phases into quadrature phases, and finally adds the quadrature-phased signals at the outputs. A continuous gain control in the VGAs will result in two-quadrant continuous phases at each output of ⑤ and ⑥, respectively. The cascading of the post phase selection stage completes 360º of phase rotation at the final output. If the weighting factors of the two VGAs are $\{w_u, w_l\}$ and assuming losses from hybrids and SPDTs are properly compensated by the amplifiers, the output signal of the phase shifter can be expressed as,

$$V_{out} \propto \begin{cases} (w_u + jw_l)\cdot V_{in} \ \ or\ (-jw_u - w_l)\cdot V_{in}\ ; If\ V_I\ is\ selected. \\ (-jw_u + w_l)\cdot V_{in}\ or (-w_u + jw_l)\cdot V_{in}; If\ V_Q\ is\ selected. \end{cases}$$

where the 90º hybrid coupler essentially generates a complex weighting. In the proposed PS, amplifiers and phase shifter functionalities are merged together in a distributed way, where majority of phase shifter function is accomplished by the passive hybrids while amplifiers provide necessary amplitude weighting for the fine phase interpolation.

IV. Building Block Design

Variable Gain Amplifier: In the VGA schematic shown in Fig. 3(a), the variable gain function is realized by steering bias current from the main signal path. All the transistors have equal emitter length of 6 µm and are biased with maximum 4 mA DC current from 2.2 V supply. All the inductors and interconnects are modeled using SONNET EM simulation. Bypass capacitor ($C_B \approx$ 660 fF) is added immediately after the load inductors to avoid any parasitic inductance at the V_{CC} interconnect and to make a solid AC ground at 94 GHz. The simulated VGA gain ranges -20~10 dB. The bias current is not fully cut off but keeps ~90 µA at the minimum gain setting to maintain S_{22}<-10 dB for impedance matching with following 90º-hybrid.

90º- and 180º-Hybrids: Fig. 3 (b) and (c) show the SONNET layout of the distributed 90º-hybrid and lumped 180º-hybrid couplers. In the 90º-hybrid λ/4 35-Ω T-lines are meandered to reduce its size. The simulated loss of the 90º hybrid coupler is 1~1.5 dB at 94 GHz and phase error is < 5º over 84-118 GHz. Lumped 180º hybrid gives smaller area compared to distributed hybrid coupler. The inductance (L) and capacitance (C_1) are determined by the equation: $\omega L = 1/\omega C_1 = \sqrt{2}Z_o$ [3]. For Z_o= 50 Ω at 94 GHz, L= 120 pH and C_1= 24 fF. The measured loss in the lumped 180º hybrid coupler is <-1.5 dB and phase error is < 8º at 90-100 GHz.

Loss Compensation Amplifiers: The amplifiers in the pre and post phase selection stages are designed with the same cascode topology as VGA and in/out matching networks are optimized accordingly to accommodate different layout parasitics. In Fig. 4(a) the PMOS M_1 and R_1 set a nominal bias current of 4.5 mA

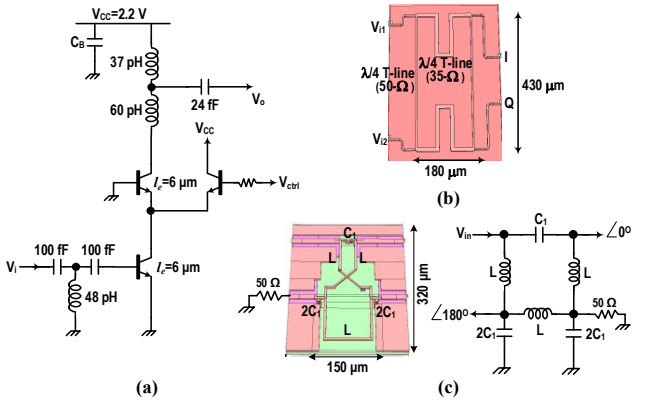

Fig. 3. (a) Schematic of VGA, and Sonnet layout of (b) distributed 90º hybrid coupler and (c) Lumped 180º hybrid coupler with schematic.

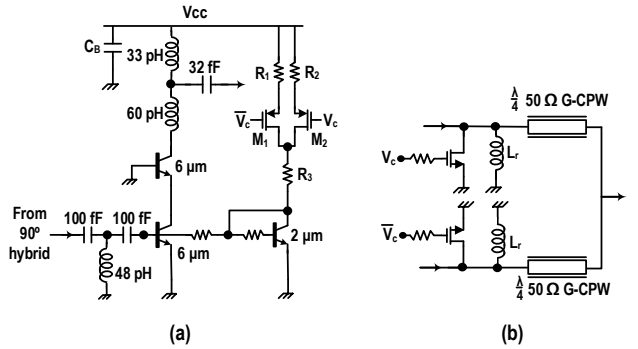

Fig. 4. (a) Schematic of amplifier with two bias control and (b) SPDT switch in pre- and post- selection operation block.

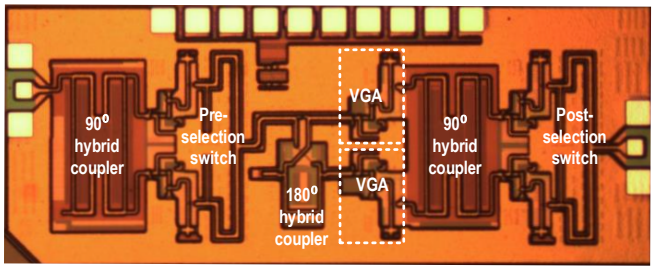

Fig. 5. Phase Shifter chip photograph (1.87×0.75 mm² including pads).

for the amplifier. When non-selected, the amplifier should be turned OFF to minimize DC power dissipation. But the ports of 90º hybrid coupler are assumed to have close to 50 Ω matched impedance all the time for a low quadrature phase error. So, instead of turning OFF the amplifier, a small bias current (~ 60 µA) set by the bias path composed of M_2 and R_2 has been applied to keep S_{11}< -10 dB, ensuring minimal power consumption as well as low quadrature phase error from the 90º hybrid couplers. The maximum gain of the pre- and post-selection stages (including SPDT switch) are 2 dB and 8 dB with 2.6 mW and 10 mW DC power consumption, respectively. The amplifier gain in the post-selection stage can be controlled to reduce gain variation across different phase states.

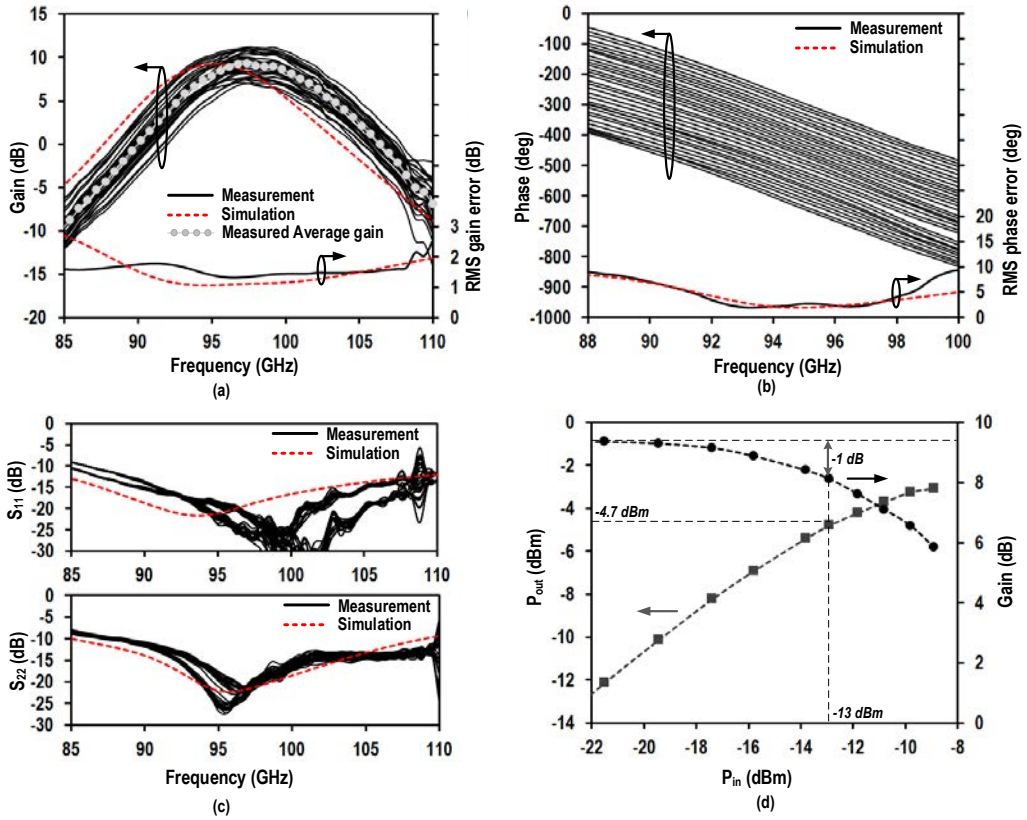

Fig. 6. Measured (a) Gain (S_{21}), (b) Absolute phase and RMS phase error, (c) Input (S_{11}) and output (S_{22}) reflection coefficients of the phase shifter and (d) Output power and power gain verses input power at 94 GHz.

SPDTs: In the pre- and post-selection stages, phase selection is achieved by a SPDT switch (Fig. 4(b)). The SPDT switch is based on λ/4 co-planner T-line that provides a high impedance when the NMOS switch is on. The NMOS size (40μm/0.12μm) is optimized for a low loss (L=2.5 dB) and the inductor L_r (95 pH) resonates out the switch OFF state parasitic capacitance.

The simulated overall gain of the phase shifter is 5-9 dB at 94 GHz with < 1.5 dB gain error and < 6º phase error at 90-100 GHz. The phase shifter was optimized for linearity to be used in a transmitter before power amplifier. With a maximum gain setting, the simulated input and output P_{-1dB} is -11 dBm and -3 dBm, respectively, at 94 GHz.

V. Experimental Results

Fig. 5 shows the chip photograph of the phase shifter. The chip is fabricated in IBM 0.13 μm SiGe BiCMOS with f_T/f_{max} = 200/220 GHz. The chip size is 1.6 × 0.65 mm² excluding pads. The chip is measured on wafer after standard GSG SOLT calibration. Fig. 6 shows the measured S-parameter results for 5-bit phase states of the phase shifter. The peak gain is 7.7-11 dB and shifted to 97 GHz. The frequency shifting may be caused by custom made metal-oxide-metal (MOM) capacitance variation in this process that is used at each amplifier's output matching network. The gain is 4.8-9.7 dB at 94 GHz. About 1 dB of input and output GSG pad losses are de-embedded. The average gain is 9 dB at 97 GHz and 3-dB bandwidth is 93-103 GHz. The RMS gain error is 1.5 dB at 94 GHz and < 1.6 dB over 93-108 GHz. The measured phase error is < 4º over 92-98 GHz and < 9º over 88-100 GHz. The measured S_{11} and S_{22} are below -10 dB over 85-110 GHz. Fig. 6 (d) shows measured output power and gain verses input power at 94 GHz. Measured input and output P_{-1dB} is -13 dBm and -4.7 dBm, respectively, at maximum gain state which is enough to drive PA. The output

Table I. Performance Summary and Comparison

	This Work	TMTT 2014 B. H. Ku *et al.*[2]	TMTT 2013 F. Golcuk *et al.* [4]	TMTT 2013 S.Y. Kim *et al.* [1]	TMTT 2015 A.Natarajan *et al.* [5]
Frequency (GHz)	92-100	76-84	90-100	74-86	88-96
Type	Vector modulator	Vector modulator	Vector modulator	Passive switched LC	Active+ RTPS
Gain (dB)	6-10	-5	-5 ~ -7	-6.5 ~ -9.5	-3.5
P_{sat} (dBm)	-3	1	-5	N/A	2 for TX*
Phase resolution	5	5	4	4	5
RMS gain error (dB)	< 1.6	<1.5	< 1.2	< 1	<2.5
RMS phase error (deg)	< 5º	<11º	< 4º	< 11º	<10º
Power consumption	37 mW	56 mW	69/137 mW for RX/TX*	60 mW for RX*	23 mW
Process	0.13μm SiGe BiCMOS	0.13μm SiGe BiCMOS	0.13μm SiGe BiCMOS	0.13μm SiGe BiCMOS	0.13μm SiGe BiCMOS

* Includes the whole RX or TX phased array single element.

saturated power is close to -3 dBm. The overall power consumption in the phase shifter including DC bias circuits is 37 mW from 2.2 V supply voltage. Table-I summarizes and compares major measured performance with current state-of-the-art W-band phase shifters.

VI. Conclusion

A vector modulator type phase shifter for W-band phased arrays is implemented in 0.13 μm SiGe BiCMOS process. In conventional active phase shifter, a quadrature network precedes active amplifiers which interpolate I/Q phases and typically the accuracy of the I/Q network suffers from a loading effect from the amplifiers. However, in the proposed phase shifter, active amplifiers precede a 90°-hybrid and amplitude weighting is performed before the phase interpolation that is accomplished in a passive way by the 90°-hybrid. In such way, by designing the weighting amplifiers with a matched impedance, the I/Q accuracy and thereby accuracy of phase interpolation is not sensitive to the amplifier loading. All building blocks can be cascaded with a matched low impedance to make less vulnerable to parasitic capacitance effect, suitable for mm-Wave applications. The proposed phase shifter is particularly promising at the high-end of mm-Wave band since the size of hybrids becomes smaller for on-chip integration, resulting in a low-loss compact phase shifter at the extremely high frequencies.

Acknowledgement

This work was supported by DARPA Strategic Technology Office (STO) under the program contract, HR0011-14-C-0128. The authors would like to thank Mr. Bruce Wallace (DARPA STO PM), Eric McNett (DARPA STO), and Alfred Hung (Army Research Lab.) for the program support. We are also thankful for Rhode & Schwarz's supporting W-band measurement equipment.

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