Microdegree Frequency and Phase Difference Control Using Fractional-N PLL Synthesizers

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Abstract—Two independently programmable on-chip delta-sigma fractional-N phased-locked loop (PLL) synthesizers were developed in 65 nm CMOS with a total die size of 2 mm x 2 mm to demonstrate a millidegree phase shifter. Both PLLs use a 24 bit fractional modulator, thus a theoretical phase shift as small as 21 microdegrees is possible. Due to limitations in the noise floor at microwave frequencies, data was collected at postdivided frequencies 50 MHz and 400 MHz resulting in a best case measured phase step of 21 millidegrees at 50 MHz with a high degree of measurement certainty.

Index Terms—Fractional-N frequency synthesizers, phase control, phase-locked loops (PLLs).

I. INTRODUCTION

Zero-IF (ZIF) and low-IF architectures employ quadrature demodulation techniques that theoretically provide infinite image rejection during down-conversion. However, in practice, ZIF and low-IF quadrature architectures will suffer in IF rejection due to mismatches between the in-phase (I) and the quadrature (Q) branches of the receiver. Known as I/Q mismatch, this phenomenon is primarily introduced at two different points in the receiver; in the local oscillator (LO) and in subsequent mixers and filters [1], [2]. The introduced mismatch is a result of the finite tolerances of the analog components implemented in the receiver. In addition, the LO can introduce an imbalance due to imperfect orthogonality. By implementing a phase shifter in the LO with very fine phase control, deep IF nulling can be achieved.

Recent work performed by Tajima et al. in [3] demonstrated a fractional-N PLL phase shifter through cyclic shift and composition of control data of frequency dividers. Their work resulted in a system whose measured phase difference error was no greater than $\pm 2^\circ$ within the L-band. PLL-based direct digital synthesizers (DDSs) phase shifters have been reported in [4], [5] with similar measured phase difference errors.

This paper demonstrates a delta-sigma fractional-N PLL phase shifter capable of millidegree phase steps through a 24 bit fractional modulator. Phase shift steps in the time domain are inversely proportional to the frequency of the output signal in as such that phase changes become difficult to detect at microwave frequencies. Using conventional measurement equipment, phase steps were measured

at postdivided output frequencies 50 MHz and 400 MHz and compared to both simulated and predicted values. In addition, regression data is presented to demonstrate the capability of the phase shifter beyond the noise floors of both the simulation and measurement setups.

II. SIMULATION AND EXPERIMENTAL SETUP

Two on-chip independently programmable delta-sigma fractional-N PLL synthesizers (north and south) with 24 bit fractional accuracy were developed in 65 nm CMOS as seen in Fig. 1. The chip requires a 256 bit codeword to control the programmable settings of both the north and south PLLs.

Fig. 1. System level diagram of one of the two identical on-chip PLLs.

Each PLL occupies $200 \mu\text{m} \times 350 \mu\text{m}$ of real estate on-chip with a total die size of 2 mm x 2 mm and has an output frequency range of approximately 1.5 MHz to 3.2 GHz with an input frequency range of 1 MHz to 1.2 GHz. The ability to independently program the north and south PLLs allows for the phase of one of the PLL outputs to act as the reference in the setup. With 24 bit fractional accuracy, each PLL has a theoretical phase step capability of

$$\Delta\phi = \frac{360^\circ}{2^{24}} = 21 \text{ microdegrees.} \quad (1)$$

The phase step in (1) can be translated into the time-

domain, Δt , through the output frequency of the PLL, f_o , by

$$\Delta t = \frac{\Delta\phi}{f_o 360^\circ}. \quad (2)$$

Equation (2) reveals a trade-off between the output frequency of the PLL and the time step; as the output frequency increases the time step decreases and requires a more precise and higher-certainty measurement. In particular, any experimental setup must be able to measure a time step equal to or less than

$$\Delta t \leq \frac{1}{2^{24} f_o} \quad (3)$$

in order to approach the theoretical limit in (1). At microwave frequencies, the time step in (3) is difficult to measure and therefore requires the VCO output to be postdivided to RF frequencies during experimentation.

The fractional-N PLL was simulated in a cycle accurate Verilog/Verilog-A simulator while the delta-sigma modulator was modeled at the gate level in Verilog. The analog portions of the loop employed abstracted models that were compared against SPICE for accuracy. The fractional-N PLL was designed with a high bandwidth enabled in part with a quantization noise canceling DAC. However, the small amount of output jitter contributed by the fractional-N modulator noise limits the observable resolution.

In order to obtain measured data to compare to simulated, the chip was mounted to a printed circuit board as seen in Fig. 2 and Table I lists the PLL settings necessary to produce the desired output frequencies during experimental testing. The test board consists of separate outputs for the north and south PLLs, DC voltage regulators, a high impedance input buffer to the programming registers, and two options for providing the reference clock to the chip; either an on-board 50 MHz crystal can be used to provide the reference signal for both PLLs or the crystal can be placed in a tristate mode and the reference clock can be fed into the test board from an external source. The PLL was programmed at 60 MHz using an FPGA.

During both simulations and measurements, the fractional-N noise is roughly 4ps RMS. Comparing two output phases, each measured over 12,500 samples, and each having an RMS jitter of 4ps RMS leads to an accuracy of

$$\frac{\sqrt{2}(4 \text{ ps})}{\sqrt{12,500}} = 0.05 \text{ ps} = 11 \text{ millidegrees}. \quad (4)$$

For the experimental setup, the output of the north PLL provided the reference phase while the south was adjusted such that the resulting phase step, in degrees, was equal to

Fig. 2. A test board with the mounted chip. Important circuit components and ports have been identified and labeled.

TABLE I
PLL SETTINGS TO PRODUCE A CONSTANT 50 MHz AND 400 MHz OUTPUT FREQUENCY.

PLL Setting	$f_o = 50 \text{ MHz}$	$f_o = 400 \text{ MHz}$
FCLK	50 MHz	400 MHz
REFDIV	1	8
FREF	50 MHz	50 MHz
FBDIV	49	64
FVCO	2.45 GHz	3.2 GHz
POSTDIV	49	8

$$\Delta\phi_{south} = 360^\circ \Delta f_{south} \Delta t_{step}, \quad (5)$$

where

$$\Delta f_{south} = \frac{FREF}{2^{24}} (WA - WB) \quad (6)$$

$$\Delta t_{step} = \frac{N}{FREF}, \quad (7)$$

N is the number of reference cycles, WA is fractional-N control word A, WB is fractional-N control word B, $FREF$ is the frequency of the reference clock, and Δt_{step} is the duration of the frequency step Δf_{south} . Substitution of (6) and (7) into (5) yields

$$\Delta\phi_{south} = \frac{360^\circ N (WA - WB)}{2^{24}}. \quad (8)$$

Figure 3 shows the timing diagram used to program the desired phase step.

III. EXPERIMENTAL RESULTS

Figures 4 and 5 show the simulated and measured phase shift step versus expected, based on (8), compared to predicted values at a constant VCO output of 2.45 GHz and 3.2 GHz, postdivided to 50 MHz and 400

Fig. 3. Timing diagram for both the north and south PLLs to demonstrate millidegree phase steps.

MHz, respectively, in order to obtain measurable data as discussed above. In addition to simulated, measured, and predicted values, Figs. 4 and 5 show a regression line that demonstrates the possible theoretical phase step of the PLL phase shifter beyond the noise floors of the simulation and measurement setups. Both measured and simulated data discontinue at the beginning of the regression line as at that point both are at their respective noise floors. The regression line terminates at the theoretical limit imposed by (1) that assumes a programming time no greater than $\frac{1}{F_{REF}}$. Strong agreement can be seen between simulated, measured, and expected values up to the noise floors of the simulation and measurement setups.

Fig. 4. Logarithmic plot of the simulated and measured phase shift versus expected compared to predicted values at a constant postdivided output frequency of 50 MHz. A regression line has been added that shows the theoretical ability of the PLL phase shifter.

Fig. 5. Logarithmic plot of the simulated and measured phase shift versus expected compared to predicted values at a constant postdivided output frequency of 400 MHz. A regression line has been added that shows the theoretical ability of the PLL phase shifter.

IV. CONCLUSION

A fractional-N delta-sigma PLL phase shifter was presented that is capable of phase shift steps in millidegrees at RF and microwave frequencies. Simple calculations revealed the theoretical phase step of the PLL phase shifter to be approximately 21 microdegrees when using a 24 bit fractional modulator, but is difficult to measure due to noise floor limitations at microwave frequencies. Simulated and measured results matched well with predicted responses up to the noise floors of the simulation and measurement setups and demonstrated a best case measured phase step of 21 millidegrees at 50 MHz.

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