# A 9-bit 2.9 GHz Direct Digital Synthesizer MMIC with Direct Digital Frequency and Phase Modulations

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***Abstract*—This paper presents a low power, high speed SiGe DDS MMIC with 9-bit phase and 7-bit amplitude resolutions. This DDS MMIC is the first reported GHz range output DDS with direct digital frequency and phase modulation capabilities. Using more than eight thousand transistors, the DDS MMIC includes a 9-bit CLA accumulator for phase accumulation, a 9-bit CLA adder for phase modulation and a 7-bit sine-weighted DAC. The core area of the DDS occupies 1.7×2.0 mm$^2$. The DDS consumes low power of 2.0 W under a 3.3 V single power supply even with the added modulation blocks. The narrow band spurious-free-dynamic range (SFDR) is measured as 35dBc with the maximum update frequency of 2.9 GHz. The DDS MMIC is packaged and tested in an LCC-44 cavity.**

***Index Terms*—accumulator, carry look ahead (CLA), digital-to-analog converter (DAC), direct digital synthesizer (DDS), Sine-weighted DAC, ROM-less DDS, frequency modulation (FM), phase modulation (PM)**

## I. Introduction

The direct digital synthesizer (DDS) is a key component for the next generation radar and communication systems. Recent developments in radar systems require frequency synthesis with low power consumption, high output frequency, fine frequency resolution, fast channel switching and versatile modulation capability. Linear frequency modulation (FM) (chirp modulation) is widely used in radars to achieve high range resolution, while pulsed phase modulation (PM) can provide anti-jamming capability. With fine frequency resolution, fast channel switching and versatile modulation capabilities, the DDS provides frequency synthesis and direct modulation capabilities that cannot be easily implemented by means of other synthesizer tools such as the analog-based phase-locked loop (PLL) synthesizers. It is difficult for conventional PLL-based frequency synthesizers to meet these requirements due to internal loop delay, low resolution, modulation problems and the limited tuning range of the voltage-controlled oscillator (VCO). The increasing availability of ultra high-speed DACs allows a DDS to operate at mm-wave frequency. However, none of the mm-wave DDS developed so far provides the desired modulation capability [1]–[3]. To achieve very high speed, all the existing DDS MMICs used pipeline accumulators that can work only with a constant input frequency control word (FCW), and thus no frequency modulation can be done [1]–[5]. To implement the direct frequency or phase modulations, carry-look-ahead (CLA) or ripple carry adder (RCA) architectures have to be used with penalty of reduced speed. This DDS MMIC represents the first reported GHz range output DDS with direct digital frequency and phase modulation capabilities. The output gives a larger than 35 dBc narrow band SFDR at maximum update frequency of 2.9 GHz.

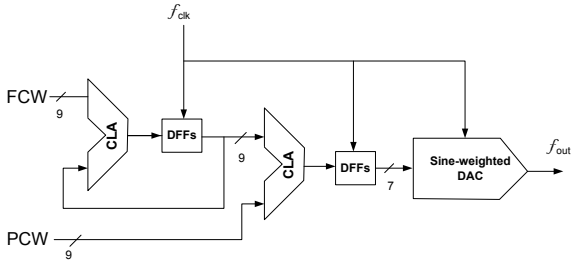


Fig. 1. Block diagram of 9-bit ROM-less DDS.

## II. Circuit Implementation

This DDS adopts a ROM-less architecture which combines both the sine/cosine mapping and digital-to-analog conversion together in a sine-weighted digital-to-analog converter (DAC). The block diagram of the 9-bit 2.9 GHz ROM-less DDS is shown in Fig.1. The major parts of the ROM-less DDS are a 9-bit CLA phase accumulator, a 9-bit CLA full adder and a 7-bit sine-weighted DAC. The 9-bit phase accumulator output modulates with the 9-bit phase control word (PCW) and truncated to 8 bits. After phase modulation and truncation, the highest 8 bit output is fed into the sine-weighted DAC. The two most significant bits (MSB) of the residue are used to determine the quadrant of the sine wave. The MSB output of the phase accumulator is used to provide the proper mirroring of the sine waveform about the $\pi$ phase point. The 2nd MSB is used to invert the remaining 6 bits for the 2nd and 4th quadrants of the sine wave by a 1's complementor, and the outputs of the complementor are applied to the sine-weighted DAC to form a quarter of the sine waveform. Because of the $\pi$ phase point mirroring, the total amplitude resolution of the sine-weighted DAC is 7 bit.

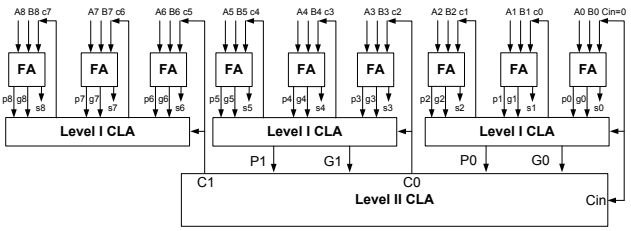


Fig. 2. Block diagram of 9-bit CLA accumulator (full adder).

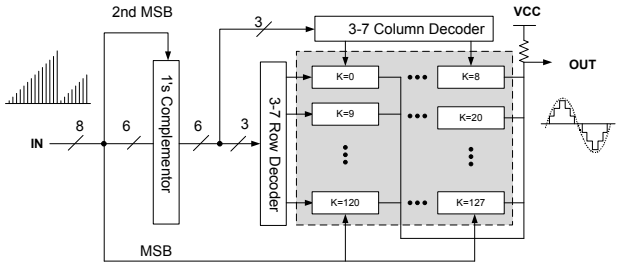


Fig. 3. Block diagram of 7-bit sine-weighted DAC.

### A. 9-bit Carry Look Ahead Adder/Accumulator

To perform a direct digital modulation, the adder must have no latency. Pipelined accumulator is not suitable because of its big latencies and can only handle a fixed FCW. In this design, CLA adder is used to implement the direct digital modulations due to its small delays beyond other zero latency architectures. A 9-bit CLA adder is used to implement the 9-bit accumulator. Fig.2 shows the architecture of the 9-bit CLA adder. The output and carry out for each bit are calculated as

$$\begin{cases} \text{Carry out: } c_i = g_i + p_i \cdot c_{i-1} \\ \text{Sum: } s_i = pi \bigoplus c_{i-1} \end{cases} \tag{1}$$

where $c_i$ is the carry out and $c_{i-1}$ is the carry in or the carry out from the previous bit. $g_i$ and $p_i$ are the carry generate and carry propagate in level I CLA. The first level carry out can be obtained by

$$\begin{cases} c_0 = g_0 + p_0 \cdot C_{in} \\ c_1 = g_1 + p_1 \cdot g_0 + p_1 \cdot p_0 \cdot C_{in} \end{cases} \tag{2}$$

where

$$\begin{cases} \text{Carry generate: } g_i = A_i \cdot B_i \\ \text{Carry propagate: } p_i = A_i \bigoplus B_i \end{cases} \tag{3}$$

and the second level carry out can be obtained by

$$\begin{cases} C_0 = G_0 + P_0 \cdot C_{in} \\ C_1 = G_1 + P_1 \cdot G_0 + P_1 \cdot P_0 \cdot C_{in} \end{cases} \tag{4}$$

where second level propagates are obtained by

$$\begin{cases} P_0 = p_2 \cdot p_1 \cdot p_0 \\ P_1 = p_5 \cdot p_4 \cdot p_3 \end{cases} \tag{5}$$

and second generates are obtained by

$$\begin{cases} G_0 = g_2 + p_2 \cdot g_1 + p_2 \cdot p_1 \cdot g_0 \\ G_1 = g_5 + p_5 \cdot g_4 + p_5 \cdot p_4 \cdot g_3 \end{cases} \tag{6}$$

In the above equations, all the logics must be implemented within less than three inputs. This is selected to compromise with the power supply voltage and CML logics. Under a 3.3 V power supply and a SiGe HBT base-collector voltage of 0.85 V 0.9 V, all the digital logic is implemented using 3 level current mode logic (CML) with differential output swings of 400 mV. Level shifters may be needed to shift between different voltage level inputs. The level shifter usually runs much faster than other CML gates. It can be ignored when counting the gate delays. Suppose XOR gate's delay is two times of the AND gate. The total delays can be calculated from the equations and diagram. (A) two gates delay to calculate level I carry generate $g_i$ and propagate $p_i$ in equation (3); (B) two gate delays to calculate level II carry generate $G_i$ and propagate $P_i$ in equations (5) and (6); (C) two gate delays to calculate level II carry in equation (4); (D) two gate delays to calculate level I carry in equation (2); and (E) two gates delay to calculate sum and carry out from equation (1). Therefore the 9-bit CLA adder needs only 10 AND gates delay, which has a much less delay than the ripple carry adder's (2N-1) = 17 gate delays especially for high resolution adders while it is much slower than the pipelined counterpart.

TABLE I
CURRENT SOURCE MATRIX IN SINE-WEIGHTED DAC

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 2 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| 3 | 3 | 3 | 2 | 3 | 3 | 3 | 2 |
| 3 | 2 | 3 | 2 | 3 | 2 | 2 | 3 |
| 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 1 | 2 | 2 | 1 | 2 | 1 | 1 | 2 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |

### B. 7-bit Sine-weighted DAC

The structure of the sine-weighted DAC is shown in Fig.3. Since the quadrant of the sine waveform was determined by the two MSBs, the left 6 bits are used to control the switch matrix and generate the amplitude for a quarter phase (0 $\pi$/2) sine wave. The current source matrix is calculated by the below equations and shown in Table I.

$$I_k = \begin{cases} \lfloor (2^9 - 1) \sin\left(\frac{\pi}{2} \cdot \frac{(0.5)}{2^6}\right) \rfloor, \text{for } k = 0 \\ \lfloor (2^9 - 1) \sin\left(\frac{\pi}{2} \cdot \frac{(k+0.5)}{2^6} - \sum_{n=0}^{k-1} I_n\right) \rfloor, \ 0 \le k \le 2^6 - 1 \end{cases} \tag{7}$$

The sine-weighted DAC current source matrix provides totally 128 unit current sources. The unit current of each current source is set as 105 $\mu$A. The largest current in the current source is 315 $\mu$A, which is composed of 3 unit current sources.

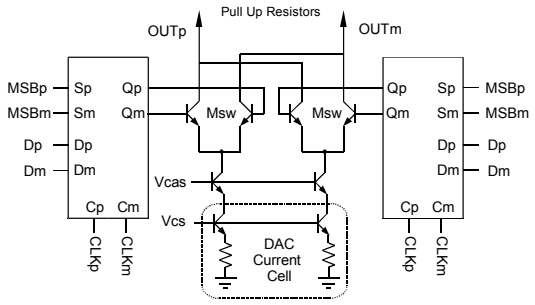


Fig. 4. Diagram of DAC switch and current source matrix cell.

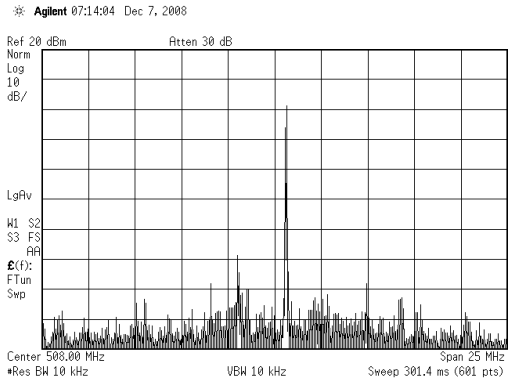


Fig. 5. Measured DDS output spectrum with 509 MHz output under 2.5 GHz clock (FCW=104), showing about 48dBc narrow band SFDR.

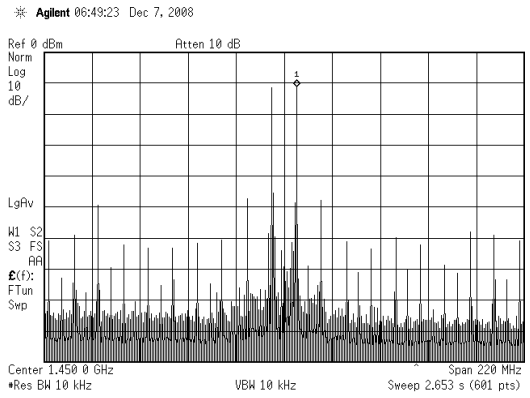


Fig. 6. Measured DDS output spectrum with 1.444 GHz output and 2.9 GHz clock (FCW = 255), showing about 35dBc narrow band SFDR. The image tone is located at 1.455 GHz.

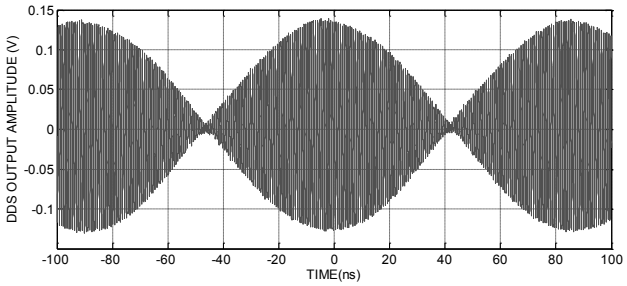


Fig. 7. Measured DDS output waveform with 1.444 GHz output and 2.9 GHz clock (FCW=255). The envelope frequency is 12 MHz

The current switch contains two differential pairs with cascode current sources for better isolation and current mirror accuracy. The current outputs are converted to differential voltages by a pair of off-chip 15 Ω pull-up resistors. Fig.4 shows that the currents from the cascode current sources are fed to outputs $OUT_p$ and $OUT_m$ by pairs of switches ($M_{sw}$). The MSB controls the selection between different half periods. The current switch contains two differential pairs with minimum size transistors and a cascode transistor to isolate the current sources from the switches, which improves the bandwidth of the switching circuits. For the layout, vertical devices SiGe HBTs are used with a degeneration resistor to improve the current source matching. All the current source transistors are randomly distributed in the current source matrix. Two dummy rows and columns have been added around the current source array to avoid edge effects. In order to minimize the phase difference of the clock to the flip-flops, an H-tree clock scheme is used to make the clock signal reach each block simultaneously in both the adder/accumulator and DAC.

## III. Experiment Results

Figs.5-7 illustrate the measured DDS output spectra and waveforms for different output and clock frequencies without modulations. Fig.5 presents a 509 MHz DDS output with a 2.5 GHz clock input, with the FCW equals to 104. The measured output power is approximately 0 dBm and the measured narrow band SFDR is approximately 48 dBc. Fig.6 gives the measured DDS output spectrum with 1.444 GHz Nyquist output under 2.9 GHz clock. Since $FCW = 2^8 - 1 = 255$, the output frequency is

$$\frac{FCW}{2^N} \times f_{clk} = \frac{255}{2^9} \times 2.9\ GHz = 1.444\ GHz$$

The first order image tone mixed by the clock frequency and the DDS output frequency occurs at

$$2.9\ GHz - 1.444\ GHz = 1.456\ GHz$$

Fig.7 shows the time domain waveform of Fig.6. The envelope frequency of the waveform is

$$\frac{2^{9+1}}{2^9} \times f_{clk} - \frac{2^{9-1}}{2^9} \times f_{clk} \approx 12\ MHz$$

Fig.8 shows the measured DDS output with FCW = 2 frequency modulated by a step of ΔFCW = 1. The frequency before the step is 9.375 MHz with FCW = 2 and after the step is 14.0625 MHz with FCW = 3. Fig.9 shows the measured DDS output with FCW = 2 phase modulated by a step of ΔPCW=256 with respect to 180° phase shift. The output frequency is 10 MHz with a 2.5GHz clock.

All measurements were done in LCC-44 packaged parts without deglitch filter or calibrating the losses of the cables and PCB tracks.

Table II compares mm-wave DDS MMIC performances. Although this DDS have a relatively low frequency than others, it is the first DDS with direct digital frequency and

TABLE II
MM-WAVE DDS MMIC PERFORMANCE COMPARISION

| Technology $f_T/f_{max}$ [GHz] | InP 137/267 [1] | InP 300/300 [2] | InP 300/300 [3] | SiGe 100/120 [4] | SiGe 200/250 [5] | SiGe 200/250 [this work] |
|---|---|---|---|---|---|---|
| Phase resolution [bit] | 8 | 8 | 8 | 9 | 11 | 9 |
| Amplitude resolution [bit] | 7 | 7 | 5 | 8 | 10 | 7 |
| Frequency modulation [bit] | None | None | None | None | None | 9 |
| Phase modulation [bit] | None | None | None | None | None | 9 |
| Max clock [GHz] | 9.2 | 13 | 32 | 9.6 | 8.6 | 2.9 |
| SFDR [dBc] | 30 | 26.67 | 21.56 | 30 | 40 | 35 (narrow) |
| Power consumption [W] | 15 | 5.42 | 9.45 | 1.9 | 4.8 | 2.0 |
| Die area [$mm^2$] | 8.0 × 5.0 | 2.7 × 1.45 | 2.7 × 1.45 | 3.0 × 3.0 | 4.0 × 3.5 | 2.5 × 3.0 |

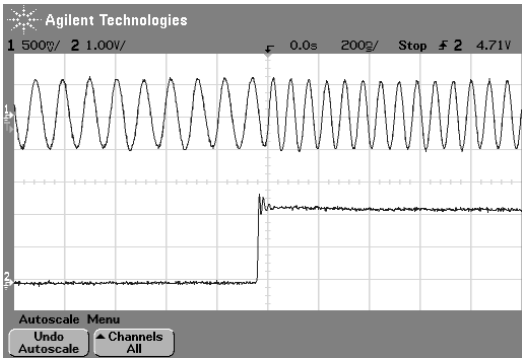


Fig. 8. Measured DDS output with FCW = 2 frequency modulated by a frequency step of ΔFCW = 1. The frequency before the step is 9.375 MHz with FCW = 2, after the step is 14.062 MHz with FCW=3.

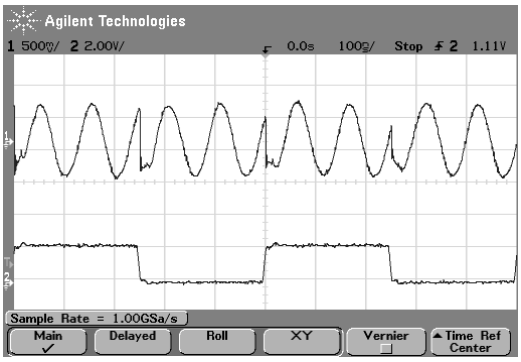


Fig. 9. Measured DDS output with FCW = 2 phase modulated by a phase step of ΔPCW = 256 with respect to 180° phase shift. The output frequency is 10 MHz with a 2.5 GHz clock.

phase modulation capabilities and has more than GHz output frequency. Some commercial parts have the FM and PM capabilities, but all the parts work no more than 1 GHz and can only output less than 500 MHz frequency. The die photo of the SiGe DDS MMIC is shown in Fig.10. This DDS design is quite compact with an active area of 1.7×2.0 mm$^2$ and a total die area of 2.5×3.0 mm$^2$.

## IV. CONCLUSION

Implemented in a 0.13 $\mu$m SiGe BiCMOS technology with $f_T/f_{max}$ of 200/250 GHz, this paper presented a 9-bit 2.9 GHz SiGe DDS MMIC design with direct digital 9-bit frequency and 9-bit phase modulations. With Nyquist output, the

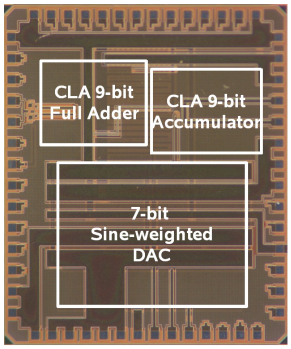


Fig. 10. Die photo of the direct digital modulation DDS.

DDS achieves a maximum clock frequency of 2.9 GHz, and a narrow band SFDR of 35 dBc. It has low power consumption as well. The power consumption is approximately 2.0 W under a single 3.3 V power supply even with added modulation blocks. This DDS MMIC is the first reported GHz range output DDS with direct digital frequency and phase modulation capabilities.

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