A CMOS Current-Mode Full-Adder Cell for Multi-Valued Logic VLSI

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Abstract

This paper describes the design and implementation of a carry save adder cell for multi-valued logic (modulo 4) VLSI using the HAMLET CAD tool [1]. A VLSI test and evaluation integrated circuit was implemented with MAGIC, simulated using SPICE, and fabricated through the MOSIS service. Engineering modifications to the original current-mode inverter cells used by HAMLET were made leading to significant power savings in a complete design. The fabricated device performed as predicted by SPICE simulation.

I. INTRODUCTION

In recent years, continued improvements in VLSI fabrication processes have led to a renewed interest in current-mode CMOS high-radix arithmetic circuits. Of particular importance is the development of high speed compact multiplier circuits for the rapidly expanding fields of digital signal processing and digital control systems. In most modern high-speed arithmetic units, multiplication of long data words is performed by simultaneously generating sets of partial products and then summing them together with a network of carry save adders (CSAs) in an operation that is referred to as "row reduction." Scalability difficulties of CSA networks can be overcome by utilizing a high-radix signed number system to significantly reduce the number of transistors required for the addition of large data-words.

II. DESIGN OF MODULO 4 ADDER CELL

At the core of the current-mode circuits required to implement an MVL expression is a CMOS inverter with a **current** input.

Figure 1: CMOS Inverter With Current Input

In Figure 1, The nFET device M0 operates in saturation because $V_{DS} = V_{GS}$ and $V_{DS} > V_T$. Ignoring the

Early voltage and bulk effects which are minimal, the saturation value of the drain current is given by:

$$I_D = 1/2 \mu_n C_{ox} (W/L) (V_{GS} - V_T)^2 \quad (1)$$

Since the drain current I_D is the input current, then the operating point at which the nMOS device M0 becomes saturated is found by:

$$I_{SW} = C(V_{SW} - V_T)^2 (W/L) \quad (2)$$

I_{SW} and V_{SW} refer to the "switching" current and switching voltage respectively. The basic cells used to implement the current mode logic consist of the current-input CMOS inverter with the output connected to a single nMOS or pMOS transistor (Figure 1). The step-down generator produces a constant I_{out} when the input current is less than the switching current, else 0. The step-up generator has an output current I_{out} of 0 unless the input current is greater than I_{SW} .

Figure 2: Step Down Function Generator

Figure 3: Step Up Function Generator

Figure 4: Transfer Curves for Function Generators

The column output generator is actually a step down function generator in which the geometry of the nMOS transistor M3 is proportioned to produce the desired output current for its term. The output currents from various step up and step down generators are connected to the input of the column

generator, which in turn generates its output value only when the input current is 0.

HAMLET - A CAD Tool for MVL Design

Unlike binary logic design, MVL of radix greater than 2 quickly becomes difficult to conceptualize. The MVL CAD tool HAMLET uses a sum-of-products (SOP) expression as formatted input[1]. Since HAMLET will minimize the SOP expression, any valid SOP expression which completely describes the functionality of the design is sufficient. Recalling for the full adder:

$$\text{SUM}(C_i X_i Y_i) = C_i (\text{XOR}) X_i (\text{XOR}) Y_i \quad (3)$$

By utilizing a mapping technique which resembles the familiar Karnaugh Map method, the SUM and CARRY functions for the carry save adder in radix 4 are completely described by tables 1 and 2.

Minimization of Literals Using HAMLET Heuristics

Once the file containing the required SOP terms was input into the HAMLET CAD tool, Simulated Annealing minimization was used, reducing the Sum function from 48 to 32 terms, and the Carry function from 17 to 15 required terms. Table 3 shows the reduced SOP expressions returned by HAMLET which were utilized to implement the modulo-four adder.

Table 1: Mapping for Sum Function

Figure 5: Current Logic Levels (µA)

To achieve these characteristics, three components are required. The step-up and step-down generators supply the appropriate currents to the column output generator[3]. Together, these components form one minterm of the logic equation.

Table 2: Mapping for Carry Function

Table 3: Sum and Carry Function Terms, Respectively

1 * x1(3,3) * x2(0,1) * x3(3,3)
+ 1 * x1(3,3) * x2(0,2) * x3(2,2)
+ 2 * x1(0,1) * x2(0,0) * x3(2,3)
+ 1 * x1(2,3) * x2(3,3) * x3(0,0)
+ 1 * x1(1,1) * x2(0,0) * x3(0,3)
+ 2 * x1(0,0) * x2(2,2) * x3(1,1)
+ 1 * x1(2,3) * x2(1,2) * x3(2,3)
+ 1 * x1(1,3) * x2(3,3) * x3(1,1)
+ 1 * x1(2,3) * x2(0,1) * x3(3,3)
+ 3 * x1(0,0) * x2(1,1) * x3(2,2)
+ 8 * x1(2,2) * x2(2,2) * x3(3,3)
+ 1 * x1(0,1) * x2(2,2) * x3(3,3)
+ 3 * x1(3,3) * x2(0,0) * x3(0,0)
+ 3 * x1(2,2) * x2(0,0) * x3(1,1)
+ 1 * x1(0,0) * x2(2,3) * x3(0,0)
+ 1 * x1(3,3) * x2(2,3) * x3(1,1)
+ 1 * x1(2,3) * x2(2,3) * x3(3,3)
+ 1 * x1(1,1) * x2(0,1) * x3(3,3)
+ 1 * x1(0,2) * x2(2,3) * x3(1,2)
+ 1 * x1(3,3) * x2(3,3) * x3(2,2)
+ 1 * x1(1,2) * x2(3,3) * x3(0,0)
+ 1 * x1(3,3) * x2(0,3) * x3(1,3)
+ 1 * x1(2,2) * x2(2,2) * x3(0,1)
+ 1 * x1(1,1) * x2(0,1) * x3(3,3)
+ 1 * x1(2,3) * x2(2,3) * x3(3,3)
+ 1 * x1(0,2) * x2(3,3) * x3(1,1)
+ 1 * x1(3,3) * x2(2,3) * x3(2,2)
+ 1 * x1(1,2) * x2(3,3) * x3(0,0)
+ 1 * x1(1,1) * x2(1,1) * x3(2,2)
+ 1 * x1(1,3) * x2(2,3) * x3(3,3)
+ 1 * x1(2,2) * x2(3,3) * x3(3,3)

III. IMPLEMENTATION

To implement the MVL expression, different values of current correspond to the four different logic levels. A serious drawback to this implementation is that it requires current to be constantly flowing in the

The column output generator outputs a current of predetermined value if there is no current flow at its input. This input is the wired-OR of the step-up and step-down generators. The predetermined value will be one of the designed logic levels. This value is set by the gate dimensions of the output transistor. Note that the column output generator is insensitive to the value of the input current when it is present, i.e. it does not produce an output if the input is not zero. There is one column output generator per minterm.

In order to improve the implementation of the MVL expression design, several engineering changes

were made to the basic cells used by HAMLET and implemented in a custom layout of the final device.

Minimum wire width is reduced from 4 μ m to 2 μ m with a λ of 1.0 μ m, allowing better precision in control of threshold detector values and column output generator current levels. In order to reduce power requirements for this design and improve noise margin performance, the logic value thresholds and the ideal current values produced by the step-up and step-down generators were redesigned as follows:

Table 4: New Logic and Threshold Current Design Values

Logic Values	Original HAMLET Design Values:			
	Step Down Generator	Ideal Current	Current Generator	Step Up Generator
0	0 μ A	0 μ A	*	10 μ A
1	20 μ A	50 μ A	58 μ A	60 μ A
2	80 μ A	100 μ A	100 μ A	110 μ A
3	130 μ A	150 μ A	136 μ A	not defined
	New Design Values:			
	Step Down Generator	Ideal Current	Current Generator	Step Up Generator
0	0 μ A	0 μ A	*	20 μ A
1	20 μ A	40 μ A	40 μ A	60 μ A
2	60 μ A	80 μ A	80 μ A	100 μ A
3	100 μ A	120 μ A	120 μ A	150 μ A

A substantial power savings was also realized by reducing the current output from the step up and step down cells. The column output generators require much less current for switching purposes than in the original HAMLET design. Table 5 summarizes the redesign of the step up/down generator output current levels

Table 5: New Step-Up and Step Down Generator Output Current Design

Output Currents From Step Up/Down Generators:		
	Step Up Generator	Step Down Generator
Original Cells	180 μ A	240 μ A
New Cell Design	60 μ A	70 μ A

The individual circuits were implemented using MAGIC and then extracted to SPICE for simulation and analysis. For this circuit, the noise margin can be defined as the difference between the output logic level and the input switching thresholds of the next gate. The optimum noise margin can be achieved only by centering the output logic value between its associated switching thresholds. These nominal current values have been achieved within 2 μ A. Propagation delays and power consumption models are as follows:

Table 6: Timing and Power Simulation of Cells.

	Step Up Generator	Step Down Generator	Column Output Generator
T_r (ns)	4.19	1.43	1.23
T_f (ns)	2.04	3.12	1.51
T_{PLH} (ns)	11.48	4.29	2.16
T_{PHL} (ns)	2.74	9.61	5.69
P_{STATIC} (mW)	1.78(H)/0.0L	1.07	0.42(H)/0.81(L)
$P_{LH(peak)}$ (mW)	1.78	1.34	0.87
$P_{PHL(peak)}$ (mW)	1.78	2.25	1.60

The power dissipation for this circuit is expectedly high because the proper operation of this type of

multi-valued logic circuit requires continuous current flow. Unlike conventional CMOS logic, the static power dissipation is much greater than the transistor leakage current.

The components were combined to yield a fairly typical minterm for analysis. The minterm chosen was:

$$3 X(2,2) Y(3,3) C(2,2) \quad (4)$$

This term was implemented in MAGIC and extracted to SPICE for simulation and analysis. The results are compiled in the following table:

Table 7: Term 3 X(2,2) Y(3,3) C(2,2)

T_r (ns)	4.19
T_f (ns)	2.04
T_{PLH} (ns)	11.48
T_{PHL} (ns)	2.74
P_{STATIC} (mW)	1.78(H)/0.0L
$P_{LH(peak)}$ (mW)	1.78
$P_{PHL(peak)}$ (mW)	1.78

The propagation delays are a result of the series connection of the step generators and the column output generator. In this configuration, there are a total of 4 CMOS inverter stages that a signal must propagate through prior to the generator output transistor. The static power dissipation is fairly significant, while the dynamic power is of much lower value.

Circuit Layout

The circuit was laid out using MAGIC for a MOSIS 2.0 micron process, using n-well process data from Orbit fabrication facility.

The basic floor plan of the chip consists of 2 "towers" wired together at the output to realize the truncated sum function, a single tower for the carry out function, and a set of current mirrors to replicate the inputs that are required for each term. The cell has 3 input and 2 output pads, as well as separate power and ground inputs for the sum function towers (2), carry function, and current mirror cell, respectively. The sum output is composed of 47 minterms, while the carry is composed of 17 minterms. The final layout for this device is shown in Figure 6.

Input Current Mirror Design and Layout

Each of these terms, in general, requires all three input current signals. A current mirror was designed to provide for these input requirements. We centered the current replicator design at 80 μ A because of the nonlinear nature of the current mirror circuit with a varying current reference. This results in less than a 10 μ A deviation from the desired current at the other logic levels.

Figure 6: Final Layout of Design

VDD and Ground Rail Considerations

Power consumption was also a major design consideration, as discussed earlier. Care must be exercised to ensure that the circuit will not fail due to electromigration problems associated with excess current within the interconnect network. In addition, to separate power and ground rails for each tower and the current mirror unit, metal 2 was used which has a nominal rating of 1 mA/ μm of width. As can be observed in the power plot of Figure 7, at no point does the current exceed 30mA on any rail. These measurements were recorded during the functional test. These values are relatively high, but do not pose a threat to the circuit.

Figure 7: Current Measurements at VDD and Ground Rails

Finally, there are transients in the output due to the nature of the circuit. The various minterms turn "on" and "off" at different times depending on the current levels at their inputs. This results in transients while the circuit is stabilizing between input changes. Provided the transients do not exceed power ratings (as previously shown) and the output is sampled once it has stabilized, these hazards will not affect the circuit operation. The time delay for transients to subside can be included in the delay of the adder.

Simulation of Completed Chip Design

A series of square current waveforms were applied at each input in order to simulate all combinations possible. The SPICE model produced output demonstrating the correct counting sequence at the output nodes for all input combinations.

IV. SUMMARY OF TEST RESULTS

This section summarizes the performance characteristics and functionality of the multiple-valued logic (modulo four) carry save adder designed and implemented in current mode CMOS. A total of 15 devices were returned from fabrication, 12 of which were mounted in appropriate packages. Four devices from the lot were completely tested (dev1 - dev4). In order to readily test these devices, a custom testbench was designed and constructed.

Static Power Tests

Static power test results for no-load and full-load conditions were found to be slightly higher than those obtained from SPICE simulation of the layout. The following table shows the power consumption of the major components of the third device in the test lot:

Table 8: Component Static Power

MVL_adder Device 3		
	Design No Load	Measured No Load
Sum (right tower)	2.93mA	3.12mA
Sum (left tower)	2.88mA	3.02mA
Carry out tower	2.95mA	3.23mA
Current mirror	0	0.0mA
Pad ring	0	0.0mA

The four test devices were measured under no load conditions (all inputs set to 0uA). As VDD was ramped from 0 to 5.0v, the power supply current was recorded. The static power consumption was calculated by finding an average current for the four devices and then multiplying by a constant VDD of 5.0v.

$$I_{ave} = (I_{dev1} + I_{dev2} + I_{dev3} + I_{dev4}) / 4 \quad (5)$$

$$P_{ave} = I_{ave} * VDD \quad (6)$$

The resulting average static power under no load conditions is plotted as a function of VDD along side the simulation obtained from SPICE in Figure 8.

Figure 8: Measured and SPICE Simulation of No Load Static Power Consumption

For full load testing, all inputs were held high (120 μA each) and VDD was set to 5.0v. Once again, the power supply current was recorded for each test device. The measured values are shown compared with the full power simulation obtained from the SPICE model in Table 9.

The highest current level at the outputs occurs when the sum output transitions from a logic 2 to a logic 3, and vice versa. The measured value was determined by using a ramped current input from 0 to 150 μ A and observing the transitions at the sum terminal. A transient current spike of 195 μ A was recorded. This effect was seen for transitions in both directions. This transient result correlates with the

Table 9: Full Power Measurements

MVL_adder Fab ID: N46EFF1			Spice Model (VDD set 5.0v)	
	Measure d Current	Calculat ed Power	VDD Current	VDD Power
Device 1	70.5mA	352.5m W	66mA	330mW
Device 2	69.3mA	346.5m W		
Device 3	70.2mA	351.0m W		
Device 4	69.3mA	346.5m W		

SPICE model which showed similar transients of 195 μ A for these transitions. This result translates into a peak power rating for the device of 353.63mW, assuming all three inputs experience a simultaneous transition from logic 2 to logic 3.

Functional Testing

Steady-state functional values for output currents were within 1.5% of design, and most were found to be significantly less than 1.0%. Exhaustive functional logic testing was conducted (64 input combinations), and no deviation from predicted output values was observed in steady-state. Table 10 is a sample set from the input test on a sample test IC.

Design delays were predicted using the extracted SPICE model of the adder. Customized pulsed current waveforms were provided to the input nodes. The output waveforms for the sum and carry out were obtained with a 1Kohm resistive load. This was done in order to gain a quantitative result which could be compared to the measured values.

Results Discussion

Steady-state functional operation conformed very closely to design and simulation. Output currents were on average within 1 percent of ideal operation for Vdd set to 5.0v. This is important due to the fact that these devices are designed to operate in both parallel (carry save) and serial (ripple) adder configurations. Static power consumption for no load, full load, and peak power were very close to design values.

Table 10: Sample IC Functional Test Results

[Xin, Yin, Cin]	Sum Output		Carry Output	
	design (mA)	measured	design (mA)	measured
[1,1,0]	80	82.2	0	0
[2,1,0]	120	119.3	0	0
[1,3,0]	0	0	40	41.3
[2,0,1]	120	119.7	0	0
[2,1,2]	40	41.2	40	40.3
[3,0,1]	0	0	40	40.9
[3,2,1]	80	80.9	40	40.0
[0,3,2]	40	40.3	40	40.3
[3,3,2]	0	0	80	79.2
[0,2,2]	0	0	40	40.2

Table 11: Propagation Delay

	Sum 0->3->0		Carry 0->1->0	
	measured	SPICE	measured	SPICE
t _r	280nS	60nS	223nS	10nS
t _f	254nS	110nS	215nS	10nS
t _{dr}	135nS	90nS	170nS	120nS
t _{df}	120nS	55nS	73nS	40nS

V. CONCLUSIONS

HAMLET was successfully utilized in the design phase of a radix-4 adder cell. Minimization heuristics correctly produced a set of sum-of-product expressions for the sum and the carry out function, which, when implemented and tested, correctly computed the desired functions.

VI. REFERENCES

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