SURVEY OF THE STATE OF THE ART
OF ELECTRICAL TRANSIENT UPSET IN DIGITAL CIRCUITS

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Abstract

A survey was conducted to assess the present upset technology status. Upset is defined as the malfunction of a circuit or system due to interference. This paper focuses on the malfunction of digital circuits due to electrical transients that cause nonpermanent undesirable logic states which show up in the output as errors. As integrated circuits are being made more dense, their susceptibility to upset is increasing. Thus, upset, which may be induced at far lower levels than damage, demands attention. Knowledge voids that were identified in this investigation of upset must be resolved. Although this survey concentrates on upset due to the electromagnetic pulse (EMP) type of transients, in the process it sorts through other types of upset as they relate to it. The survey results increase the need for a basic upset test which should lead to a systematic characterization of upset due to EMP. The test results should be fundamental building blocks in the computer modeling of circuit response to transient drivers, in addition to aiding in the prediction of the stochastic response of systems to known transients.

Summary

The susceptibility of circuits, analog and digital, to upset demands greater attention as integrated circuits (IC's) are made more dense, circuit components become smaller, and upset levels become increasingly lower. Integrated chips may now be an entire subsystem, and the susceptibility to upset may accordingly be more severe. A review of the literature was carried out in order to determine the present status of the upset technology, and to find studies on upset due to EMP. Information given here was drawn from 61 references, not listed because of space limitations. The literature survey touched upon several other areas, including an analysis of impulsive noise and upset due to ionizing radiation, a probabilistic approach to electromagnetic compatibility (EMC), an analysis of upset due to radio frequency interference (RFI) (both computer modeling and experimentation), and an analysis of computer systems. It became evident that the issue of upset has not yet received its proper attention. Techniques used in these different areas can combine to provide building blocks for a thorough analysis of upset.

The earlier investigations of digital circuit upset dealt with noise and data transmission. It was realized that impulsive noise, as well as Gaussian noise, needed to be accounted for in the calculation of bit error rate. Statistical models of the impulsive noise were derived [1], some of

which were experimentally verified. These results may be of interest since EMP can be modeled as impulsive noise.

Another bulk of literature describes the effects (including upset) of ionizing radiation (e.g., gamma rays, protons, neutrons) on digital systems. A major concern has been the susceptibility of space vehicles with their increasing digital complexity. A variety of experiments including the use of ion microbeams to investigate soft errors and single-event upsets have been performed. An article of interest [2] described a portable test system for upset testing of very large scale integrated (VLSI) circuits exposed to pulsed radiation. The outputs of a device under test (DUT) and a reference device were compared. Two criteria, the logic error and the voltage level error, were used to determine upset. The experimental approach of comparing the outputs of disturbed and undisturbed digital circuits is a powerful approach for future upset tests.

In recent years, a few articles [3, 4] have suggested a probabilistic approach for predicting upset of large complex systems, reasoning that a deterministic approach is inappropriate for the complexities of larger systems. The randomness associated with parameters in electromagnetic susceptibility (EMS) problems causes statistical analysis to be more accurate than deterministic "worst case" predictions. A methodology incorporating fault trees to arrive upon a figure of merit or compatibility factor is being developed. This methodology, when developed, may also be applicable to the analysis of circuit upset due to EMP.

Computer-aided circuit analysis techniques [5], especially device modeling, were frequently discussed in the literature. For example, the Modified Ebers-Moll model and SPICE, the most widely used program, were employed to study upset due to RFI. These models have fewer limitations and are more appropriate than the other available transistor models. Upset, such as change of output logic or propagation delay, was observed over a range of frequencies and amplitudes. While the conversion of RFI to bias shift is not relevant to EMP, the way in which the induced bias shift is analyzed is relevant.

The survey results revealed an equal interest in the empirical measurement of RFI effects. The largest project [6], done by McDonnell Douglas under contract to the United States Naval Surface Weapons Center (NSWC) at Dahlgren, developed a technology base of IC susceptibility to microwave signals. The results of a massive amount of computer-aided testing on such IC's as transistor-

transistor logic (TTL) and complementary metal-oxide-semiconductor (CMOS) digital circuits were supplemented by computer modeling results. The data were condensed into graphs, showing the RF and microwave power susceptibility levels. In the instance of pulsed RF, the probability of the bit error increased because of such factors as the clock rate, pulse width, pulse repetition frequency, and the flow of information processed by the device.

As part of the Defense Nuclear Agency (DNA) sponsored "Apache" Program, transient high-altitude EMP (HEMP) effects on common computer systems employed in the Pacific Command (PACOM) were analyzed [7]. The assessment approach involved dividing the computer system into "functional units," including the teletype, central processor, etc. These units were then associated with their major states, for example "read" or "write" states. Once the major states were defined, the functional units were experimentally tested, with the use of appropriate software to run them through their major states. The assessment results revealed (a) the existence of a sharp transition from a state of low probability of error to a state of high probability of error, (b) logic state upsets occurred at very low current levels, and (c) system level upsets occurred with very high probabilities. These test results allowed a better understanding of functional units and their errors, enabling one to develop hardware and/or software to help guard against the event of EMP-induced upset.

In the early 1970's, several reports [8-10] were published on upset of integrated circuits. There was an effort to define and analyze upset in different types of IC's. However, a unified, systematic analysis approach was not developed. In addition to component testing, methods were developed at the Air Force Weapons Laboratory for testing mission-critical and system-critical subassemblies with the use of software to simulate "in system" conditions. However, this process is complex, for each system and subsystem is very different, but the procedure is presently being optimized and standardized.

Conclusions

In conclusion, the issue of EMP-induced upset has not been thoroughly investigated. Although the knowledge of the subject is sketchy, the assessment techniques employed in the related areas should combine to provide building blocks for a comprehensive analysis. The results of this survey indicate a need for a basic upset test methodology which should lead to a systematic characterization of upset. The test data should serve as fundamental building blocks for the computer modeling of circuits to predict their response and the stochastic response of systems to known transients.

Currently at Harry Diamond Laboratories, a test methodology for measuring the upset of IC's is being developed. The methodology is being built from the response of one of the most basic and fundamental units, the shift register. The idea is to build a strong foundation which permits thorough investigation of the more complex units. With successful screening of the more

susceptible devices, results could be used in the design stage of less susceptible systems. The annotated bibliography on which this summary is based will be available to interested attendees.

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