Digital Beamforming Developments for the Joint NASA/Air Force Space Based Radar

Mark A. Fischman and Charles Le

Radar Science and Engineering Section

Jet Propulsion Laboratory, California Institute of Technology

Pasadena, CA 91109 USA

e-mail: mafisch@jpl.nasa.gov

Abstract—The Space Based Radar (SBR) program includes a joint technology demonstration between NASA and the Air Force to design a low-earth orbiting, 2×50 m L-band (1.26 GHz) radar system for Earth science and intelligence-related observations. A key subsystem aboard SBR is the electronically-steerable digital beamformer (DBF) network that interfaces between 32 smaller sub-antenna panels in the array and the on-board processing electronics for Synthetic Aperture Radar (SAR) and Moving Target Indication (MTI). In this paper, we describe the development of a field-programmable gate array (FPGA) based DBF processor for handling the computationally intensive inner-product operations for wideband, coherent beamforming across the 50 m length of the array. The core functions of the DBF—the CORDIC (Coordinate Rotation Digital Computer) phase shifters and combiners—have been designed in the Verilog HDL (hardware description language) and implemented onto a high-density Xilinx Virtex II FPGA. This design achieves real-time processing at an input data rate of 25.6 Gbit/s. Tests with an antenna array simulator demonstrate that the beamformer performance metrics (0.07° rms phase precision per channel, -35.2 dB peak sidelobe level) will meet the system-level requirements for SAR and MTI operating modes.

I. INTRODUCTION

Research groups from NASA and the Air Force are currently collaborating on the design of a very large aperture, 2×50 m L-band (1.26 GHz) Space Based Radar (SBR) as a joint technology demonstration for Earth science and defense-related applications. The SBR baseline mission requirements call for a low-Earth orbiting, electronically-steerable phased-array radar with multiple processing modes for Synthetic Aperture Radar (SAR), Interferometric SAR (InSAR), and Moving Target Indication (MTI). In terms of Earth science goals, the capability to make global SAR and InSAR observations at L-band frequencies would enable centimeter-precision geodetic imaging (for land surface topography and earthquake hazard forecasting) and measurements of other parameters that are crucial to understanding the Earth's water cycle and energy balance (soil moisture, vegetation height and biomass, sea ice velocity and thickness) [1], [2].

A key subsystem in SBR is the beamforming network that interfaces between 32 smaller sub-antenna panels (each 1.56×2 m) and the SAR on-board processing electronics. In missions that preceded SBR such as the Spaceborne Imaging

Radar-C/X-band Synthetic Aperture Radar (SIR-C/X-SAR) flown in 1994 [3] and the Shuttle Radar Topography Mapper (SRTM) flown in 2000 [4], beamforming was carried out in the RF electronics using corporate-fed microwave phase-shifters and combining networks that extended over the entire antenna length. RF combining was a suitable technology for these past radar missions because the antenna apertures were smaller (≤ 12 m), the system bandwidth was relatively low (≤ 20 MHz), and the radars were mainly operated in a fixed-azimuth (boresight) steering mode.

The recent development of very large aperture spaceborne radar systems such as SBR, combined with wide bandwidth and beam steering requirements, has introduced new technical challenges. In addition to the 50 m antenna length, SBR also has a significantly wider bandwidth of 80 MHz and must be electronically steerable up to $\pm 45^\circ$ in azimuth. Microwave phase-shifters are by themselves not sufficient for coherent beamforming because the time lag of the radar echo's wavefront across the array is much greater than the correlation length of the wideband echo. Also due to the large antenna structure, the radar is susceptible to thermal gradients across the antenna mast which can significantly degrade phase stability in orbit. The challenge becomes how to combine the wideband echoes from each antenna panel while maintaining signal coherence and phase stability across the array length.

In this paper, we present the development of a highly phase-stable digital beamformer (DBF) system for SBR, facilitated by field-programmable gate array (FPGA) technology. The DBF concept is to move the analog-to-digital conversion stage of the radar receiver further up in the signal chain—in the case of SBR, to the antenna panel level. Multiple digitized phase-center data from the 32 panels are then sent via high-speed fiber-optic links to a centralized, FPGA-based DBF processor, where the beam steering operations are performed in digital electronics. A time-domain processing technique is used in the FPGA design to achieve real-time operation for on-board processing of SAR science data.

II. BEAMFORMING APPROACH

A functional diagram of the SBR beamforming system is shown in Fig. 1. The DBF must phase rotate and coherently sum the return signals from all elements of the array at azimuth scan angles up to $\pm 28^\circ$ in spotlight SAR mode or $\pm 45^\circ$ in MTI mode. Because of the large array size and wideband operation, true time delay (TTD) devices are needed to focus the wavefront energy and achieve correlation between antenna panels. SBR uses a hybrid approach (a combination of TTDs and phase-shifters) which comprises the following components: 1) 6-bit RF phase shifters at each of the 12×12 antenna elements in a panel, 2) microwave

Fig. 1. Functional diagram of the Space Based Radar's digital beamformer (DBF) system.

analog TTDs integrated into each panel, with a fine time step resolution of $t_d = 0.25$ ns, 3) digital TTDs which are effected in first-in/first-out memory after each panel's A/D conversion stage, with a coarse time resolution of 5 ns (200 MHz A/D sampling), and 4) digital phase shift correction on the 32 data channels arriving at the DBF processor.

The received offset video signals from the 32 antenna panels are each A/D converted at a nominal 8-bit resolution, decimated to a sampling rate of 100 MSPS, and sent via an OC-48 fiber optic link to 32 input ports of the DBF. This yields a maximum input data rate of 25.6 Gbit/s (800 Mbit/s per channel). Steering vector data from the radar's beam controller subsystem is sent to the DBF processor to define the amount of phase-shift to apply to steer the receive beam pattern in azimuth. Phase-correction information is also sent to the DBF from the Metrology/Calibration Processor to compensate for errors due to mechanical and electrical length variations in the 32 phase-centers of the array. As part of the technology demonstration for SBR, the raw data channels will also be stored to a solid-state recorder to later verify the on-board processing algorithm.

The performance drivers for the TTDs and phase-shifters are set by SBR's sidelobe level (SLL) requirements in azimuth. Table I summarizes the key requirements and system parameters for coherent beamforming. The fine (analog) adjustments in each TTD are made at each panel by switching between various lengths of sinuous microwave stripline before the RF-to-IF downconversion and A/D converter stages. The minimum time step resolution, t_d , is therefore limited by the switching losses in this stripline circuit.

The effect of having less than 100% true time delay adjustment in the array is that there will be a loss of coherence for signal frequency components further from the passband center frequency, $f_0 = 1.26$ GHz. Consider the case in which two adjacent antenna panels receive a 3-tone signal having bandwidth B and a remaining time lag t_d . The received signal at panel 1 is

$$x_1(t) = a_0 e^{j2\pi(f_0 - B/2)t} + a_1 e^{j2\pi f_0 t} + a_2 e^{j2\pi(f_0 + B/2)t}, \quad (1)$$

and the signal at the adjacent panel 2 is

$$x_2(t) = a_0 e^{j2\pi(f_0 - B/2)(t-t_d)} + a_1 e^{j2\pi f_0(t-t_d)} + a_2 e^{j2\pi(f_0 + B/2)(t-t_d)}. \quad (2)$$

The DBF processor then compensates for the remaining time delay in signal x_2 by applying a phase shift of $\phi_d = 2\pi f_0 t_d$. The

parameter	SAR	MITI
Peak antenna sidelobes	-13 dB	-35 dB
Mean antenna sidelobes	-20 dB	-50 dB
Bandwidth B	45-80 MHz	3-10 MHz
Maximum azimuth scan range θ_{az}	$\pm 28^\circ$	$\pm 45^\circ$
Analog TTD adjustment range	≥ 7 ns	
TTD net resolution t_d	≤ 1 ns	

Table I. Key requirements and system parameters for the SBR digital beamformer.

combined signal between panels is then

$$\sum_n x_n(t) = x_1(t) + e^{j\phi_d} x_2(t) = (1 + e^{j\pi B t_d}) a_0 e^{j2\pi(f_0 - B/2)t} + 2a_1 e^{j2\pi f_0 t} + (1 + e^{-j\pi B t_d}) a_2 e^{j2\pi(f_0 + B/2)t}. \quad (3)$$

For the finite bandwidth echo, the phase shift operation therefore causes dispersion in the panel 2 signal, which leads to a loss of coherence at the $f_0 \pm B/2$ band edges:

$$CL \text{ (coherence loss)} = \left| \frac{a_0 (1 + e^{j\pi B t_d})}{2a_0} \right|^2 = 10 \log_{10} \left[\frac{1 + \cos(\pi B t_d)}{2} \right] \text{ [dB]} \quad (4)$$

From (4), the time-bandwidth product $B t_d$ must be kept small ($\ll 1$) in order to minimize the coherence loss. For example, in the case of a full bandwidth 80 MHz return echo and the nominal time resolution of $t_d = 0.25$ ns, there is only a 3.6° error ($\pi B t_d$ radians) in the DBF's phase shift operation at the band edges. The resulting coherence loss is negligible (< 0.01 dB). Losses become more noticeable (a tenth of a dB or more) for $t_d > 1$ ns, and rapidly deteriorate once the TTD resolution approaches the scale of the digital sampling interval (5 ns).

Numerical floating-point simulations of the hybrid time-delay/phase-shift system in SBR have been developed in MATLAB to confirm the beamformer performance. The DBF output is expressed as

$$y(t) = \sum_{n=0}^{N-1} w_n x_n(t), \quad (5)$$

where $w_n = \exp(-j2\pi f_0 t_{dn})$ represents the steering vector that imparts the final phase correction and x_n represents the received channels from $N = 32$ antenna panels. The detected RF signals are modeled as short-pulse ($1/B$) Gaussian returns off of a point-target:

$$x_{RF}(t) = e^{-\ln 4 (Bt)^2} \cos(2\pi f_0 t). \quad (6)$$

A target location of $\theta_{az} = 30^\circ$ and a bandwidth of $B = 80$ MHz were chosen to emulate the beamforming in spotlight SAR mode, which is considered the most stringent condition for preserving coherence because it uses both a wide bandwidth and wide scan angle. The computed response in both azimuth (space) and range (time) showed that for a Hamming array taper, azimuth sidelobes of -42 dB were achieved, and that

there was no discernable loss of coherence in the power detected samples at $t = 0$ ns in range (center of pulse). This performance satisfies the peak SLL requirement of -35 dB for MTI radar modes and confirms that a TTD time resolution of 0.25 ns is adequate for maintaining phase coherence across the array.

III. DBF PROCESSOR DESIGN AND SIMULATION

A. CORDIC Digital Phase-Shifter Technique

Each of the 32 channels within the DBF processor contains an I/Q demodulator, digital phase-shifter, and amplitude-scaling module. After phase rotation and scaling, the 32 sub-channels are added together in a digital combiner network to generate either a single receive beam for SAR processing or multiple simultaneous beams (a primary beam plus several neighboring auxiliary beams) for space-time adaptive processing in MTI. The beamforming operation described in (5) has a total equivalent processing performance of 26×10^9 op/s for real-time, simultaneous SAR and MTI processing.

One of the key design aspects for achieving highly precise phase-shift computations in real-time is use of the CORDIC (Coordinate Rotation Digital Computer) technique [5], [6]. In CORDIC, the phase shift operation is carried out through a series of M smaller rotation stages at particular arctangent intervals, i.e., in phase shift intervals

$$\phi_m = \pm \tan^{-1}(1/2^m), \quad m = 0, \dots, M. \quad (7)$$

The sign of each ϕ_m value is chosen so that the net rotation (the sum of all ϕ_m angles) approaches the desired phase shift angle ϕ :

$$\phi = \sum_{m=0}^M \phi_m. \quad (8)$$

The phase precision can therefore be improved by increasing the number of iterations M . The choice of rotation angles in (7) is understood by looking at the math expression after each iteration. If z_m represents the complex output of the m^{th} CORDIC stage and $z_{m-1} = x_{m-1} + jy_{m-1}$ represents the complex input of that stage, then

$$z_m = z_{m-1} e^{\pm j \tan^{-1}(2^{-m})} = \frac{1}{\sqrt{1+2^{-2m}}} [(x_{m-1} \mp 2^{-m} y_{m-1}) + j(y_{m-1} \pm 2^{-m} x_{m-1})] \quad (9)$$

It follows that the rotation in arctangent intervals is accomplished using just a series of adders, subtractors, and binary right-shift (divide-by- 2^m) operators. The sequence of phase rotations can be implemented in the FPGA as a systolic digital process, in which a series of simple, repetitive logic functions are pipelined together to meet the DBF's high data throughput requirements.

A fixed-point (bit-true) CORDIC phase shifter module and testbench were designed in the Simulink language to

Fig. 2. Amplitude and phase precision simulation results for the 15-bit/15-stage CORDIC phase-shifter. The root-mean-square errors are plotted as a function of the input signal level (normalized to full scale).

study the effects of finite bit precision. The testbench generates input test vectors (1000 randomly distributed complex samples and phasor arguments) for both the CORDIC device under test and for an ideal, floating-point phase shifter. The amplitude and phase error statistics could then be calculated from the difference between the ideal and fixed-point output vectors.

After experimenting with various bit widths for the CORDIC's x , y , and ϕ registers, it was found that a 15 stage CORDIC with a 15 bit register width (8 bit A/D integer data + 6 fractional bits + 1 overflow bit) yielded sufficient precision for meeting the antenna sidelobe requirements [shown in the following section]. The fixed-point simulation results for the 15-bit CORDIC design are plotted in Fig. 2. This graph shows the rms phase and amplitude errors for the CORDIC output as a function of the normalized input signal level, σ/v_{FS} , where σ is the standard deviation and v_{FS} is the full scale value of the digitized input signal. At the optimum radar return level $\sigma = 1/4 v_{FS}$ (where the digital processor is neither limited by quantization noise nor by saturation), the CORDIC module performed with rms amplitude and phase precisions of 0.012 dB and 0.07°.

B. FPGA Implementation and Antenna Array Simulator Tests

The logic for a synchronous 32-to-1 DBF combiner with CORDIC phase shifters has been designed and implemented at the register transfer level in the Verilog HDL (hardware description language). The Xilinx Virtex-II XC2V6000 (six-million gate FPGA) has been chosen as the processing platform for implementing the DBF algorithm. The advantages of this particular FPGA are its high logic density, large number of I/O ports to support multi-Gbit/s data bandwidths, and reconfigurable SRAM-based technology which eases development time and cost.

Results from the Xilinx synthesis and mapping tools show that the current DBF design uses 51% of the available logic slices aboard the XC2V6000. Because multiple combiners will eventually need to be instantiated to support simultaneous, multiple beamforming modes in MTI, the board-level design of the DBF will likely require more than one Virtex-II part. In terms of speed performance, the post place-and-route static timing analysis passed at a maximum clock rate of 56.2 MHz, which gives more than 10% timing margin above the required 50 MHz clock rate for processing complex baseband data.

To link the bit-true CORDIC performance described in the previous section to the actual SBR sidelobe level performance, an antenna array simulator named *channelSim* was developed in MATLAB. *channelSim* generates the 32 wideband digital output channels from the panel radar electronics modules in the 50 m array. These output vectors are then sent to the fixed-point device under test—the digital beamformer designed in Verilog. The simulator generates the full bandwidth radar return signals received and combined over 12 azimuth antenna elements per panel for the case of a point target located at θ_{az} . As in the coherence loss tests, a target location of $\theta_{az} = 30^\circ$ and a bandwidth of $B=80$ MHz were chosen as a stringent test condition. It was assumed for simplicity and for testing the fundamental limits of the DBF design that the array was perfectly flat, with no electrical or mechanical distortion.

Functional simulations of the bit-true DBF Verilog hardware were run to test the peak and mean sidelobe level performance in the presence of quantization errors. Fig. 3 shows some of the array pattern results. The peak SLL using the 15-bit CORDIC implementation is -35.2 dB below the main lobe, thus meeting the most stringent requirement of -35 dB in MTI modes. A comparison between the golden (ideal floating-point) and fixed-point DBF performance also reveals that the grating lobes near 20° and 40° , which arise from the uniform illumination on each antenna panel, are masked out by the quantization noise floor in the fixed-point implementation. The implication for the antenna design is that it is suitable (and preferable for simplifying the antenna electronics) to use a uniform amplitude gain rather than a taper across the T/R elements within each panel. Bit-true testing of the beamformed pattern over the entire azimuth plane ($-90^\circ \leq \theta_{az} \leq +90^\circ$) resulted in an equivalent mean hemispheric SLL of -65.2 dB, which satisfies the -50 dB worst case requirement for SBR (Table I).

IV. CONCLUSION

A digital beamforming architecture and FPGA-based processor have been developed to enable advanced SAR and MTI on-board processing in the very large aperture (50 m) L-band Space Based Radar. Recent research efforts at NASA/JPL have involved DBF algorithm development, fixed-point modeling, and digital hardware implementation (hardware description language coding, synthesis, and testing), which have led to the delivery of working FPGA firmware that meets SBR's baseline requirements for phase precision and antenna sidelobe level response. The DBF processor and its related technologies—modular antenna

Fig. 3. Functional simulations of the DBF point-target response in azimuth. Top: bit-true processed output from the Verilog hardware description language. Bottom: the golden (floating-point) model output. The HDL simulation results demonstrate a peak sidelobe level performance of -35.2 dB and a dynamic range (limited by quantization noise) of 43 dB at the main lobe.

design, digital RF receivers, and fiber-optic data distribution—will have important implications for improving the overall phase-stability and calibration of large aperture radar systems like SBR.

ACKNOWLEDGMENT

The research described in this paper was performed by the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration.

REFERENCES

- [1] P. A. Rosen, S. Hensley, I. R. Joughin, F. K. Li, S. N. Madsen, E. Rodriguez, and R. M. Goldstein, "Synthetic aperture radar interferometry," *Proc. IEEE*, vol. 88, no. 3, pp. 331-382, Mar. 2000.
- [2] J. T. Booth, D. L. Evans, C. Heeg, Y. Kim, and D. M. Tralli, "A plan for living on a restless planet," *Earth Observ. Magazine*, pp. 14-21, Nov. 2003.
- [3] R. L. Jordan, B. L. Huneycutt, and M. Werner, "The SIR-C/X-SAR synthetic aperture radar system," *IEEE Trans. Geosci. Remote Sensing*, vol. 33, no. 4, pp. 829-839, July 1995.
- [4] D. L. Evans and A. Freeman, "Beyond SIR-C/X-SAR," *Proc. IEEE Aero. Applications Conference*, vol. 2, pp. 49-55, Feb. 1996.
- [5] J. E. Volder, "The CORDIC trigonometric computing technique," *IRE Trans. Elec. Computers*, pp. 330-334, Sept. 1959.
- [6] R. Andraka, "A survey of CORDIC algorithms for FPGA based computers," *Proc. 1998 ACM/SIGDA symp. field programmable gate arrays*, pp. 191-200, Monterey, CA, Feb. 1998.