22nm FDSOI Technology for Emerging Mobile, Internet-of-Things, and RF Applications

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***Abstract*—**22FDX™ is the industry's first FDSOI technology architected to meet the requirements of emerging mobile, Internet-of-Things (IoT), and RF applications. This platform achieves the power and performance efficiency of a 16/14nm FinFET technology in a cost effective, planar device architecture that can be implemented with ~30% fewer masks. Performance comes from a second generation FDSOI transistor, which produces nFET (pFET) drive currents of 910µA/µm (856µA/µm) at 0.8V and 100nA/µm Ioff. For ultra-low power applications, it offers low-voltage operation down to 0.4V V_{min} for 8T logic libraries, as well as 0.62V and 0.52V V_{min} for high-density and high-current bitcells, ultra-low leakage devices approaching 1pA/µm Ioff, and body-biasing to actively trade-off power and performance. Superior RF/Analog characteristics to FinFET are achieved including high f_T/f_{MAX} of 375GHz/290GHz and 260GHz/250GHz for nFET and pFET, respectively. The high f_{MAX} extends the capabilities to 5G and milli-meter wave (>24GHz) RF applications.

I. Introduction

Rising manufacturing costs and emerging applications requiring unparalleled energy efficiency are driving the need for new semiconductor device solutions. For the first time, an increase in the cost per die is observed with the introduction of 16/14nm FinFET technologies due to increased process complexity and mask count. Cost sensitive IoT and mobile applications are driving new requirements such as increased integration, advanced power management, and high performance RF and analog.

The Fully Depleted Silicon-On-Insulator (FDSOI) transistor architecture has inherent electrostatic control benefits and very low mismatch capability [1,2], making it a powerful option to fulfil those requirements while keeping process cost and complexity low. This paper presents the process architecture, baseline device and yield performance, the benefits of back-bias in power management, as well as key platform features of a new FDSOI technology based on 22nm design rules.

II. Technology Overview

A. Process Architecture

The 22nm FDSOI architecture provides maximum die scaling relative to 28nm while minimizing the expensive double-patterning steps required at the 16/14nm FinFET technology nodes. Approximately 75% of the process steps are common with the 28nm platform enabling high yield capability. The gate-first High-K Metal Gate (HKMG) integration is used to ensure a low cost process flow [3]. A typical cross-section of nFET and pFET devices is shown in Fig.1. All active devices are built on SOI whereas passive devices and select active devices, such as LDMOS, are conventionally formed in the bulk substrate (Fig.2). In addition to the introduction of FDSOI substrates, new process modules are introduced to support back-bias capability, passive device fabrication, enhanced device performance and technology scale factor (Fig.3). The introduction of a SiGe channel for pFET devices by the condensation technique [4] and SOI thickness <7nm enable high DC drive currents. A post STI hybrid etch process is used to form back gate contacts and enable the implementation of devices and tap-cells in the bulk substrate (Fig.4). Dual in-situ doped epi processes (Si:P and SiGe:B) are formed in combination with a low-k spacer to ensure highly doped source/drain regions while maintaining low gate-to-drain capacitance (critical for RF applications). Technology CPP is scaled without adding extra masking steps relative to the 28nm Front-End-of-Line. Dual patterning techniques are used to scale M1/M2 pitch, leading to a logic/SRAM die scaling of 0.72x/0.83x relative to the 28nm Poly/SiON technology node.

B. Device Performance

Device construction utilizes either flip well (SLVT/LVT devices) or conventional well (RVT/HVT devices) to enable a multiple V_T device suite. In the so called flip well construction, nFET devices are located on n-type back gates and pFET devices are located on p-type back gates. This configuration is well suited for forward back biasing (FBB), i.e. increasing performance. In contrast, the conventional well construction enables the reduction of Ioff leakage by using reverse back biasing to raise the V_T. Three gate lengths (20, 24, 28nm) are available for each of the four offered V_T flavors. Devices are measured at back gate voltages from 0V to 1V (Fig.5). A coupling factor $|dV_T/dV_B|$ of 75mV/V is reported. I_{DS}/I_{off} DC performance for nFET and pFET devices are reported at V_{dd}=0.8V (Figs.6-7). I_{DS}=910µA/µm and 856µA/µm at Ioff=100nA/µm are achieved with L=20nm and W=0.17µm for nFET and pFET, respectively. The FBB

impact is also reported. Extremely low $A_{\Delta VT}$ mismatch values of 1.2/1.4 mV·µm for nFET/pFET are demonstrated (Fig.8). The results on coupling factor, device performance, and V_T mismatch are in line with previously reported data for high performance FDSOI transistors [1,5]. Standard cell based ring oscillators have been investigated using logic test vehicles (Fig.9a and Fig.9b). Frequency vs. static and dynamic leakage were measured for V_{dd}=0.7, 0.8, and 0.9V. At V_{dd}=0.8V, matched ring oscillator frequency to V_{dd}=0.9V can be obtained by forward biasing the back gate (Fig.9a). This is achieved with only a slight increase in static leakage, while dynamic leakage is reduced by 10%. By utilizing the inherent capability of back-bias, optimization in standard cells can be realized resulting in circuit level performance on a par with FinFETs. Recent ARM simulations comparing FDSOI to FinFET have shown the benefit of back-bias, where product performance matches FinFET and in some use cases there is a power-performance advantage with 22nm FDSOI [6]. Frequencies and static power consumption were also measured for V_{dd}=0.6 and 0.8V (Fig.9b). At V_{dd}=0.6V a similar ring oscillator frequency to V_{dd}=0.8V can be obtained by biasing the back gate up to ~ 1.2V.

C. SRAM

A full suite of embedded SRAM bitcells is offered, inclusive of both 6-transitor single port and 8-transistor two port bitcells. The suite spans from high-density (HD) to ultra-low V_{min} across a wide range of leakage, performance and operating voltages. FDSOI technology provides excellent control on sources of V_T mismatch, such as random dopant fluctuations, due to elimination of channel doping. As a result, SRAMs are able to achieve a competitive $A_{\Delta VT}$ of 1.46mV·µm for nFET and 1.49mV·um for pFET devices. The low $A_{\Delta VT}$ values enable a 95% limited yield (LY) V_{min} of 0.62V (0.52V) at 25°C without the use of any design assist on a HD (High Current) bitcell (Fig.10 shows V_{min} of HD bitcell).

D. Test Product Yield

Besides achieving benchmark device performance and V_{min} SRAM yield, the technology has been implemented on test products showing high yield capability. A yield comparison between 22nm FDSOI and a high volume 28nm production process is shown in Fig.11. As can be seen, 22nm FDSOI is already achieving yield levels matching the reference production technology.

III. Platform Features

A. Ultra Low Leakage

Gate Induced Drain Leakage (GIDL) is a key parameter to achieve low off-state leakage current. In that context, the SiGe channel can be swapped with Si in order to reduce the leakage floor of the pFET devices (band gap of Si is larger than for SiGe compound materials). By doing so a GIDL reduction of more than 10x is demonstrated (inset in Fig.12b). Off-state currents <3pA/µm for V_{dd}=0.8V at room temperature are achieved (Fig.12). Further Ioff reduction can be obtained through process optimization and reverse back bias.

B. Ultra Low Power

Due to the superior electrostatic properties, circuit functionality on logic test vehicles is demonstrated down to a minimum operating voltage of 0.38V for nominal back gate voltages (Fig.13). The plot shows V_{min} read outs for two different libraries (8-track and 12-track height) resulting in similar V_{min} values ~150-300mV lower than 28nm reference libraries. A further reduction is possible by utilizing the inherent technology capability of back gate biasing, thus ensuring a certain gate overdrive at low V_{dd} operation due to the corresponding V_T reduction.

C. RF Integration

The use of a planar technology and gate first HKMG integration enables flexible layouts with lower resistances and capacitances compared to FinFET technology. The capability of the technology for RF applications is highlighted in Fig.14. f_T values of 375GHz and 260GHz are reported on thin oxide nFET and pFET devices. f_{MAX} values of 290GHz and 250GHz have also been achieved. This is the first time that RF performance is reported for both nFET and pFET devices in FDSOI. These f_{MAX} values make the technology capable of spanning the full suite of RF applications including 5G and mmWave (>24GHz), an application space that FinFET technology is extremely challenged to meet due to inherent parasitics. Low-frequency noise (LFN) is measured on similar devices (Fig.15). The measured flat-band voltage power spectrum density (SVg) at 100 Hz is $550 \cdot 10^{-15}$ $V^2 \cdot \mu m^2/Hz$ for nFET and pFET (0V back bias is applied). With a 2V forward back bias, there is no penalty (and slight benefit in the 1/f noise performance). The values are on a par with the ITRS2.0 target ($550 \cdot 10^{-15}$ $V^2 \cdot \mu m^2/Hz$).

IV. Conclusion

An industry first 22FDX™ platform demonstrating benchmark yield and performance designed for RF, low power, and low leakage applications is presented. The use of forward back-bias achieves matched frequency at lower V_{dd} and in turn lower active power. The benefits of back-bias can be further realized at the product level where simulations have shown comparable power-performance of 22nm FDSOI to FinFETs. Low off state leakage, 0.4V logic operation, high f_T/f_{MAX} performance, and low cost manufacturing make the technology a compelling offering to meet emerging markets in mobile, IoT, and RF.

Acknowledgment

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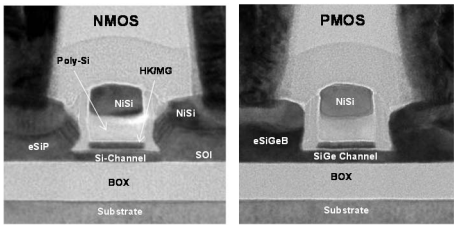

Fig.1. Typical cross-section of nFET and pFET transistors.

Device	SOI	Substrate	Comment
Core-FET	X		4 V_T flavors for logic + ULL devices
Io-FET	X		2 V_T flavors
LDMOS		X	Supporting 3.3V and 5.0V
Bitcells	X		HD, HC, LV, ULV, ULL, Two-port
Resistors	X	X	Poly, diffusion, well
BJT		X	
Varactors		X	
eFuse		X	
Diodes		X	
RF devices	X	X	Includes also inductors, APMOMs, etc.

Fig.2. 22nm FDSOI offers a complete device suite. All active transistors are built on SOI whereas most of the passive devices are built in bulk.

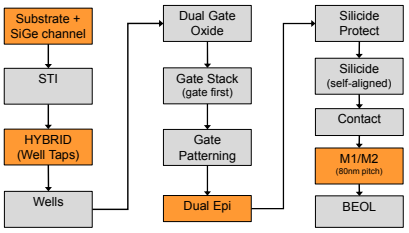

Fig.3. Schematic process flow. Marked process modules are unique to 22nm FDSOI whereas all other modules are copied directly from a mature 28nm high-k metal gate platform.

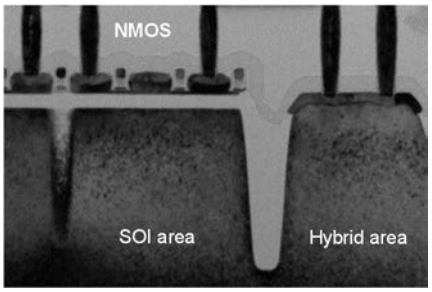

Fig.4. Cross-section showing co-integration of devices on bulk and SOI.

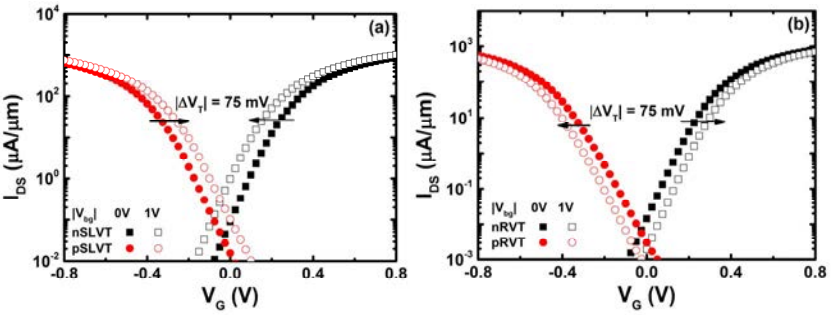

Fig.5. Typical transfer characteristics for nFET and pFET devices formed in flip-well (SLVT) and conventional-well (RVT) for |Vbg|=0V and 1V. A coupling factor of 75mV/V is demonstrated.

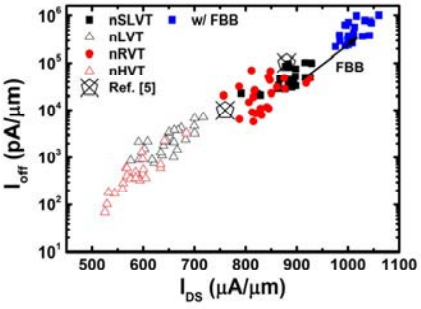

Fig.6. I_{DS}/I_{off} for nFET at V_{dd}=0.8V for L=20nm and W=0.17µm. V_{bg}=0V except for nSLVT where V_{bg}=0V and V_{bg}=0.8V (FBB) were used. Wide Ioff range in between 1nA/µm and 100nA/µm is demonstrated by the full device suite.

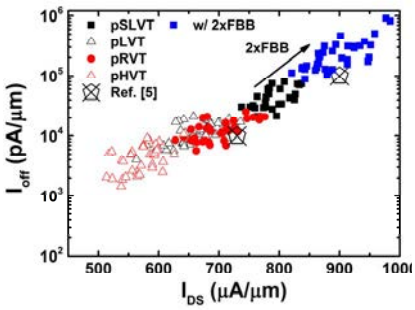

Fig.7. I_{DS}/I_{off} for pFET at V_{dd}=0.8V for L=20nm and W=0.17µm. V_{bg}=-0.8V except for pSLVT where V_{bg}=-0.8V and V_{bg}=-1.6V (FBB) were used. Wide Ioff range in between 1nA/µm and 100nA/µm is demonstrated by the full device suite.

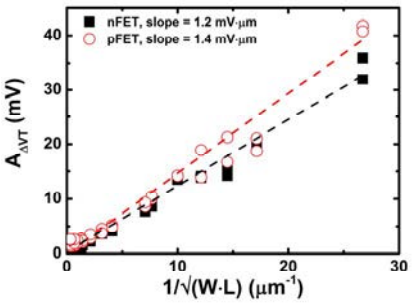

Fig.8. Mismatch measured on SLVT devices for various L and W dimensions. Very low $A_{\Delta VT}$ are reported (1.2mV.µm for nFET and 1.4mV.µm for pFET).

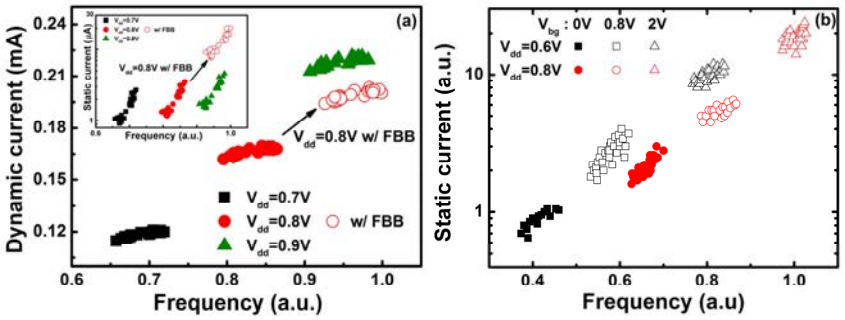

Fig.9. a) Dynamic current versus frequency for V_{dd}=0.7V, 0.8V and 0.9V. Empty symbols reports V_{dd}=0.8V with FBB. The corresponding static current is reported in the inset. b) Ring oscillator data for 0.6V and 0.8V. For each V_{dd} back gate voltages $|V_{bg}|$ were varied from 0 up to 2V.

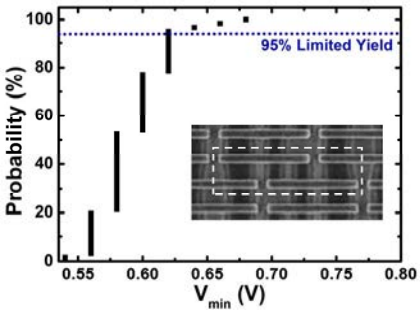

Fig.10. V_{min} cumulative distribution for HD 0.110μm² bitcell. 95% LY V_{min} of 0.62V at 25ºC without the use of any design assist.

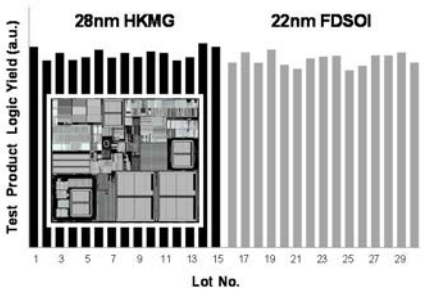

Fig.11. Test product logic yield comparison between 28nm HKMG and 22nm FDSOI.

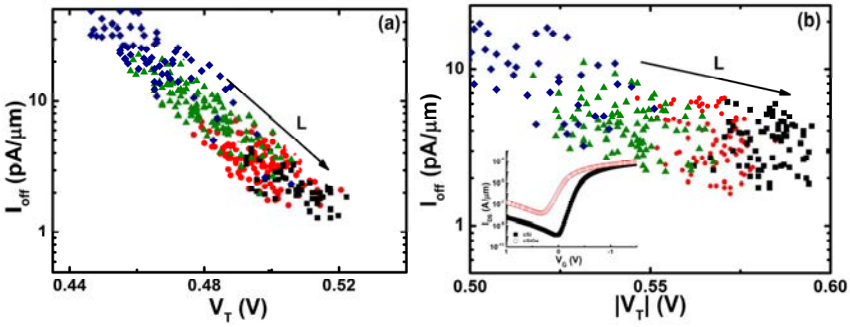

Fig.12. Ultra low leakage devices reaching down to single digit pA/μm off currents. V_{dd}=0.8V, a) nFET; b) pFET. Inset in Fig.12b: GIDL reduction by replacing SiGe channel material with Si.

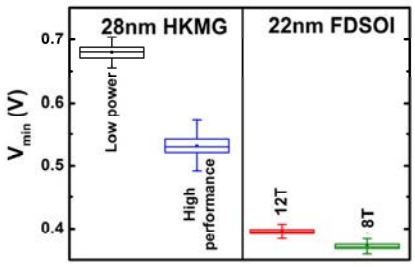

Fig.13. V_{min} capability <0.4V achieved and ~150-300mV lower compared to 28nm reference libraries.

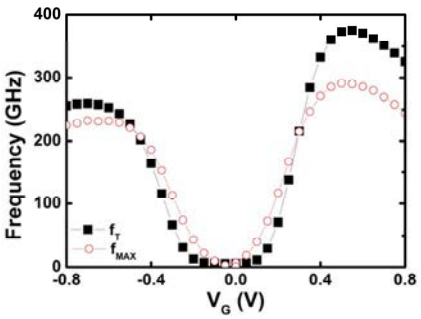

Fig.14. f_T and f_{MAX} versus V_G on nFET and pFET devices. f_T/f_{MAX}=375/290GHz for nFET and f_T/f_{MAX}=260/250GHz for pFET.

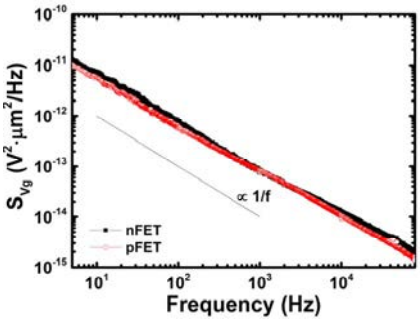

Fig.15. 1/f noise measurement on 22nm FDSOI thin oxide nFET and pFET devices with forward back bias.