2015 International Conference on Unmanned Aircraft Systems (ICUAS)
Denver Marriott Tech Center
Denver, Colorado, USA, June 9-12, 2015

Cognitive Radio Development for UAS Applications

Austin Anderson, Eric W. Frew, and Dirk Grunwald.
University of Colorado, Boulder, CO, 80309

***Abstract*—This paper presents an overview of unmanned aircraft systems developed at the University of Colorado and the development of a new software defined radio sensor that will be integrated into the existing systems. The architecture and performance of the new sensor is discussed. Potential research applications enabled by the radio sensor are covered.**

I. Introduction

Communications aware path-planning, data ferrying, and emitter localization are all major areas of research [1]–[3]. This work has, in the past, been conducted with off the shelf Wi-Fi cards using received signal strength indicator (RSSI) measurements to sense the RF environment. While RSSI is a very low-cost metric to use, it very much limits the type of experiments that can be conducted. More sophisticated metrics of the RF environment could be measured using a dedicated radio sensor.

Another major area of research is in the development of software defined radios (SDRs). These radios couple the flexibility of general purpose processors (GPPs) with the hardware acceleration performance of field programmable gate arrays (FPGAs). Recently, the advent of integrated GPP-FPGAs coupled with ultra-wide band radios-on-a-chip have made it feasible to host a high performance SDR on a small unmanned aircraft. This paper will cover the development of such an SDR and how it will fit in the existing unmanned aircraft system (UAS) framework [4]. It will conclude with a discussion of the potential applications of this system.

II. SDR Sensor

The WiSER (Wideband Software Extensible Radio) project[1] is developing a low-cost, high-performance software defined radio (SDR) platform for use in academic applications. The WiSER effort was motivated by a perceived lack of high performance, low cost, and small form factor SDRs. Ettus research offered a variety of radio platforms, but these typically contained small FPGAs forcing radio development to focus exclusively on software hosted on a powerful laptop or desktop [5]. The Rice WARP platform provided larger FPGAs, but at significantly increased cost [6]. The WiSER project will produce a software and firmware package targeting high-performance, low-cost system-on-chip development boards coupled with commercial, off-the-shelf (COTs) radio peripherals.

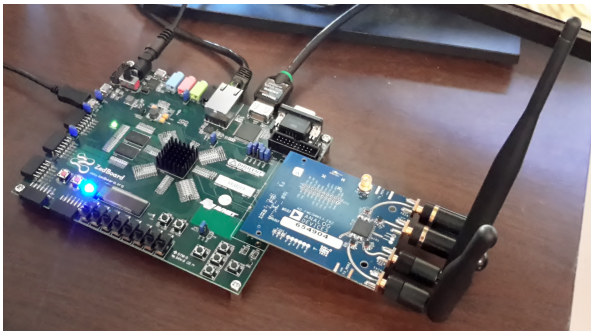

Fig. 1: WiSER hardware, Zynq Zedboard and Analog Devices AD9361 Radio Card.

A. SDR Hardware

The enabling technology behind the WiSER project is the Xilinx Zynq system-on-chip processor, and Analog Devices' AD9361 radio frequency integrated circuit (RFIC). While neither device offers revolutionary performance, they do offer significant performance at an unprecedented cost and size (Figure 1).

The Zynq processor integrates Xilinx 7-series FPGA fabric with a dual-core ARM processor

[1]NSF CRI grant #CNS-1305171

on the same die. Nearly every SDR integrates an FPGA with a general purpose processor, but it is particularly unique for the two to exist on the same die. This eliminates the need for multiple boards or at least multiple chips. The FPGA fabric is connected to the ARM processor using a high speed data bus. This bus gives the designer the option of pre-processing incoming radio data or passing full-rate in-phase and quadrature (IQ) samples to the processor. The WiSER effort uses the low-cost Zedboard, Zynq development platform.

The Analog Devices' AD9361 RFIC is a full-duplex, two-channel direct conversion transceiver capable of receiving and transmitting 56 MHz instantaneous bandwidth signals from 70 MHz to 6 GHz. RF signals can be preconditioned using manual or automatic gain control. The radio performs analog to digital conversions with 12-bits of precision on receive and transmit. While a wide instantaneous bandwidth and ultra-wide tuning bandwidth are not particularly unusual, it is again, very unique to be integrated into a single chip. This gives end users the ability to access a number of industrial, scientific, and medical (ISM) bands as well as a number of communication bands using a single radio chip. This represents a significant reduction in size, complexity, and cost while increasing performance relative to previous SDR radio front-ends. An Analog Devices FMCOMMS3 board breaks out the RFIC functionality to SMA connectors and an FPGA mezzanine card site for connection to the Zedboard. The expected performance characteristics of the sensor are documented in Figure 2.

A comparison of the size, weight, power, and cost of various SDRs is shown in Figure 3. The E310 is an SDR developed by Ettus Research that uses the same processor and radio as the WiSER, but is heavier and more expensive than the WiSER. What makes the WiSER particularly appealing is its ability to act as a standalone SDR. The Ettus N210 and WARP both require an external computer to run their radio processing. Because the Zynq chip integrates a CPU and FPGA on a single die, the WiSER sensor is able to provide high performance radio processing at a much lower cost and size.

B. SDR Software and Firmware Architecture

The primary goal of the WiSER effort is to develop software and firmware tools to exploit the capabilities of the new hardware. The ARM processor on the Zynq chip is capable of hosting a Linux operating system. This OS gives users access to open-source libraries including GNURadio [8]. This library provides a powerful set of tools for performing signal processing operations and data management tasks. Moreover, it provides a framework for developing new functionality. The GNURadio project is a constantly evolving library supported by an active digital community. Analog Devices has already released a driver and plug-in to interface their RFIC to GNURadio. The WiSER effort will build on this driver, improve its performance, and develop cross-compilation tools to reduce development times.

The unique nature of the Zynq chip presents a series of challenges for accomplishing this. As the ARM processor can host an operating system, the software package will include the necessary tools to build an operating system with the necessary packages. The WiSER effort will be based on an open-embedded operating system that is relatively light-weight and can be built using Xilinx tools to include various software packages. As the operating system is based on Linux, it requires a Kernel. The generic Xilinx Kernel has been modified to include Kernel drivers to configure and control the RFIC and manage direct memory access (DMA) transactions between the CPU and FPGA fabric. The software package includes the necessary drivers and scripts to compile this Kernel as well. In addition to building the OS and Kernel, the software package will include basic software applications. Analog Devices has already released a driver and plug-in to interface their RFIC to GNURadio. The performance of the Analog Devices DMA driver was bench-marked by establishing a DMA transfer from the FPGA fabric to the ARM processor. The amount of data transferred was counted for a fixed amount of time and an average data rate was calculated. This experiment was conducted for a number of commanded sampling rates to see how the DMA engine would perform. The results are shown in Figure 5.

	Tuning Range	Instantaneous Bandwidth	Channels	Digital Precision	Processor	FPGA Size
WiSER	70 MHz-6 GHz	0.2-56 MHz	2, Full Duplex	12-bits	Dual Core, 667 MHz	85K Logic Cells

Fig. 2: Expected radio and processing performance of WiSER sensor.

SDR	Dimension (w x l x h)	Weight	Power	Cost	Standalone?
WiSER	5.3" x 9.4" x 0.95"	0.43 lbs.	7W	$1069	Yes
Ettus E310*	2.7" x 5.2" x 1.0"	0.83 lbs.	6W	$2700	Yes
Ettus N210*	6.3" x 8.7" x 1.9"	2.6 lbs.	13.8W	$1717+Daughter Card	No
WARP v3 **	4.4" x 7.9" x 0.75"	0.59 lbs.	14.5W	$4900	No

* Taken from Ettus Datasheets

** Price taken from Mango Communications Website, size and power measured on actual hardware

Fig. 3: Size, weight, power, and cost of various SDRs.Data taken from hardware measurements and Ettus Research website [7]

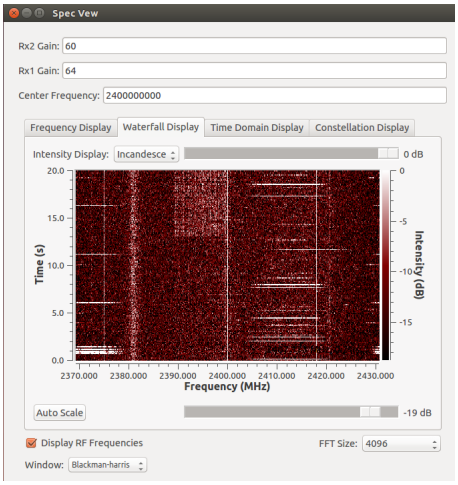

Fig. 4: Waterfall plot using GNURadio running on the Zedboard showing power at 2.4 GHz over time and frequency. WiFi emissions are visible as broad white lines in the spectrum.

The DMA driver provided by Analog Devices was able to keep up with the commanded sample rate up to 5 MSPS. Sampling rates in excess of 5 MSPS simply dropped data and resulted in 5 MSPS effective data transfer rates from the FPGA fabric to the ARM processor. The WiSER project is currently working to develop the Kernel driver and associated firmware based on the Xilinx AXI DMA engine to improve this performance.

Sample Rate	Number of Rx Channels	Average Data Rate
2 MSPS	1	1.99 MSPS
3 MSPS	1	3.02 MSPS
4 MSPS	1	4.01 MSPS
5 MSPS	1	4.98 MSPS
10 MSPS	1	4.98 MSPS
20 MSPS	1	4.98 MSPS

Fig. 5: Results of data rate experiment to benchmark DMA driver performance.

According to the Xilinx DMA Engine datasheet, transfer rates of 298 MB/s should be possible between the CPU and FPGA [9]. For a 64-bit bus this works out to a data rate of 39 MSPS. When this driver is finalized, a GNURadio block will be developed to interface it with that library. It has been found during testing, that the ARM CPU on the Zynq chip is relatively under-powered. This generally results in very long compilation times and limited radio processing performance. To address the first issue, the software package will include cross-development tools so that applications can be compiled on a faster computer and simply deployed to the ARM to run. The second

issue can be addressed by pushing some or most of the radio processing to the Zynqs FPGA fabric. This is the second main thrust of the WiSER project.

In addition to the software development, a firmware tool-set is being developed to leverage the full capabilities of the FPGA fabric on the Zynq chip. The firmware in the Zynq FPGA fabric will perform several functions. Primarily, it converts the digital lines from the RFIC into IQ data streams that are passed through a DMA engine to the CPU. Because the Zynq CPU is somewhat underpowered, the FPGA firmware will also be used to accelerate radio processing. Previous work has focused on developing a full 802.11 physical layer transceiver in FPGA fabric [10], enhanced physical (PHY) [11] and media access control (MAC) [12] layers as well as mechanisms for covert communication [13]. The WiSER effort will build on this work by breaking down the original, monolithic design into its fundamental building blocks. These building blocks will be used to build a digital signal processing library of FPGA firmware modules. This firmware library can be leveraged like the software modules of GNURadio to build signal processing chains in the FPGA fabric. Traditionally, FPGA development can be complicated and time consuming. To reduce the complexity and time required for firmware development, the WiSER firmware will include a network-on-chip. This leverages past research conducted at CU [14]. NoCs are lightweight firmware modules that connect processing elements in a network. This network provides standardized interfaces for processing elements and can be easily exploited by a CPU for hardware acceleration of processing tasks. Moreover, NoCs can be used to improve FPGA design performance by breaking down a single clock domain (monolithic design) to multiple clock domains [15]. While WiSER will use this processing architecture for SDR, it can also be applied to improve processing performance of generic algorithms. The use of NoCs for hardware acceleration of radio processing is being adopted in other SDR processing architectures [5].

Figure 4 depicts a basic application developed in GNURadio to sample the spectrum at 2.4GHz and visualize the results using a waterfall plot. These initial results were captured using Analog Device's OS, Kernel, drivers, and firmware. While the Analog Device's software and firmware package is good for initial prototyping, it has limited DMA bandwidth for data transfers between the CPU and FPGA. The WiSER development tools will improve DMA performance and include cross-development tools to reduce compilation times.

C. SDR Integration

The WiSER sensor will be hosted on a small unmanned aircraft. The sensor will be connected to a variety of antennas depending on the target application. Many SDR applications require fine time alignment between multiple platforms. To address this need, a GPS module will be included in the integration of the sensor on the aircraft. This module will be used to align the WiSERs internal timing with external systems. The sensor will act as a standalone system and can operate independently of the autopilot or interface with it to set or change flight plans. While the WiSER can interface to the autopilot directly, a small supervisory computer will be included in the aircraft integration. This supervisory computer can act as an intermediary between the autopilot and the WiSER sensor, or it can be bypassed completely. The architecture of the WiSER SDR is shown in Figure 6.

III. UAS Platform

The WiSER will be integrated into the Research and Engineering Center for Unmanned Vehicles (RECUV) Heterogeneous Unmanned Aircraft System (**R-HUAS**) [16]–[18]. The R-HUAS deploys a flock of miniature unmanned aircraft communicating via a meshed WiFi network [16]–[18].

A. Airframe

The WiSER will be integrated into a CU Skywalker X8 unmanned aircraft (Figure 7). The CU Skywalker X8 is made of EPO foam with a wingspan of 2.1 meters and takeoff weight of approximately 3.5 kg. This airframe provides a low cost platform with a large payload bay for flexible sensor integration. The Skywalker X8

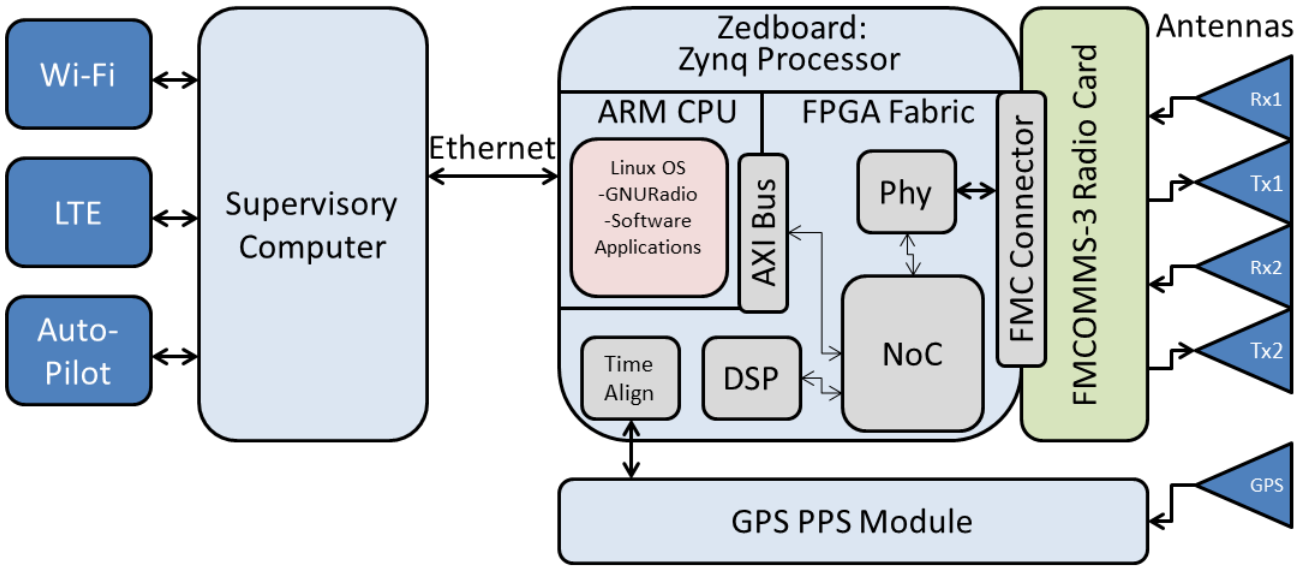

Fig. 6: WiSER Hardware, processing architecture, and integration into RECUV platform.

Fig. 7: The Skywalker X8 UAS.

kit was modified to use modular autopilot and payload packages that include an air data system comprised of a 3-axis magnetometer for improved attitude estimation, a Vaisala RS92 sonde for measuring temperature and humidity, and an Aeroprobe 5-hole probe for measuring the full aircraft-relative wind velocity vector; a video camera; or the WiSER device.

TABLE I: Airframe Specifications

	Skywalker X8
Wingspan	2.12m
GTOW	3.5kg
Motor	AX2820 KV780
Battery	5Ah 4S Lipo
Endurance	35 minutes
Launch	Hand Launch

B. Avionics

The 3DR Pixhawk is an advanced autopilot system designed by the PX4 open-hardware project and manufactured by 3D Robotics. Command and control of the Pixhawk is provided by several systems including the native 3DR Tower control application, a customized net-centric architecture, or the DroneDeploy Co-Pilot device [19] which is a cellular modem integrated with web-based mission management tools. The Pixhawk runs the ArduPilot open source autopilot. As the software is open source, developers can choose to alter the autopilot firmware directly or interact with the Pixhawk through the MAVLink protocol from a supervisory computer. ArduPilot supports soft-

ware in the loop simulations and can be controlled from a ground station using the open-source Tower mission planning software.

C. Flight Test Facility

Flight testing is conducted at the Table Mountain Radio Quiet Zone (2 x 2 mi.) near Boulder, CO, in the mountainous terrain in Boulder County, and in the Pawnee National Grasslands (20 x 20 mi.) outside of Greeley, CO. RECUV has obtained Certificates of Authorization (COAs) from the FAA for simultaneous flight operations of multiple aircraft at these sites. The Table Mountain COA provides a small flight test area near the CU Boulder campus that is designated radio quiet. This is advantageous for conducting passive RF data collecting missions. The Pawnee National Grasslands COA provides a much larger area to conduct flight tests. In addition to these, RECUV has also obtained a COA for an area in Boulder county. Figure 8 depicts the area provided for in the new COA. This area includes very mountainous terrain which is ideal for conducting simulated search and rescue experiments or wildlife tracking experiments.

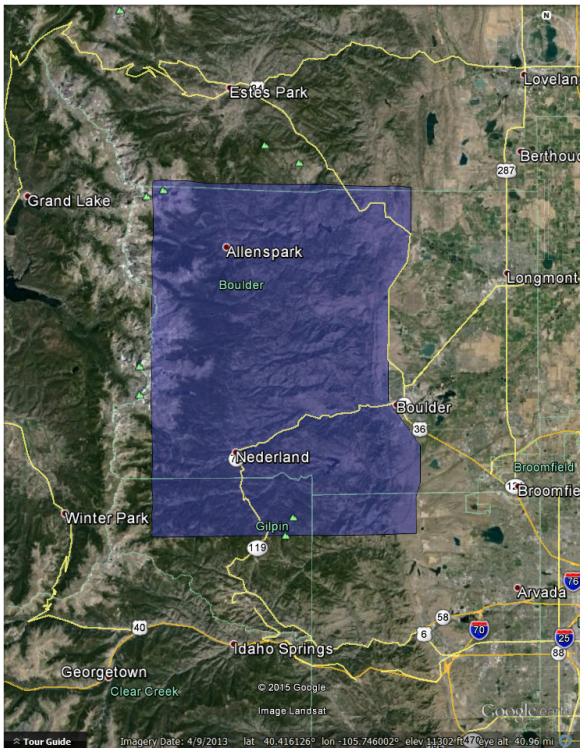

Fig. 8: Boulder county COA, 2014-WSA-113-COA.

IV. Applications

Integration of the WiSER cognitive radio into the R-HUAS is motivated by the need to improve channel monitoring in a communication-aware information gathering framework (Figure 9). Previous radio research conducted by RECUV was limited to using measurements of RSSI and data throughput as these were the only metrics available from the on-board WiFi cards [20]. The WiSER SDR sensor will give access to raw IQ data that can be preprocessed by the FPGA fabric, passed to the CPU, or even passed to a ground station. The new SDR sensor would replace the WiFi cards and RSSI measurements at the channel monitoring stage.

Access to IQ data allows for custom application development that can expose a variety of radio metrics from timing information to Doppler shift estimation. Moreover, the wide-band nature of the radio allows for application development at frequency bands that were simply unavailable to the WiFi card alone. Open source tools like GNURadio provide a powerful tool for rapid application development.

Because it is highly reconfigurable and covers a wide range of frequency bands, the WiSER can be configured to accomplish a variety of radio processing applications that traditionally would require application specific radio circuits. This opens up opportunities for research in a variety of areas:

- **Emitter Localization and Mapping:** Enhanced radio sensing gives access to improved metrics with which to localize emitters. For example, custom FPGA firmware can be developed to monitor the autocorrelation sequence embedded in WiFi signals to estimate the power of the signal in a more reliable manner than RSSI. As the WiSER sensor is not limmited to WiFi bands alone, signal strength localization applications can be developed for a variety of signals that fall in the SDR's tuning range.
- **GPS Denied Radio Navigation:** Timing information is embedded in a number of mod-

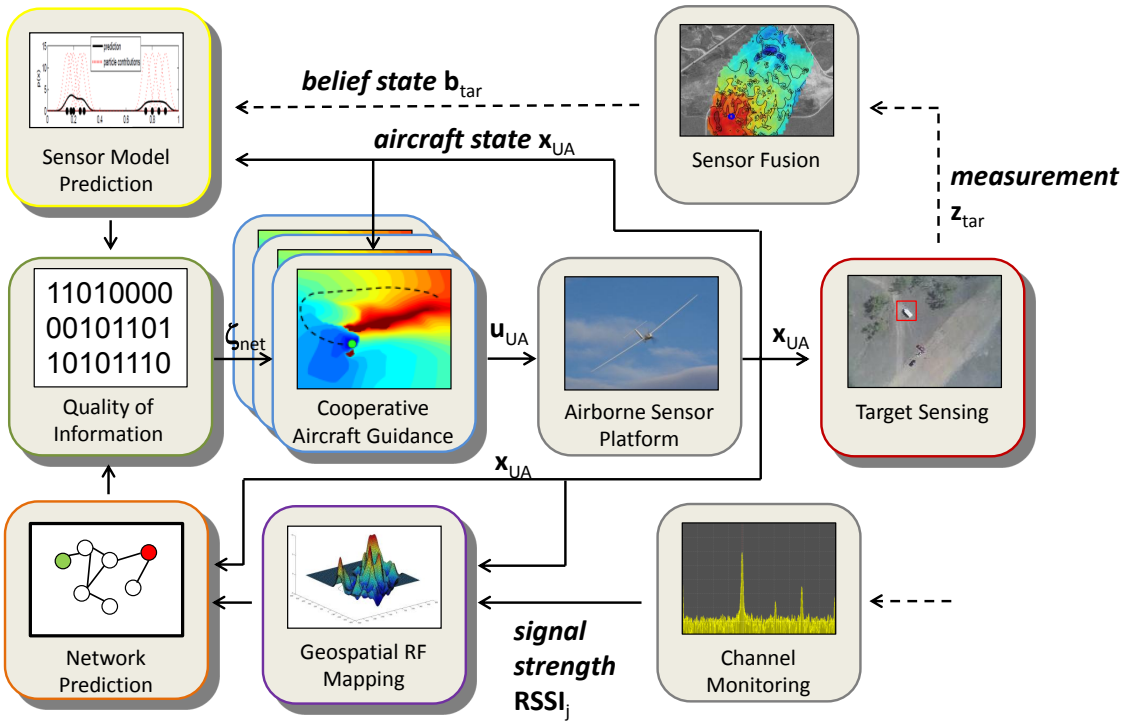

Fig. 9: Communication-aware information gathering framework.

ern RF signaling specifications. This information can potentially be extracted by an SDR to either aide a GPS navigation solution or substitute for GPS entirely using multi-spectral techniques such as those explored in DARPA's "All Source Positioning and Navigation" program [21].

- **Sense and Avoid:** Integration of UAS into the National Airspace hinges on developing a reliable methodology for sense and avoid. The WiSER SDR can be used to access aircraft transponder data for this purpose. Alternatively, this platform would be suitable for the development of a low size, weight, and power (SWaP) radar for use in sense and avoid.
- **Interference Detection:**The detection of unauthorized or interfering transmissions is very important as the amount of usable radio spectrum continues to shrink. Current systems for interference detection rely heavily on either static emplacements or ground based tracking equipment. Because the WiSER sensor can tune over such a wide bandwidth and can cover large geographic areas rapidly, it is a good candidate for automating the detection and localization of interference sources.
- **Low SWaP Computing:** Advanced guidance and control algorithms can be computationally expensive. The WiSER sensor will include a NoC architecture in its FPGA fabric designed expressly for hardware acceleration of computations. This coupled with the reconfigurable nature of FPGAs make WiSER a suitable candidate for exploring distributed computing amongst a swarm of small UAVs.

The integration of the WiSER sensor will aim to build on past work in emitter localization. In the near term, realistic flight experiments will be conducted to explore the following applications:

- **Characterization of the Radio Environ-**

ment: RF characterization consists of mapping the received radio signal strength over a range of frequencies in a given environment. RF characterization is critical for identifying emitting sources over the ambient background [22].

- **Search and Rescue:** The authors will collaborate with the Rocky Mountain Rescue group (RMR) to perform wilderness search and rescue operations. The sensing problem will consist of visual and infra-red video cameras to detect moving ground targets. The localization of emitters of opportunity carried by targets will be explored to augment the visual search. The SDR could be configured to monitor the power of emitters of opportunity or even be configured to imitate a WiFi router or cellular base station to aide in localization.
- **Wildflife Radio Collar Tracking:** The authors plan to collaborate with the Colorado Parks and Wildlife Division to track radio collars currently fit onto wildlife in Boulder County. Currently, collars are localized by rangers using high gain antennas on foot in a time-consuming process or in a piloted aircraft that is expensive to rent. The power, frequency, and timing of the signals emitted by the collars can be detected and measured by WiSER to both discriminate between different collars and track the movement of the wildlife. The combination of WiSER's ability to automatically detect and track collars, and the Skywalker's ability to cover wide geographic areas in a short time will result in a significant improvement in performance compared to current methods.

V. Conclusion

The development of a small, high-performance SDR will greatly increase the RF sensing capabilities of RECUV's current unmanned aircraft. Sophisticated RF sensing will enable research in topics ranging from radio navigation to sense and avoid. The WiSER effort will produce a toolset to greatly reduce the complexity of radio application development by leveraging existing tools like GNURadio. Flight tests will be conducted in the near term to verify the performance of the SDR as the WiSER toolset is developed.

References

[1] M. Stachura and E. W. Frew, "Cooperative target localization with a communication aware unmanned aircraft system," *AIAA Journal of Guidance, Control, and Dynamics*, vol. 34, no. 5, September 2011.

[2] A. J. Carfang, E. W. Frew, and D. Kingston, "Cascaded optimization of aircraft trajectories for persistent data ferrying," *AIAA Journal of Aerospace Information Systems*, January 2015.

[3] A. Carfang, N. Wagle, and E. W. Frew, "Improving data ferrying by iteratively learning the radio frequency environment," in *2014 IEEE/RSJ International Conference on Intelligent Robots and Systems (IROS)*, Chicago, IL, Sept 2014.

[4] E. W. Frew, B. Argrow, D. Lawrence, J. Elston, and M. Stachura, "Unmanned aircraft systems for communication and atmospheric sensing missions," in *American Control Conference*, Washington DC, June 2013.

[5] J. Malsbury and M. Ettus, "Simplifying fpga design with a novel network-on-chip architecture," *Proceedings of the second workshop on Software radio implementation forum - SRIF '13*, p. 45, 2013.

[6] P. Murphy, A. Sabharwal, and B. Aazhang, "Design of warp: A wireless open-access research platform," *European Signal Processing Conference*, 2006.

[7] "Ettus research - products."

[8] "Wikistart - gnu radio - gnuradio.org."

[9] P. S. Guide, "Table of contents table of contents," pp. 1–98, 1996.

[10] A. Dutta, D. Saha, D. Grunwald, and D. Sicker, "An architecture for software defined cognitive radio categories and subject descriptors," 2010.

[11] D. Saha, A. Dutta, D. Grunwald, and D. Sicker, "Gratis: Free bits in the network," *IEEE Transactions on Mobile Computing*, vol. 99, no. PrePrints, p. 1, 2013.

[12] A. Dutta, D. Saha, D. Grunwald, and D. Sicker, "Smack: a smart acknowledgment scheme for broadcast messages in wireless networks," in *ACM SIGCOMM Computer Communication Review*, vol. 39, no. 4. ACM, 2009, pp. 15–26.

[13] ——, "Secret agent radio: Covert communication through dirty constellations," in *Information Hiding*, ser. Lecture Notes in Computer Science, M. Kirchner and D. Ghosal, Eds. Springer Berlin Heidelberg, 2013, vol. 7692, pp. 160–175.

[14] G. Schelle and D. Grunwald, "Exploring fpga network on chip implementations across various application and network loads," *Proceedings - 2008 International Conference on Field Programmable Logic and Applications, FPL*, pp. 41–46, 2008.

[15] M. K. Papamichael and J. C. Hoe, "{CONNECT }: Re-examining conventional wisdom for designing {nocs} in the context of {fpgas}," *International Symposium on Field-Programmable Gate Arrays*, pp. 37–46, 2012.

[16] T. X. Brown, B. M. Argrow, E. W. Frew, C. Dixon, D. Henkel, J. Elston, and H. Gates, *Experiments Using Small Unmanned Aircraft to Augment a Mobile Ad Hoc Network*, 2007, no. ISBN-13: 9780521895842, ch. 28, pp. 123–145.

[17] E. W. Frew, C. Dixon, J. Elston, B. Argrow, and T. X. Brown, "Networked communication, command, and control of an unmanned aircraft system," *AIAA Journal of Aerospace Computing, Information, and Communication*, vol. 5, no. 4, pp. 84–107, April 2008.

[18] J. Elston, E. W. Frew, D. Lawrence, P. Gray, and B. Argrow, "Net-centric communication and control for a heterogeneous

unmanned aircraft system," *Journal of Intelligent and Robotic Systems*, vol. 56, pp. 199–232, Sept 2009.

[19] (2015) Dronedeploy. [Online]. Available: https://www.dronedeploy.com/

[20] M. Stachura and E. W. Frew, "Wifi localization experiments with an unmanned aircraft system," no. August, 2011.

[21] S. T.-N. O. Defense Advanced Research Projects Agency, "All source positioning and navigation (aspn)," no. November, p. 11, 2010.

[22] N. Wagle and E. W. Frew, "Online evaluation of communication models derived via transfer learning," in *Wireless Networking for Unmanned Autonomous Vehicles*, Anaheim, CA, Dec. 2012.